4-20mA Current-Loop Transmitter

FEATURES

- LOW QUIESCENT CURRENT: 130μA
- 5V REGULATOR FOR EXTERNAL CIRCUITS
- LOW SPAN ERROR: 0.05%
- LOW NONLINEARITY ERROR: 0.003%
- WIDE-LOOP SUPPLY RANGE: 7.5V to 40V
- MSOP-8 AND DFN-8 PACKAGES

APPLICATIONS

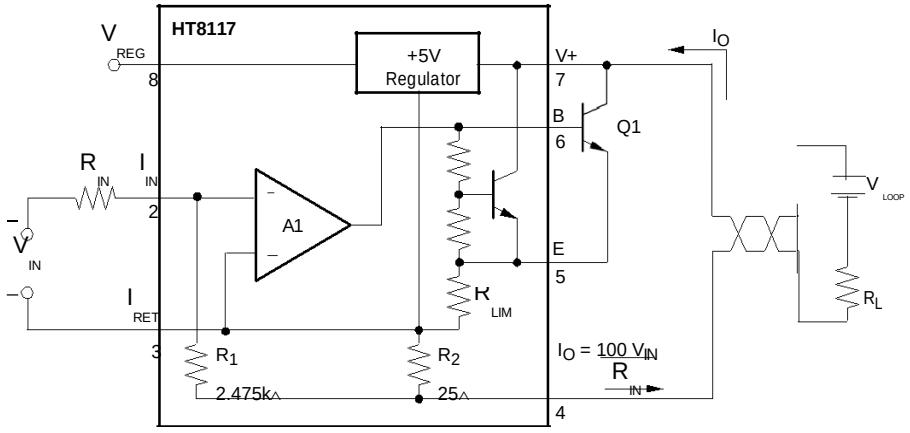
- TWO-WIRE, 4-20mA CURRENT LOOP TRANSMITTER
- SMART TRANSMITTER
- INDUSTRIAL PROCESS CONTROL
- TEST SYSTEMS
- CURRENT AMPLIFIER
- VOLTAGE-TO-CURRENT AMPLIFIER

DESCRIPTION

The HT8117C is a precision current output converter designed to transmit analog 4-20mA signals over an industry-standard current loop. It provides accurate current scaling and output current limit functions.

The on-chip voltage regulator (5V) can be used to power external circuitry. A current return pin (I_{RET}) senses any current used in external circuitry to assure an accurate control of the output current.

The HT8117C is a fundamental building block of smart sensors using 4-20mA current transmission. The HT8117C is specified for operation over the extended industrial temperature range, −40°C to +125°C.



ABSOLUTE MAXIMUM RATINGS(1)

PowerSupply,V+(referencedtoIopin)	+50V
Input Voltage, (referenced to I_{RET} pin)	0V to V+
Output Current Limit	Continuous
V_{REG}, Short-Circuit	Continuous
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Junction Temperature	+165°C
ESD Rating (Human Body Model)	2000V
(Charged Device Model)	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

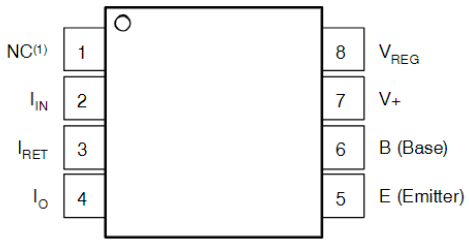
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
HT8117CRMZ	MSOP-8	R	R
HT8117CRDZ	DFN-8	R	R

(1) Please refer to for packing specification7 inch disk 1K per package, 13 inch disk 2.5K per package.

PIN ASSIGNMENTS

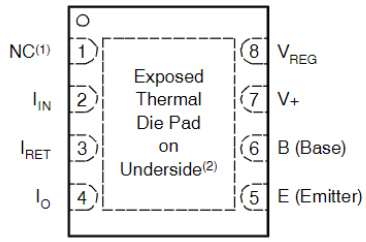
Top View

HT8117CRMZ



MSOP−8

HT8117CRDZ



DFN−8

NOTES: (1) NC = No connection. Leave unconnected on PCB.
(2) Connect thermal die pad to I_{RET} or leave unconnected on PCB.

ELECTRICAL CHARACTERISTICS: V+ = +24V

Boldface limits apply over the temperature range, **T_A = –40°C to +125°C**.

All specifications at T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, and TIP29C external transistor, unless otherwise noted.

PARAMETER		CONDITION	HT8117C MIN	HT8117C TYP	HT8117C MAX	UNITS
OUTPUT						
Output Current Equation	I_O			$I_O = I_{IN} \times 100$		
Output Current, Linear Range			0.20		30	mA
Over-Scale Limit	I_{LIM}			32		mA
Under-Scale Limit	I_{MIN}	I_{REG} = 0		0.13	0.20	mA
SPAN						
Span (Current Gain)	S			100		A/A
Error[1]		I_O = 200µA to 25mA		±0.05	±0.4	%
vs Temperature		**T_A = –40°C to +125°C**		**±3**	**±20**	**ppm/°C**
Nonlinearity		I_O = 200µA to 25mA		±0.003	±0.02	%
INPUT						
Offset Voltage (Op Amp)	V_{OS}	I_{IN} = 40µA		±100	±500	µV
vs Temperature		**T_A = –40°C to +125°C**		**±0.7**	**±6**	**µV/°C**
vs Supply Voltage, V+		V+ = 7.5V to 40V		+0.1	+2	µV/V
Bias Current	I_B			–35		nA
vs Temperature		**T_A = –40°C to +125°C**		**150**		**pA/°C**
Noise: 0.1Hz to 10Hz	e_n			0.6		μV_{PP}
DYNAMIC RESPONSE						
Small-Signal Bandwidth		C_{LOOP} = 0, R_L = 0		380		kHz
Slew Rate				3.2		mA/µs
V_{REG}[2]						
Voltage				5		V
Voltage Accuracy		I_{REG} = 0		±0.05	±0.1	V
vs Temperature		**T_A = –40°C to +125°C**		**±0.1**		**mV/°C**
vs Supply Voltage, V+		V+ = 7.5V to 40V		1		mV/V
vs Output Current				See Typical Characteristics		
Short-Circuit Current				12		mA
POWER SUPPLY						
Specified Voltage Range	V+			+24		V
Operating Voltage Range			+7.5		+40	V
Quiescent Current	I_Q			130	200	µA
Over Temperature		**T_A = –40°C to +125°C**			**250**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+125	°C
Storage Range			–55		+150	°C
Thermal Resistance	θ_{JA}					
MSOP				150		°C/W
DFN				53		°C/W

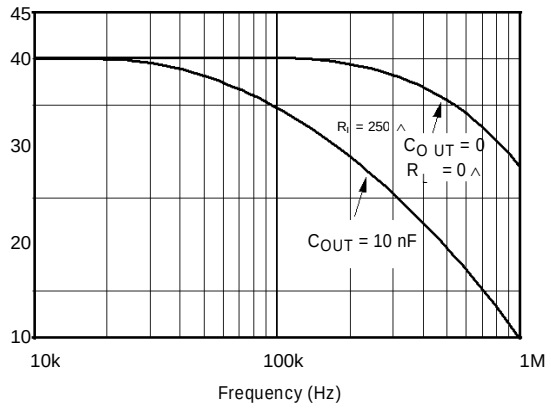
(1) Does not include initial error or temperature coefficient of R_{IN}.

(2) Voltage measured with respect to I_{RET} pin.

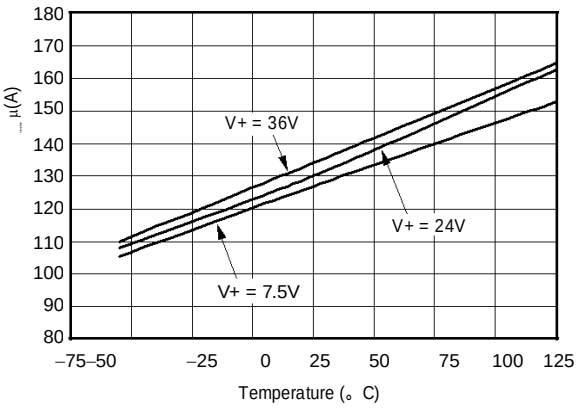
TYPICAL CHARACTERISTICS: V+ = +2.7V to +5.5V

At T_A = +25°C, V+ = 24V, R_{IN} = 20kΩ, and TIP29C external transistor, unless otherwise noted.

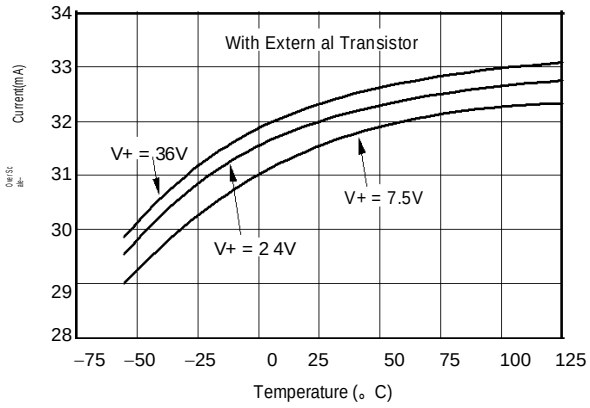
CURRENT GAIN vs FREQUENCY



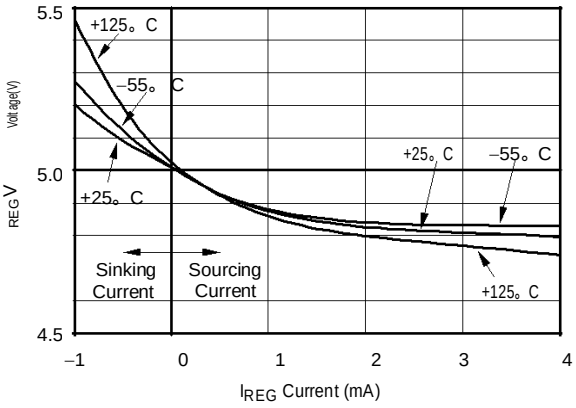
QUIESCENT CURRENT vs TEMPERATURE



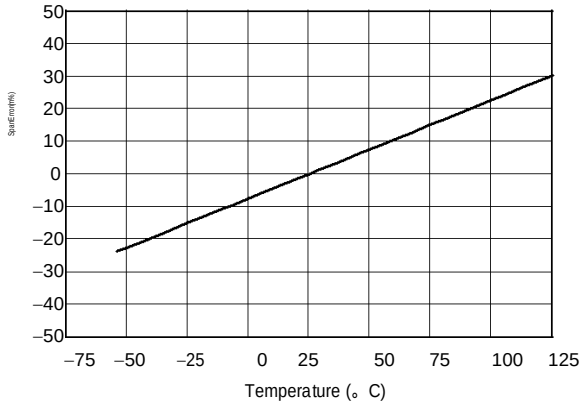
OVER-SCALE CURRENT vs TEMPERATURE



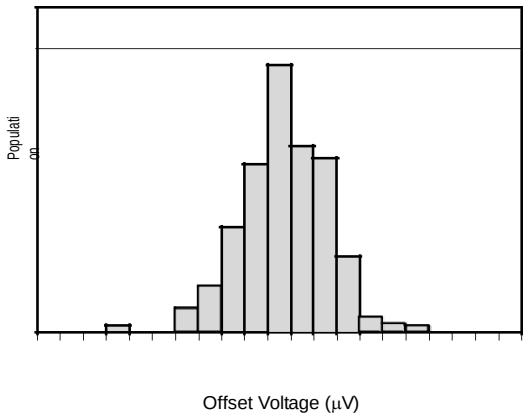
V_{REG} VOLTAGE vs V_{REG} CURRENT



SPAN ERROR vs TEMPERATURE



OFFSET VOLTAGE DISTRIBUTION



APPLICATIONS INFORMATION

BASIC OPERATION

The HT8117C is a precision current output converter designed to transmit analog 4-20mA signals over an industry-standard current loop. Figure 1 shows basic circuit connections with representative simplified input circuitry. The HT8117C is a two-wire current transmitter. Its input current (pin 2) controls the output current. A portion of the output current flows into the V+ power supply, pin 7. The remaining current flows in Q_1. External input circuitry connected to the HT8117C can be powered from V_{REG}. Current drawn from these terminals must be returned to I_{RET}, pin 3. The $I_{RE\ T}$ pin is a *local ground* for input circuitry driving the HT8117C.

The HT8117C is a current-input device with a gain of 100. A current flowing into pin 2 produces $I_O = 100 \times I_{IN}$. The input voltage at the I_{IN} pin is zero (referred to the I_{RET} pin). A voltage input is converted to an input current with an external input resistor, R_{IN}, as shown in Figure 1. Typical full-scale input voltages range from 1V and upward. Full-scale inputs greater than 0.5V are recommend to minimize the effects of offset voltage and drift of A1.

EXTERNAL TRANSISTOR

The external transistor, Q_1, conducts the majority of the full-scale output current. Power dissipation in this transistor can approach 0.8W with high loop voltage (40V) and 20mA output current. The HT8117C is designed to use an external transistor to avoid on-chip, thermal-induced errors. Heat produced by Q_1 will still cause ambient temperature changes that can influence the HT8117C performance. To minimize these effects, locate Q_1 away from sensitive analog circuitry, including HT8117C. Mount Q_1 so that heat is conducted to the outside of the transducer housing.

The HT8117C is designed to use virtually any NPN transistor with sufficient voltage, current and power rating. Case style and thermal mounting considerations often influence the choice for any given application. Several possible choices are listed in Figure 1. A MOSFET transistor will not improve the accuracy of the HT8117C and is not recommended.

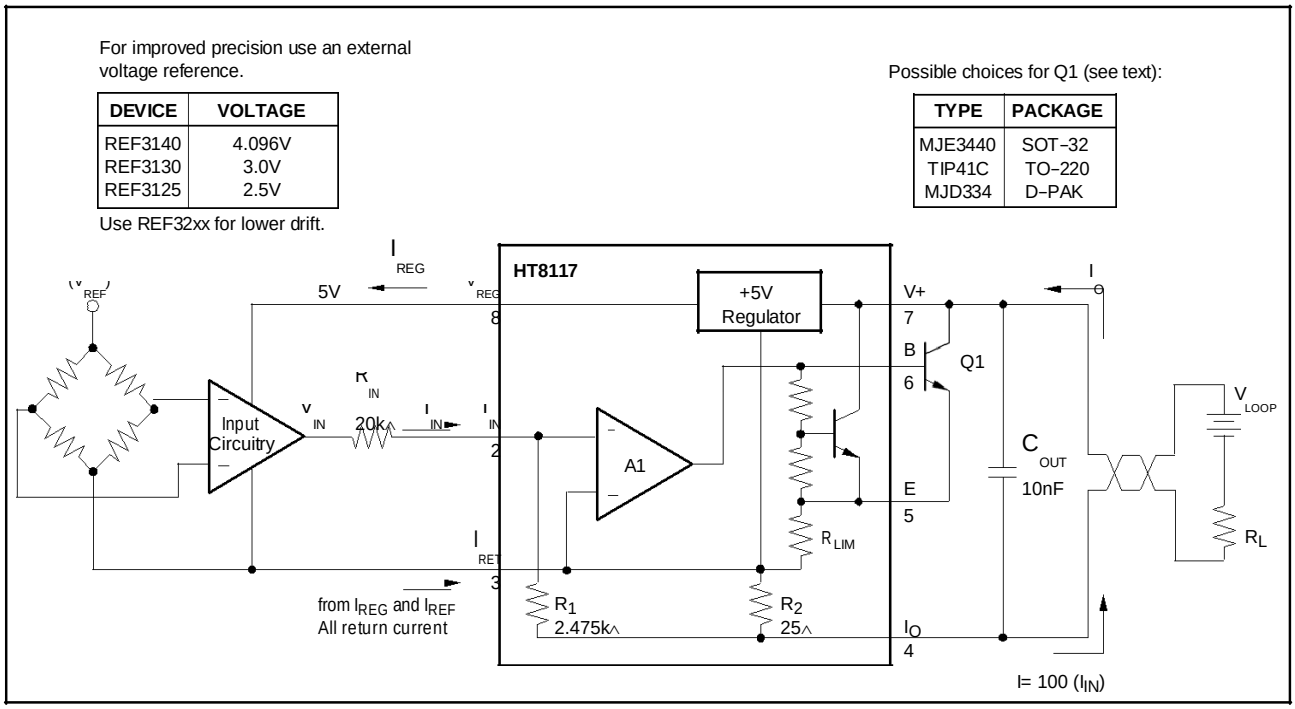


Figure 1. Basic Circuit Connections

MINIMUM OUTPUT CURRENT

The quiescent current of the HT8117C (typically 130μA) is the lower limit of its output current. Zero input current (I_{IN} = 0) will produce an I_O equal to the quiescent current. Output current will not begin to increase until $I_{IN} > I_Q/100$. Current drawn from V_{REG} will be added to this minimum output current. Up to 3.8mA is available to power external circuitry while still allowing the output current to go below 4mA.

OFFSETTING THE INPUT

A low-scale output of 4mA is produced by creating a 40μA input current. This input current can be created with the proper value resistor from an external reference voltage (V_{REF}) as shown in Figure 2. V_{REG} can be used as shown in Figure 2 but will not have the temperature stability of a high quality reference such as the REF3125.

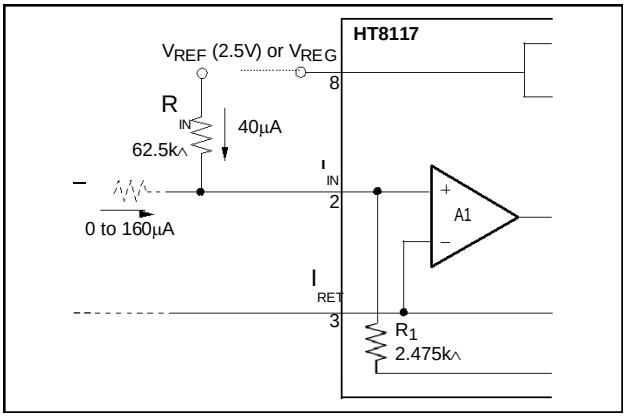


Figure 2. Creating Low-Scale Offset

MAXIMUM OUTPUT CURRENT

The HT8117C provides accurate, linear output up to 25mA. Internal circuitry limits the output current to approximately 32mA to protect the transmitter and loop power/measurement circuitry.

It is possible to extend the output current range of the HT8117C by connecting an external resistor from pin 3 to pin 5, to change the current limit value. Since all output current must flow through internal resistors, it is possible to cause internal damage with excessive current. Output currents greater than 45mA may cause permanent damage.

REVERSE-VOLTAGE PROTECTION

The HT8117C low compliance voltage rating (minimum operating voltage) of 7.5V permits the use of various voltage protection methods without compromising operating range. Figure 3 shows a diode bridge circuit which allows normal operation even when the voltage connection lines are reversed. The bridge causes a two diode drop (approximately 1.4V) loss in loop supply voltage. This voltage drop results in a compliance voltage of approximately 9V—satisfactory for most applications. A diode can be inserted in series with the loop supply voltage and the V+ pin to protect against reverse output connection lines with only a 0.7V loss in loop supply voltage.

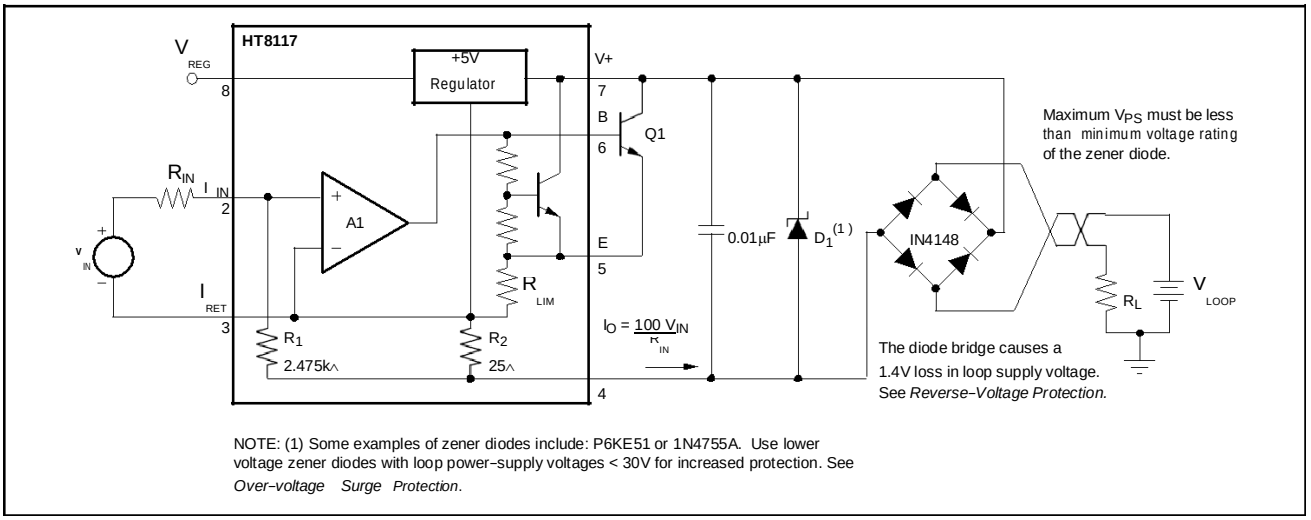


Figure 3. Reverse Voltage Operation and Over-Voltage Surge Protection

OVER-VOLTAGE SURGE PROTECTION

Remote connections to current transmitters can sometimes be subjected to voltage surges. It is prudent to limit the maximum surge voltage applied to the HT8117C to as low as practical. Various zener diode and surge clamping diodes are specially designed for this purpose. Select a clamp diode with as low a voltage rating as possible for best protection. Absolute maximum power-supply rating on the HT8117C is specified at +50V. Keep overvoltages and transients below +50V to ensure reliable operation when the supply returns to normal (7.5V to 40V).

Most surge protection zener diodes have a diode characteristic in the forward direction that will conduct excessive current, possibly damaging receiving-side circuitry if the loop connections are reversed. If a surge protection diode is used, a series diode or diode bridge should be used for protection against reversed connections.

RADIO FREQUENCY INTERFERENCE

The long wire lengths of current loops invite radio frequency (RF) interference. RF interference can be rectified by the input circuitry of the HT8117C or preceding circuitry. This effect generally appears as an unstable output current that varies with the position of loop supply or input wiring. Interference may also enter at the input terminals. For integrated transmitter assemblies with short connections to the sensor, the interference more likely comes from the current loop connections.

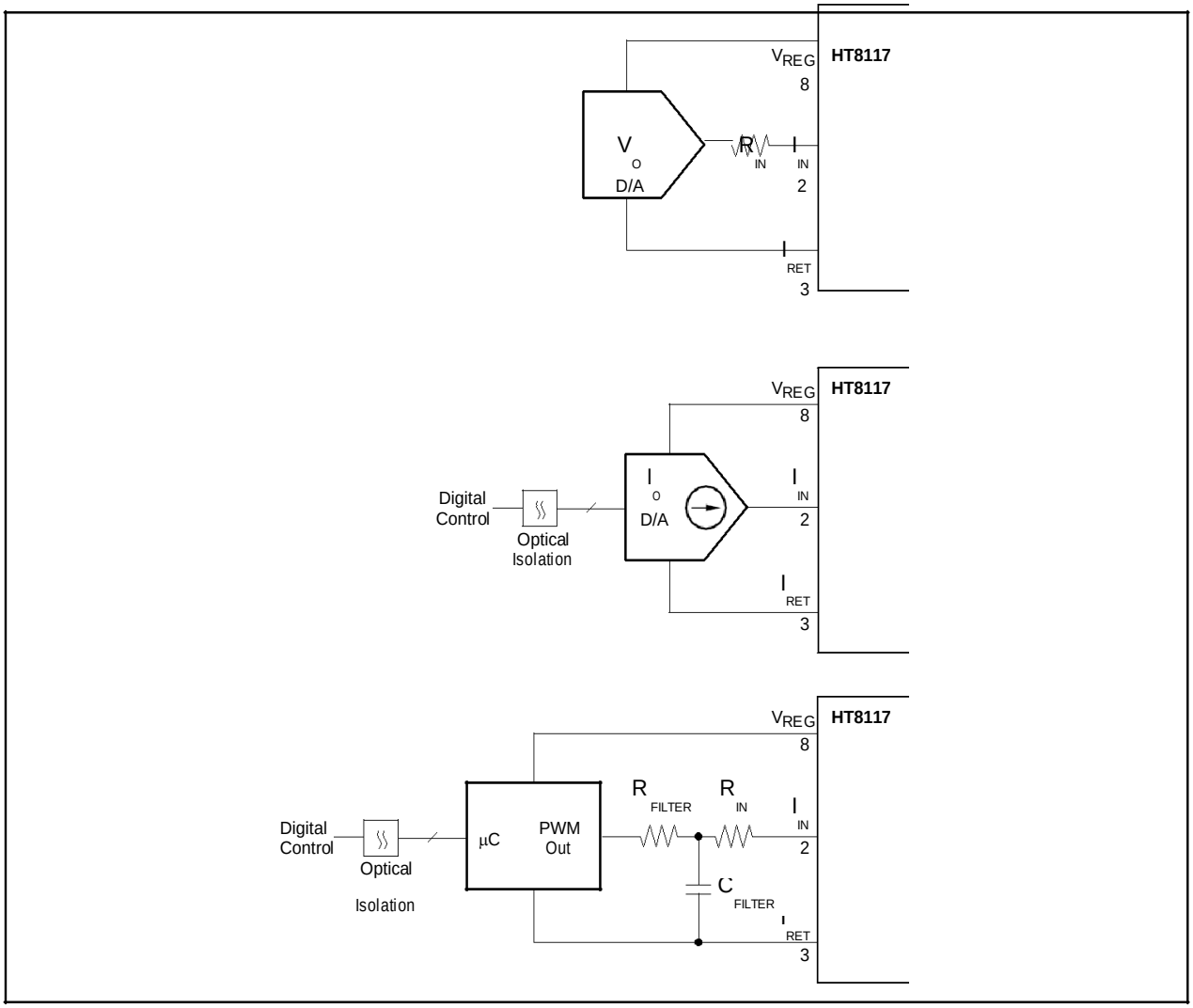


Figure 4. Digital Control Methods

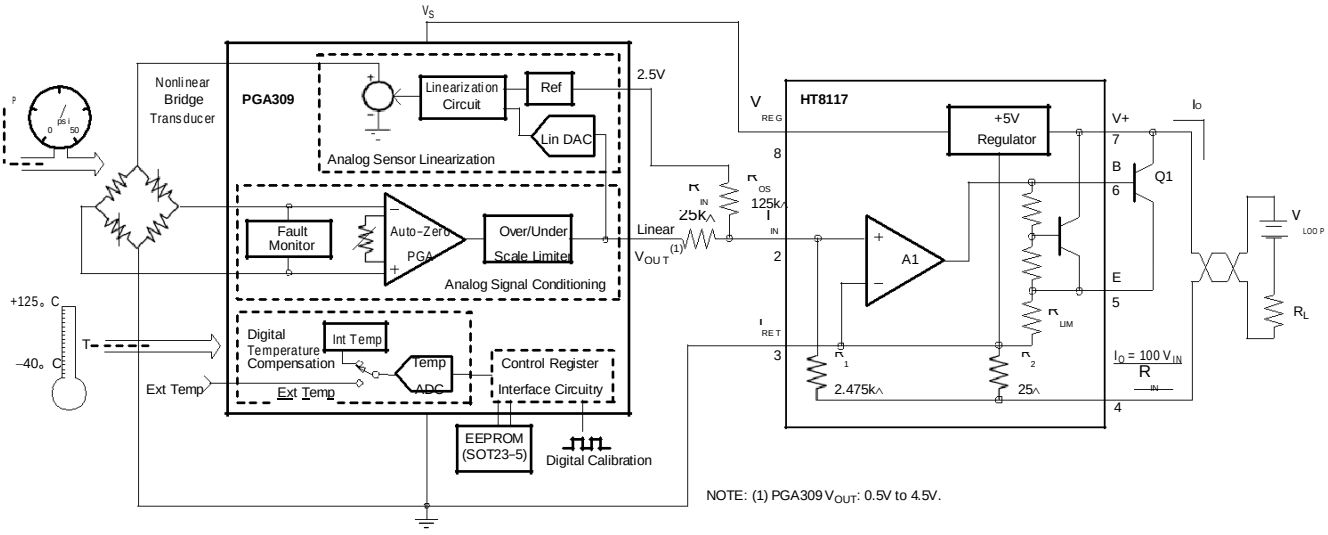


Figure 5. Complete 4-20mA Pressure Transducer Solution with PGA309 and HT8117C

DFN PACKAGE

The HT8117C is offered in a DFN-8 package (also known as SON). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to I_{RET} or left unconnected.

LAYOUT GUIDELINES

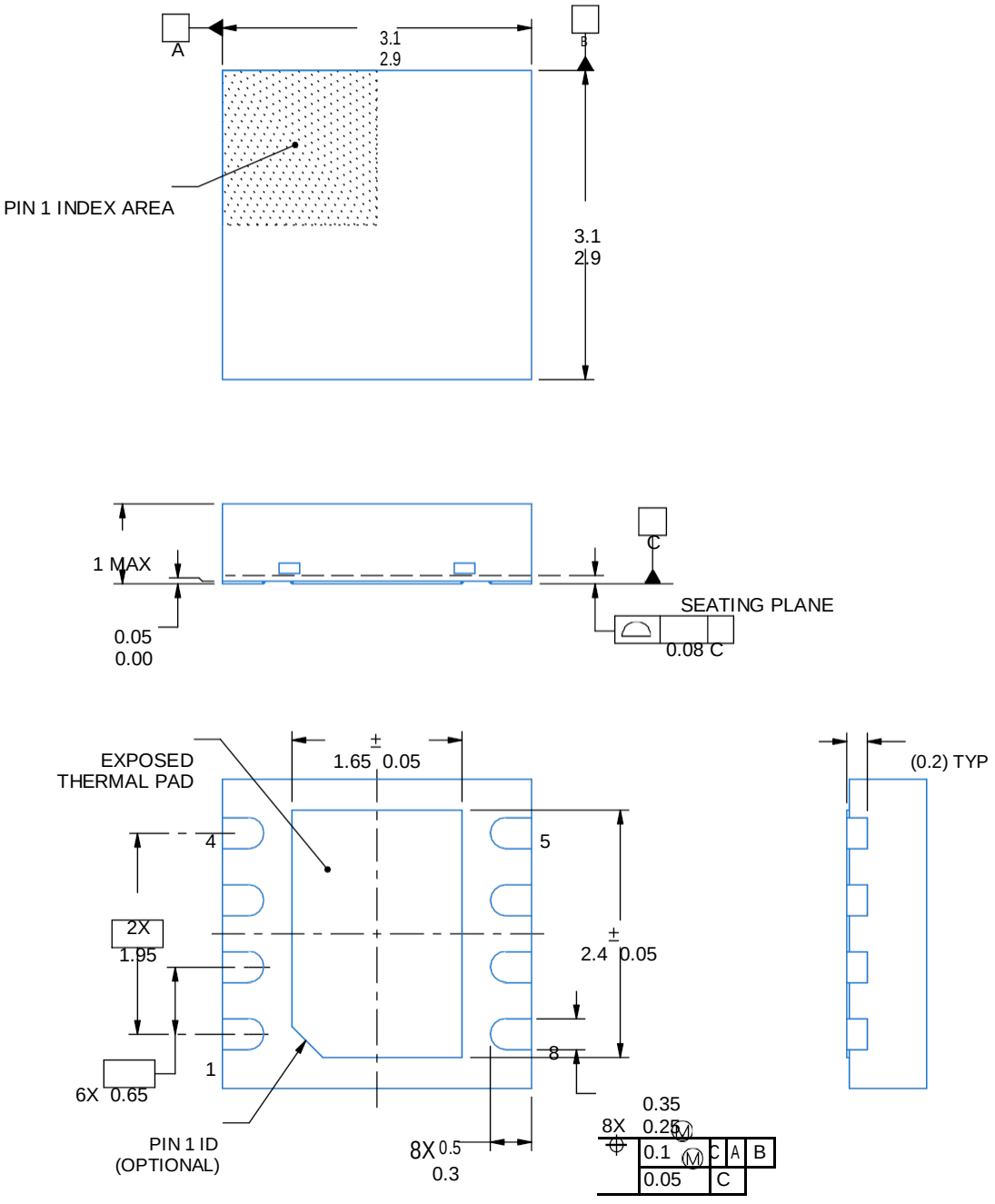
The exposed leadframe die pad on the DFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term stability.

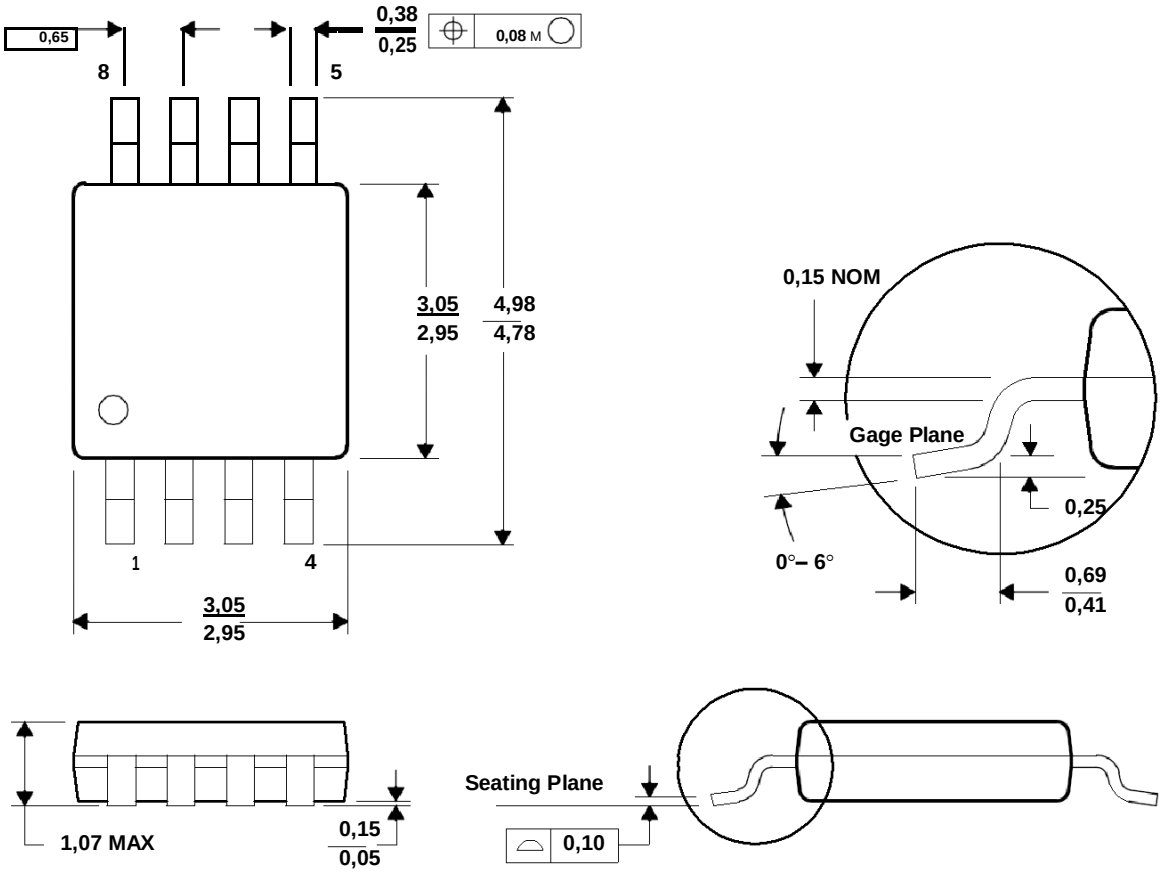
TEST DATA

IQ	VREG	IIN1	IOUT1	IIN2	IOUT2	S
133.76	5037.034	40	4.078	60	6.078	100.0221
135.873	5035.946	40	4.067	60	6.065	99.8977
134.63	5027.991	40	4.083	60	6.09	100.3641
133.262	5032.124	40	4.086	60	6.093	100.3641
136.433	5025.66	40	4.069	60	6.065	99.8356
134.164	5031.13	40	4.066	60	6.062	99.7734
132.267	5023.206	40	4.069	60	6.067	99.8977
119.957	5038.152	40	4.082	60	6.084	100.0843
116.911	5038.432	40	4.079	60	6.082	100.1465
130.278	5034.268	40	4.074	60	6.072	99.8977
133.324	5016.897	40	4.094	60	6.098	100.2398
134.412	5019.601	40	4.077	60	6.083	100.3019
130.371	5022.646	40	4.075	60	6.075	99.991
128.599	5024.386	40	4.082	60	6.08	99.8977
125.553	5022.46	40	4.068	60	6.065	99.8667
128.288	5022.584	40	4.061	60	6.055	99.7112
130.247	5028.333	40	4.067	60	6.067	99.991
133.076	5026.22	40	4.071	60	6.067	99.8356
136.309	5014.132	40	4.089	60	6.088	99.991
120.859	5012.92	40	4.066	60	6.063	99.8356
139.417	5029.203	40	4.079	60	6.077	99.8977
137.21	5022.553	40	4.081	60	6.085	100.1776
132.951	5029.048	40	4.058	60	6.05	99.6179
129.687	5025.288	40	4.073	60	6.074	100.0221
127.418	5039.706	40	4.059	60	6.051	99.6179
125.086	5030.632	40	4.082	60	6.085	100.1776
134.35	5029.855	40	4.059	60	6.055	99.7734
117.905	5022.771	40	4.077	60	6.08	100.1465
137.21	5026.841	40	4.063	60	6.059	99.8356
135.034	5031.378	40	4.058	60	6.053	99.7734
130.962	5015.53	40	4.066	60	6.059	99.6179
126.299	5042.037	40	4.071	60	6.07	99.9599
126.05	5019.663	40	4.063	60	6.059	99.8045
128.102	5036.878	40	4.071	60	6.07	99.9599
138.858	5024.262	40	4.084	60	6.085	100.0221
136.868	5022.864	40	4.08	60	6.08	99.991
134.226	5032.404	40	4.077	60	6.075	99.9288
134.257	5051.98	40	4.081	60	6.08	99.991
129.936	5021.248	40	4.077	60	6.078	100.0843
123.159	5024.853	40	4.069	60	6.064	99.7112

DFN8-3*3


A
B
3.1
2.9
PIN 1 INDEX AREA
3.1
2.9
1 MAX
0.05
0.00
C
SEATING PLANE
0.08 C
EXPOSED
THERMAL PAD
1.65 ± 0.05
4
5
2X
1.95
2.4 ± 0.05
1
8
6X 0.65
PIN 1 ID
(OPTIONAL)
8X 0.5
0.3
0.35
8X 0.25
0.1 M C A B
0.05 C
(0.2) TYP

MSOP8


0,65
8
5
0,38
0,25
0,08 M
3,05
2,95
4,98
4,78
1
4
3,05
2,95
0,15 NOM
Gage Plane
0,25
0°– 6°
0,69
0,41
1,07 MAX
0,15
0,05
Seating Plane
0,10