

## FEATURES

**14  $\Omega$  (maximum) on resistance**  
**1.4  $\Omega$  (maximum) on-resistance flatness**  
**2.7 V to 5.5 V single supply**  
 **$\pm 2.7$  V to  $\pm 5.5$  V dual supply**  
**Rail-to-rail operation**  
**8-lead SOT-23**  
**Typical power consumption ( $<0.1$   $\mu$ W)**  
**TTL-/CMOS-compatible inputs**  
**Supports defense and aerospace applications**  
**(AQEC standard)**  
**Military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$**   
**Controlled manufacturing baseline**  
**One assembly and test site**  
**One fabrication site**  
**Enhanced product change notification**  
**Qualification data available on request**

## APPLICATIONS

**Automatic test equipment**  
**Power routing**  
**Communication systems**  
**Data acquisition systems**  
**Sample-and-hold systems**  
**Avionics**  
**Relay replacement**  
**Battery-powered systems**

## GENERAL DESCRIPTION

The ADG619-EP is a monolithic, CMOS single-pole double-throw (SPDT) switch.

The ADG619-EP offers a low on resistance of 4  $\Omega$ , which is matched to within 0.7  $\Omega$  between channels. These switches also provide low power dissipation, yet result in high switching speeds. The ADG619-EP exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

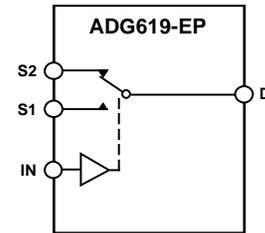
The ADG619-EP is available in an 8-lead SOT-23 package.

Additional application and technical information can be found in the [ADG619](#) data sheet.

### Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## FUNCTIONAL BLOCK DIAGRAM



**NOTES**  
**1. SWITCHES SHOWN FOR**  
**A LOGIC 1 INPUT.**

08844-001

Figure 1.

## PRODUCT HIGHLIGHTS

1. Low on resistance ( $R_{ON}$ ): 4  $\Omega$  typical.
2. Dual  $\pm 2.7$  V to  $\pm 5.5$  V or single 2.7 V to 5.5 V supplies.
3. Low power dissipation.
4. Fast  $t_{ON}/t_{OFF}$ .
5. Tiny, 8-lead SOT-23 package.

## TABLE OF CONTENTS

Features .....	1	Single Supply .....	4
Applications.....	1	Absolute Maximum Ratings .....	5
Functional Block Diagram .....	1	ESD Caution.....	5
General Description .....	1	Pin Configurations and Function Descriptions .....	6
Product Highlights .....	1	Typical Performance Characteristics .....	7
Revision History .....	2	Test Circuits.....	8
Specifications.....	3	Outline Dimensions .....	10
Dual Supply .....	3	Ordering Guide .....	10

## REVISION HISTORY

11/10—Revision 0: Initial Version

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

**Table 1.**

Parameter	+25°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>				
Analog Signal Range		$V_{SS}$ to $V_{DD}$	V	$V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$
On Resistance ( $R_{ON}$ )	4		$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_{DS} = -10\text{ mA}$ ; see Figure 9
	6.5	10	$\Omega$ max	
$R_{ON}$ Match Between Channels ( $\Delta R_{ON}$ )	0.7		$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_{DS} = -10\text{ mA}$
	1.1	1.45	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.7		$\Omega$ typ	$V_S = \pm 3.3\text{ V}$ , $I_{DS} = -10\text{ mA}$
	1.35	1.6	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$		nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
	$\pm 0.25$	$\pm 3$	nA max	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ ; see Figure 10
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.01$		nA typ	$V_S = V_D = \pm 4.5\text{ V}$ ; see Figure 11
	$\pm 0.25$	$\pm 25$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{ON}$	80		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	120	215	ns max	$V_S = 3.3\text{ V}$ ; see Figure 12
$t_{OFF}$	45		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	75	105	ns max	$V_S = 3.3\text{ V}$ ; see Figure 12
Break-Before-Make Time Delay, $t_{BBM}$	40		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 3.3\text{ V}$ ; see Figure 13
Charge Injection	110		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 14
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 15
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 16
Bandwidth -3 dB	190		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 17
$C_S$ (Off)	25		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (On)	95		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
		1.0	$\mu\text{A}$ max	Digital inputs = 0 V or 5.5 V
$I_{SS}$	0.001		$\mu\text{A}$ typ	Digital inputs = 0 V or 5.5 V
		1.0	$\mu\text{A}$ max	

<sup>1</sup> Guaranteed by design, not subject to production test.

# ADG619-EP

## SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ . All specifications  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , unless otherwise noted.

Table 2.

Parameter	+25°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	$V_{DD} = 4.5\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance ( $R_{ON}$ )	7	14	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $4.5\text{ V}$ , $I_{DS} = -10\text{ mA}$ ; see Figure 9
$R_{ON}$ Match Between Channels ( $\Delta R_{ON}$ )	0.8	1.4	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $4.5\text{ V}$ , $I_{DS} = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5	1.4	$\Omega$ typ $\Omega$ max	$V_S = 1.5\text{ V}$ to $3.3\text{ V}$ , $I_{DS} = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source Off Leakage, $I_S$ (Off)	$\pm 0.01$		nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ ; see Figure 10
Channel On Leakage, $I_{Dv}$ , $I_S$ (On)	$\pm 0.25$ $\pm 0.01$ $\pm 0.25$	$\pm 3$  $\pm 25$	nA max nA typ nA max	$V_S = V_D = 1\text{ V}/4.5\text{ V}$ ; see Figure 11
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
Digital Input Capacitance, $C_{IN}$	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{ON}$	120		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	220	390	ns max	$V_S = 3.3\text{ V}$ ; see Figure 12
$t_{OFF}$	50		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	75	135	ns max	$V_S = 3.3\text{ V}$ ; see Figure 12
Break-Before-Make Time Delay, $t_{BBM}$	70		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		10	ns min	$V_{S1} = V_{S2} = 3.3\text{ V}$ ; see Figure 13
Charge Injection	6		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 14
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 15
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 16
Bandwidth -3 dB	190		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 17
$C_S$ (OFF)	25		pF typ	$f = 1\text{ MHz}$
$C_{Dv}$ , $C_S$ (ON)	95		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$
		1.0	$\mu\text{A}$ max	Digital inputs = 0 V or 5.5 V

<sup>1</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	13 V
$V_{DD}$ to GND	-0.3 V to +6.5 V
$V_{SS}$ to GND	+0.3 V to -6.5 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Digital Inputs <sup>1</sup>	-0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA (whichever occurs first)
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	50 mA
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Thermal impedance	
$\theta_{JA}$	229.6°C/W
$\theta_{JC}$	91.99°C/W
Lead Soldering	
Reflow, Peak Temperature	260(+0/-5)°C
Time at Peak Temperature	20 sec to 40 sec

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at a time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG619-EP

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

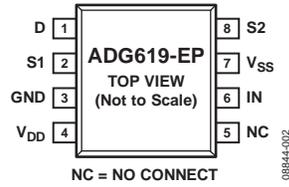


Figure 2. 8-Lead SOT-23 (RJ-8)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. Can be an input or output.
2	S1	Source Terminal. Can be an input or output.
3	GND	Ground (0 V) Reference.
4	V <sub>DD</sub>	Most Positive Power Supply.
5	NC	No Connect. Not internally connected.
6	IN	Logic Control Input.
7	V <sub>SS</sub>	Most Negative Power Supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
8	S2	Source Terminal. Can be an input or output.

Table 5. Truth Table for the ADG619-EP

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

# TYPICAL PERFORMANCE CHARACTERISTICS

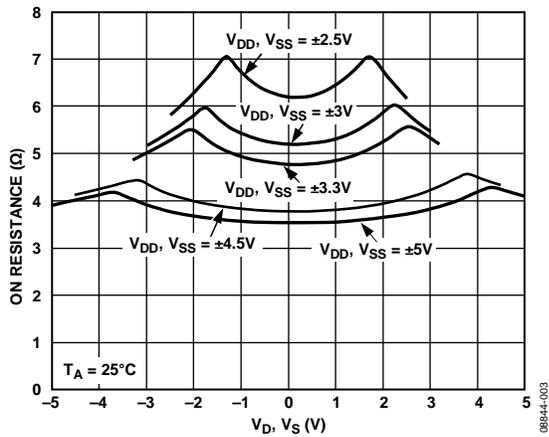


Figure 3. On Resistance vs.  $V_D, V_S$  (Dual Supply)

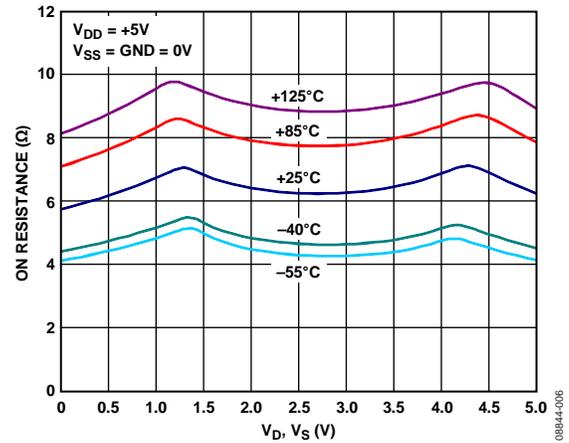


Figure 6. On Resistance vs.  $V_D, V_S$  for Different Temperatures (Single Supply)

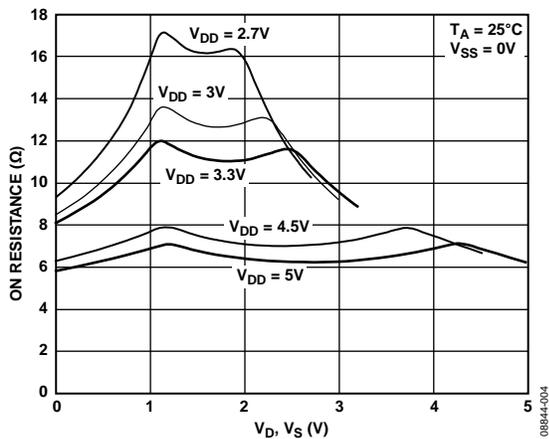


Figure 4. On Resistance vs.  $V_D, V_S$  (Single Supply)

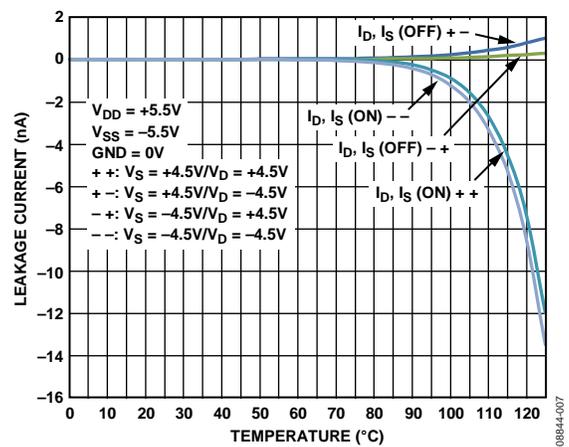


Figure 7. Leakage Currents vs. Temperature (Dual Supply)

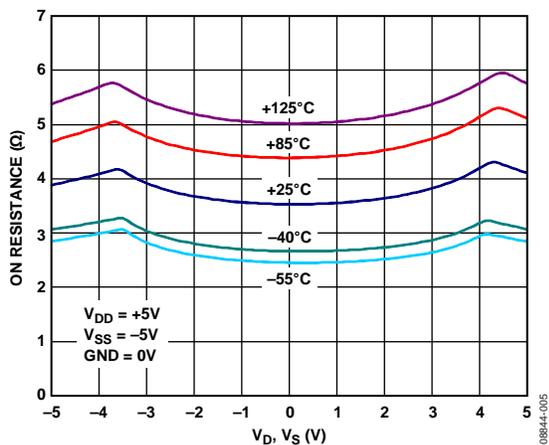


Figure 5. On Resistance vs.  $V_D, V_S$  for Different Temperatures (Dual Supply)

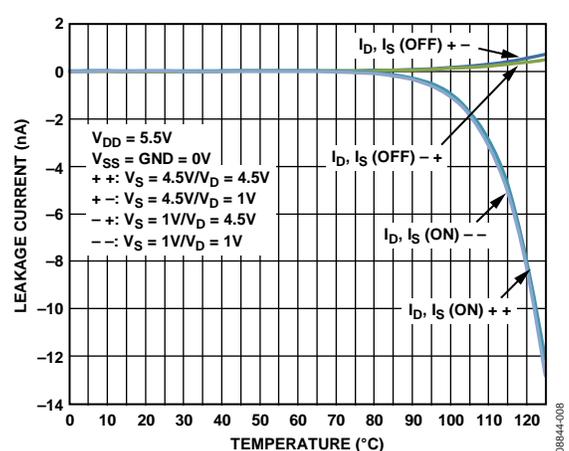


Figure 8. Leakage Currents vs. Temperature (Single Supply)

## TEST CIRCUITS

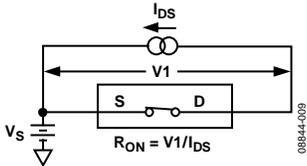


Figure 9. On Resistance

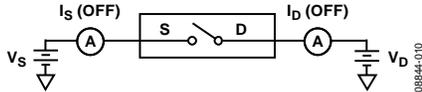


Figure 10. Off Leakage

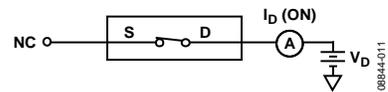


Figure 11. On Leakage

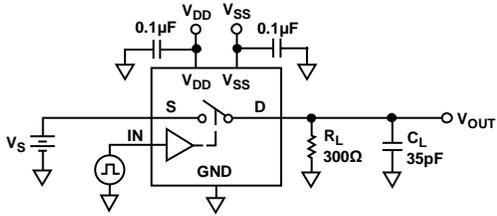


Figure 12. Switching Times

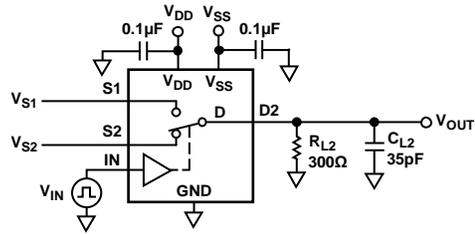
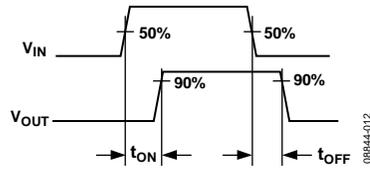


Figure 13. Break-Before-Make Time Delay,  $t_{BBM}$

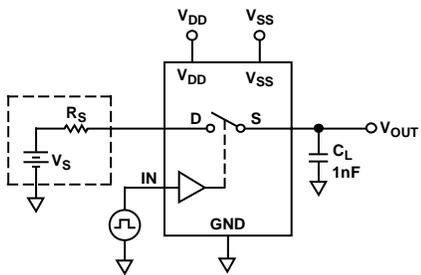
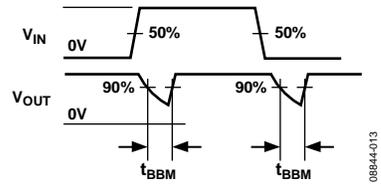
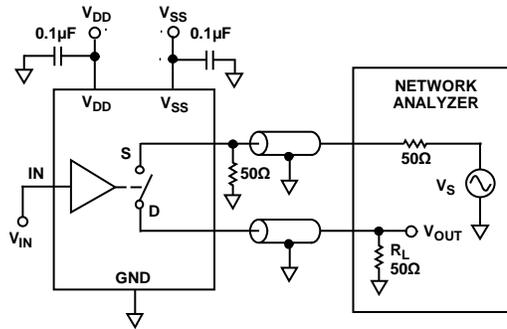
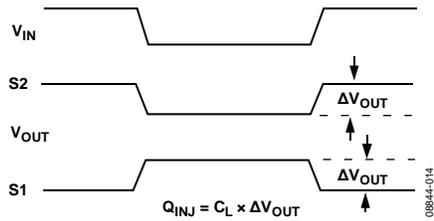
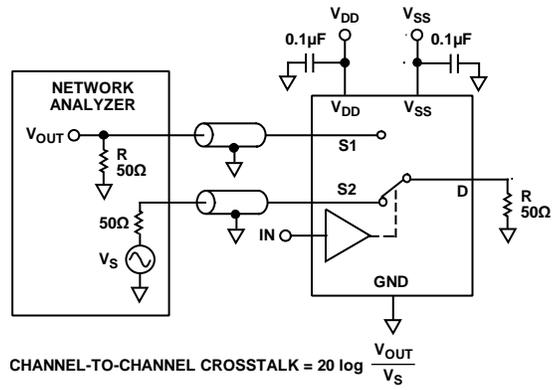


Figure 14. Charge Injection



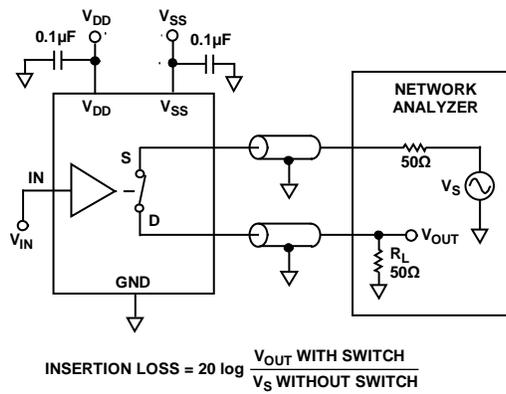
$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 15. Off Isolation



08844-016

Figure 16. Channel-to-Channel Crosstalk

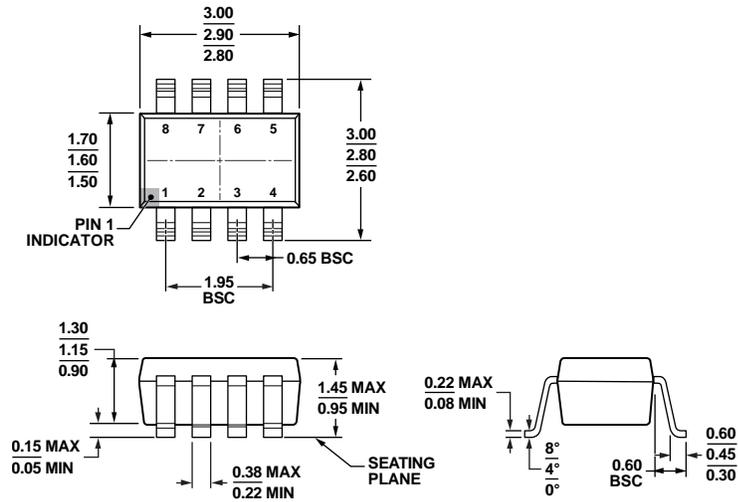


08844-017

Figure 17. Bandwidth

# ADG619-EP

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 18. 8-Lead Small Outline Transistor Package [SOT-23] (RJ-8)

Dimensions shown in millimeters

121608-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding <sup>2</sup>
ADG619SRJZ-EP-RL7	-55°C to +125°C	8-Lead Small Outline Transistor Package [SOT-23]	RJ-8	S3V

<sup>1</sup> Z =RoHS Compliant Part.

<sup>2</sup> Branding on SOT-23 packages is limited to three characters due to space constraints

**NOTES**

**NOTES**