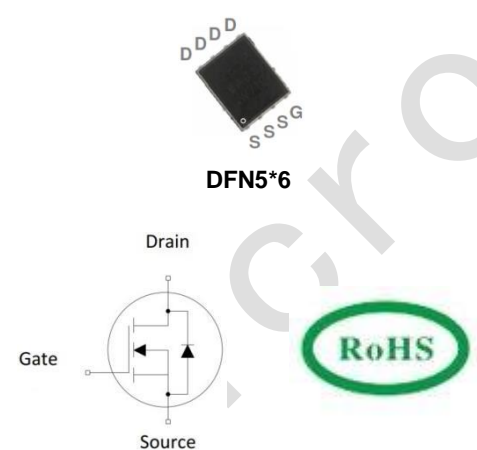


N-channel 80V, 52A, 10mΩ Super-Junction Power MOSFET

<p>Description</p> <p>This power MOSFET is designed with split gate trench technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.</p> <p>Features</p> <ul style="list-style-type: none"> ◆ Very low FOM $R_{DS(on)} \times Q_g$ ◆ 100% UIS tested ◆ RoHS compliant <p>Applications</p> <ul style="list-style-type: none"> ◆ Motor Drivers. ◆ DC-DC Converter. ◆ Uninterrupted power supply (UPS). 	<p>Product Summary</p> <table> <tr> <td>$V_{DS} @ T_{j,25^\circ C}$</td> <td>80V</td> </tr> <tr> <td>$R_{DS(on),max}$</td> <td>10mΩ</td> </tr> <tr> <td>I_D</td> <td>52A</td> </tr> </table> <div style="text-align: center;">  <p>DFN5*6</p> <p>RoHS</p> <p>N-Channel MOSFET</p> </div>	$V_{DS} @ T_{j,25^\circ C}$	80V	$R_{DS(on),max}$	10mΩ	I_D	52A
$V_{DS} @ T_{j,25^\circ C}$	80V						
$R_{DS(on),max}$	10mΩ						
I_D	52A						

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	80	V
Continuous drain current ($T_C = 25^\circ C$)	I_D	52	A
($T_C = 100^\circ C$)		35	A
Pulsed drain current ¹⁾	I_{DM}	208	A
Gate-Source voltage	V_{GSS}	± 20	V
Avalanche energy, single pulse ²⁾	E_{AS}	180	mJ
Power Dissipation DFN5*6 ($T_C = 25^\circ C$)	P_D	56	W
- Derate above 25°C		0.82	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	52	A
Diode pulse current	$I_{S,pulse}$	208	A

Thermal Characteristics DFN5*6

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.73	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	49	$^{\circ}C/W$
Soldering temperature, wave soldering only allowed at leads. (1.6mm from case for 10s)	T_{sold}	260	$^{\circ}C$

Electrical Characteristics $T_c = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
Drain cut-off current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V,$ $T_j = 25^{\circ}C$ $T_j = 125^{\circ}C$	-	-	1	μA
			-	10	-	
Gate leakage current, Forward	I_{GSSF}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	$V_{GS}=-20V, V_{DS}=0V$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=35A$ $T_j = 25^{\circ}C$	-	10.6	13.5	$m\Omega$
			-		-	
Dynamic characteristics						
Input capacitance	C_{iss}	$V_{DS} = 50V, V_{GS} = 0V,$	-	1590	-	pF
Output capacitance	C_{oss}	$f = 1MHz$	-	580	-	
Reverse transfer capacitance	C_{rss}		-	5.5	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 35A$	-	15	-	ns
Rise time	t_r	$R_G = 25\Omega, V_{GS}=10V$	-	40	-	
Turn-off delay time	$t_{d(off)}$		-	120	-	
Fall time	t_f		-	80	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	$V_{DD}=80V, I_D=35A,$	-	6.4	-	nC
Gate to drain charge	Q_{gd}	$V_{GS}=0$ to 10 V	-	3.2	-	
Gate charge total	Q_g		-	26	-	
Gate plateau voltage	$V_{plateau}$		-	2.5	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=35A$	-	0.9	-	V
Reverse recovery time	t_{rr}	$V_R=50V, I_F=35A,$	-	68	-	ns
Reverse recovery charge	Q_{rr}	$dI_F/dt=100A/\mu s$	-	95	-	nC

Notes:

- Limited by maximum junction temperature, maximum duty cycle is 0.75.
- $I_{AS} = 20A, V_{DD} = 50V, \text{Starting } T_j = 25^{\circ}C.$
- Repetitive Rating: Pulse width limited by maximum junction temperature.

Electrical Characteristics Diagrams

Figure 1. Output Characteristics

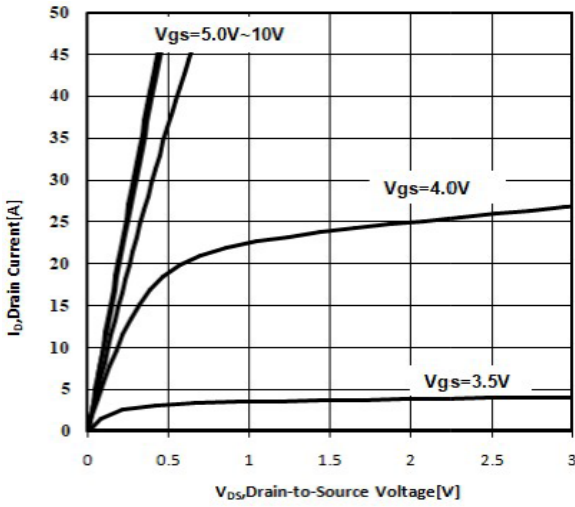


Figure 2. Transfer Characteristics

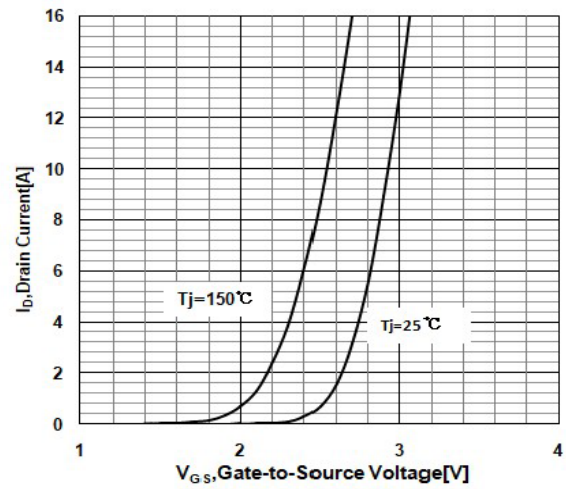


Figure 3. On-Resistance vs. Drain Current

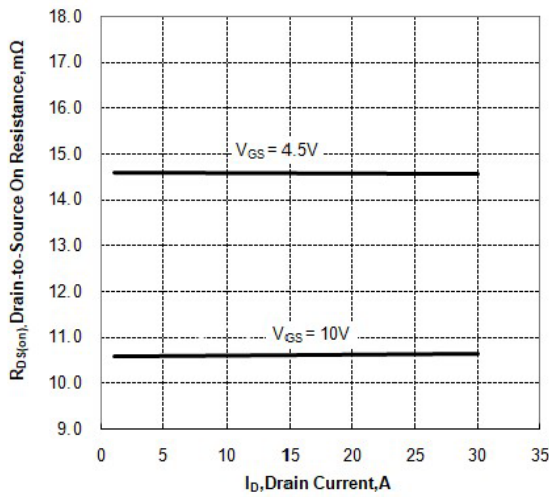


Figure 4. Capacitance Characteristics

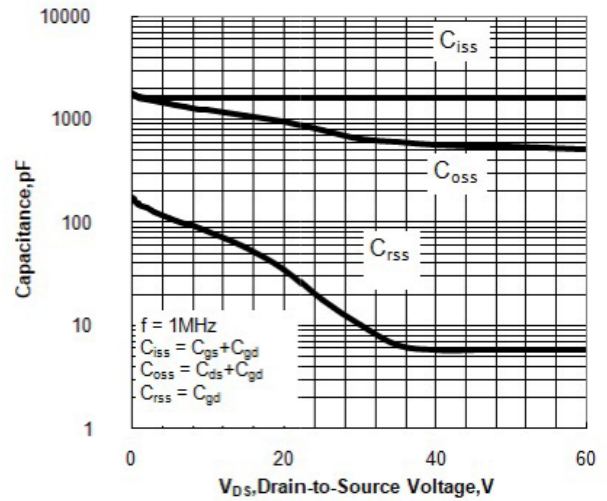


Figure 5. Gate Charge Characteristics

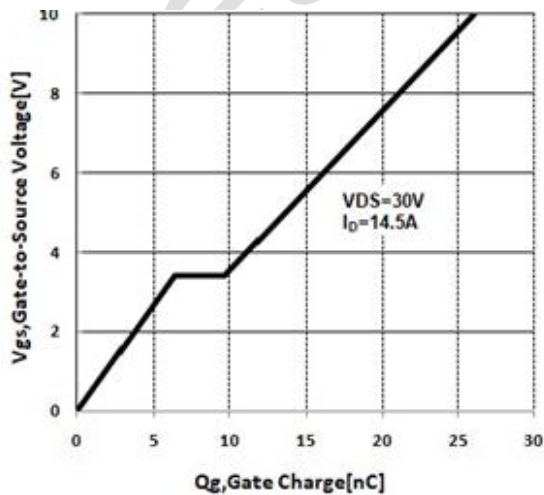


Figure 6. Body Diode Forward Voltage

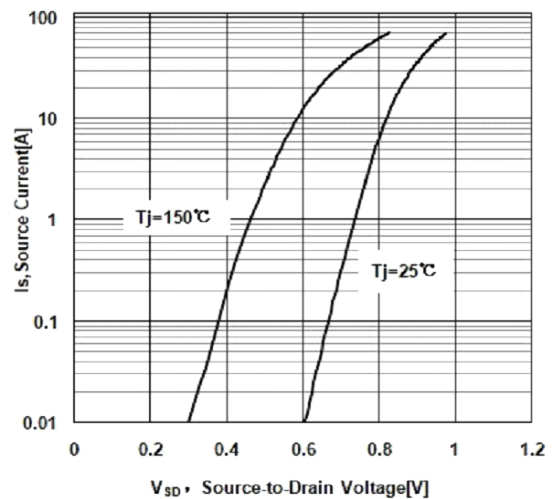


Figure 7. Breakdown Voltage vs. Temperature

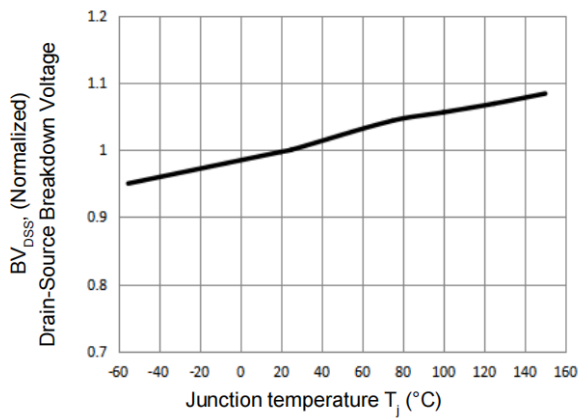


Figure 8. On-Resistance vs. Temperature

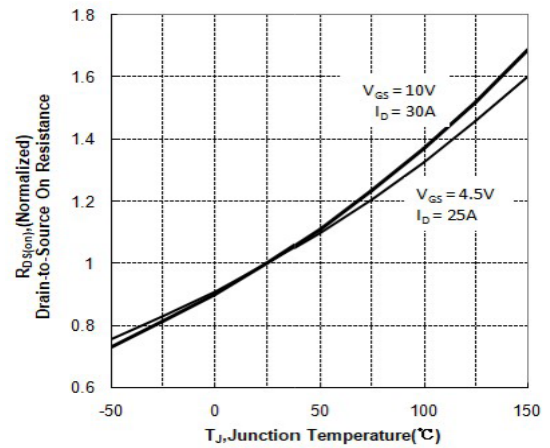


Figure 9. Transient Thermal Impedance

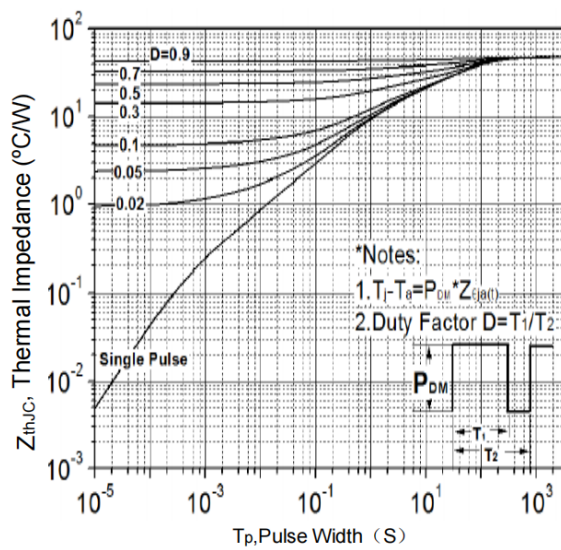
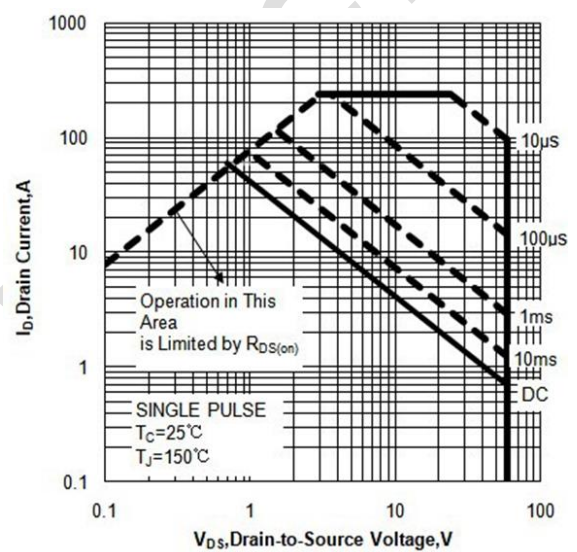
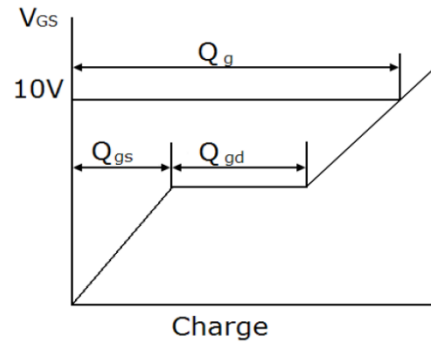
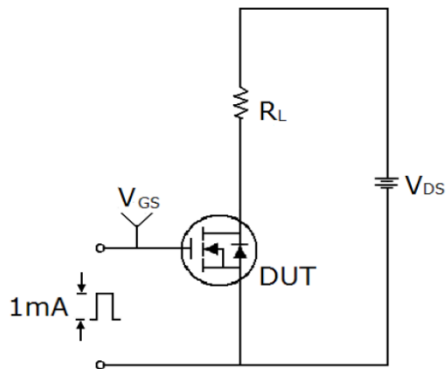


Figure 10. Maximum Safe Operating Area

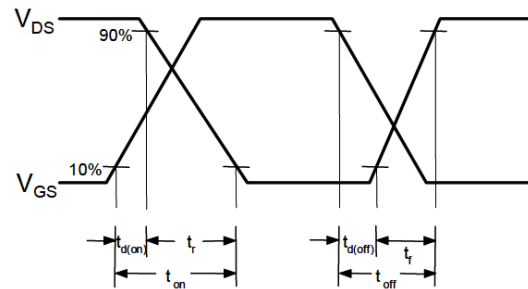
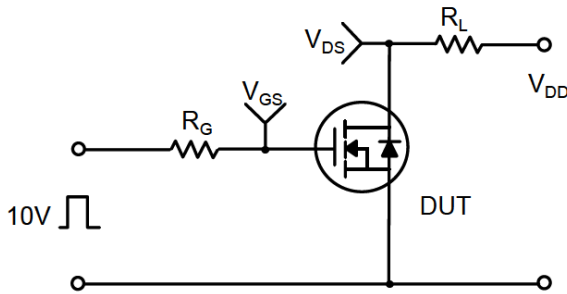


Test Circuits

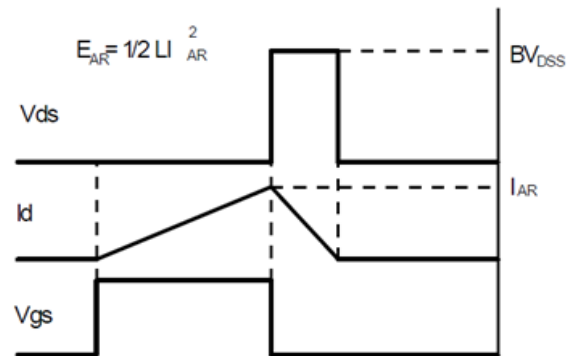
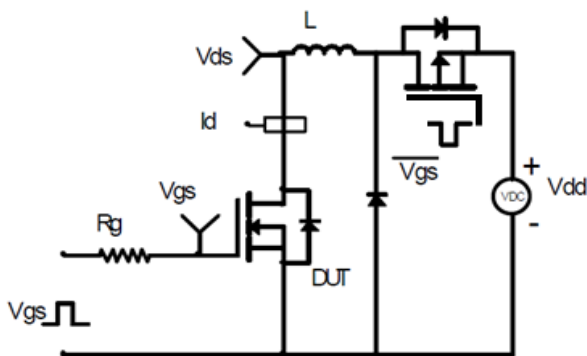
Gate Charge Test Circuit & Waveform



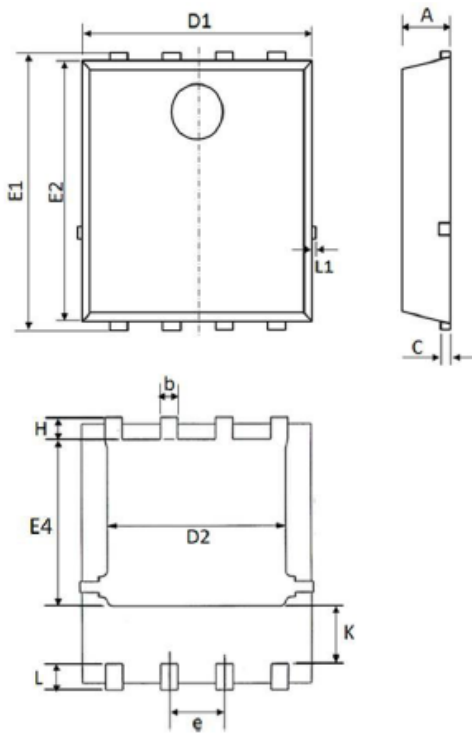
Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



Mechanical Dimensions for DFN5*6



COMMON DIMENSIONS						
SYMBOL	MILLIMETERS			INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1	1.1	1.2	0.039	0.043	0.047
b	0.3	0.4	0.5	0.012	0.016	0.020
C	0.154	0.254	0.354	0.006	0.010	0.014
D1	5	5.2	5.4	0.197	0.205	0.213
D2	3.8	4.1	4.25	0.150	0.161	0.167
E1	5.95	6.15	6.35	0.234	0.242	0.250
E2	5.66	5.86	6.06	0.223	0.231	0.239
E4	3.52	3.72	3.92	0.139	0.146	0.154
e	1.27 BSC			0.050 BSC		
H	0.4	0.5	0.6	0.016	0.020	0.024
L	0.5	0.6	0.7	0.020	0.024	0.028
L1	-	-	0.12	-	-	0.005
K	1.14	1.29	1.44	0.045	0.051	0.057

Reactor