

30V Dual P-Channel Enhancement Mode MOSFET

Description

The NP4953C uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.

General Features

- ◆ $V_{DS} = -30V$, $I_D = -5.5A$
 $R_{DS(ON)}(Typ.) = 50m\Omega$ @ $V_{GS} = -4.5V$
 $R_{DS(ON)}(Typ.) = 40m\Omega$ @ $V_{GS} = -10V$
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

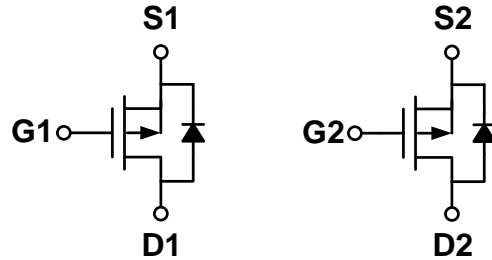
Application

- ◆ PWM applications
- ◆ Load switch

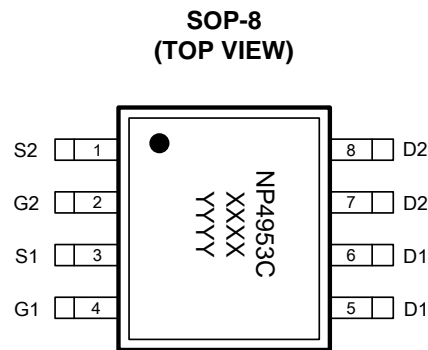
Package

- ◆ SOP-8

Schematic diagram



Marking and pin assignment



Note: XXXX is the date code, YYYY is the wafer lot number.

Ordering Information

Part Number	Storage Temperature	Package	Devices Per Reel
NP4953CSR	-55°C to +150°C	SOP-8	3000

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

parameter	symbol	limit	unit	
Drain-source voltage	V_{DS}	-30	V	
Gate-source voltage	V_{GS}	±20	V	
Drain Current-Continuous (Silicon Limited)	I_D	$T_A = 25^\circ C$	-5.5	A
		$T_A = 75^\circ C$	-4	A
Pulsed Drain Current (Package Limited)	I_{DM}	-22	A	
Maximum power dissipation	P_D	$T_A = 25^\circ C$	1.4	W
		$T_A = 75^\circ C$	1	W
Operating junction Temperature range	T_j	-55—150	°C	

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	1	μA
Gate-body leakage	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
ON Characteristics						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.7	-1.3	-2.0	V
Drain-source on-state resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-5.5A$	-	40	65	m Ω
		$V_{GS}=-4.5V, I_D=-4.5A$	-	50	90	
Forward transconductance	g_{fs}	$V_{GS}=-5V, I_D=-5A$	-	5	-	S
Dynamic Characteristics						
Input capacitance	C_{ISS}	$V_{DS}=-15V, V_{GS}=0V$ $f=1.0MHz$	-	700	-	pF
Output capacitance	C_{OSS}		-	120	-	
Reverse transfer capacitance	C_{RSS}		-	70	-	
Switching Characteristics						
Turn-on delay time	$t_{D(ON)}$	$V_{DD}=-15V$ $I_D=-5.5A$ $V_{GEN}=-10V$ $R_L=10ohm$ $R_{GEN}=-6ohm$	-	9	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{D(OFF)}$		-	28	-	
Fall time	t_f		-	12.5	-	
Total gate charge	Q_g	$V_{DS}=-15V, I_D=-5.5A$ $V_{GS}=-10V$	-	14	-	nC
Gate-source charge	Q_{gs}		-	3.1	-	
Gate-drain charge	Q_{gd}		-	3	-	

Thermal Characteristics

Thermal Resistance junction-to ambient	$R_{th JA}$	100	$^{\circ}C/W$
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Typical Performance Characteristics

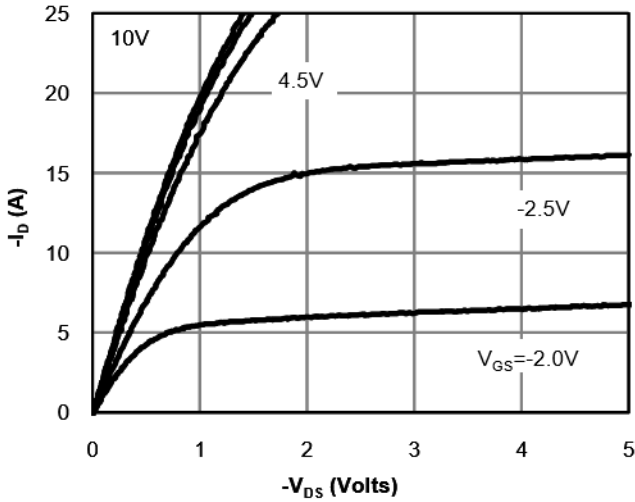


Fig 1: On-Region Characteristics (Note E)

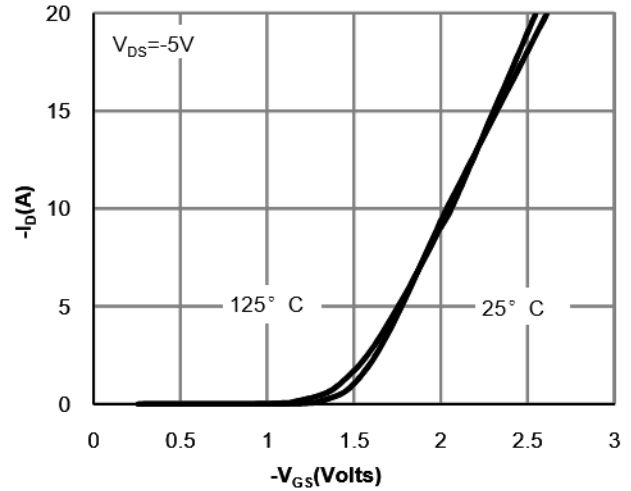


Figure 2: Transfer Characteristics (Note E)

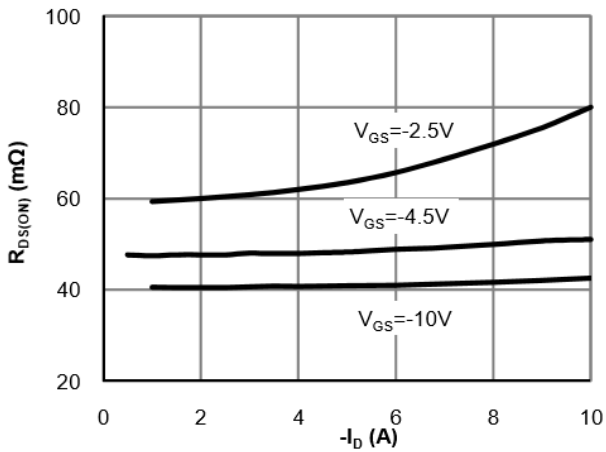


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

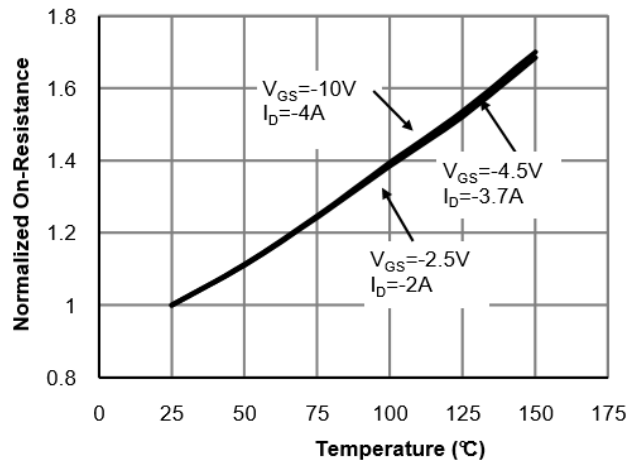


Figure 4: On-Resistance vs. Junction Temperature (Note E)

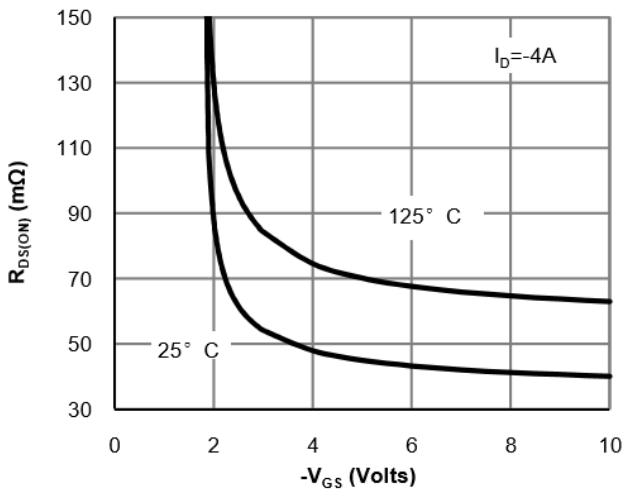


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

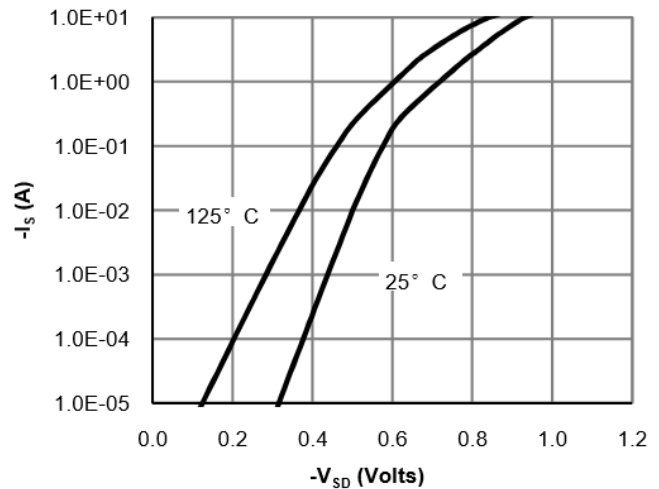


Figure 6: Body-Diode Characteristics (Note E)

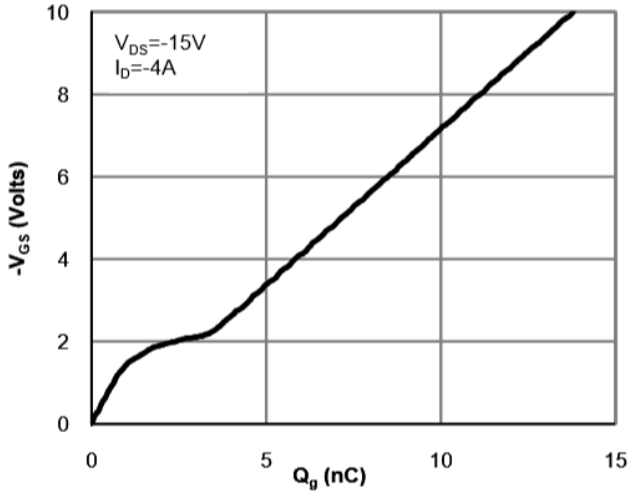


Figure 7: Gate-Charge Characteristics

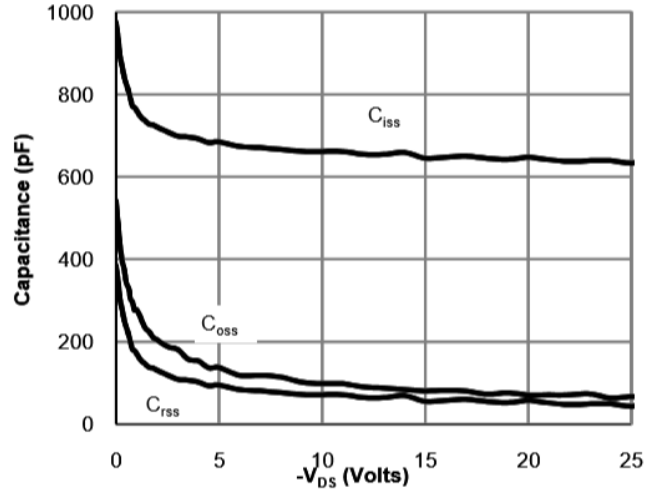


Figure 8: Capacitance Characteristics

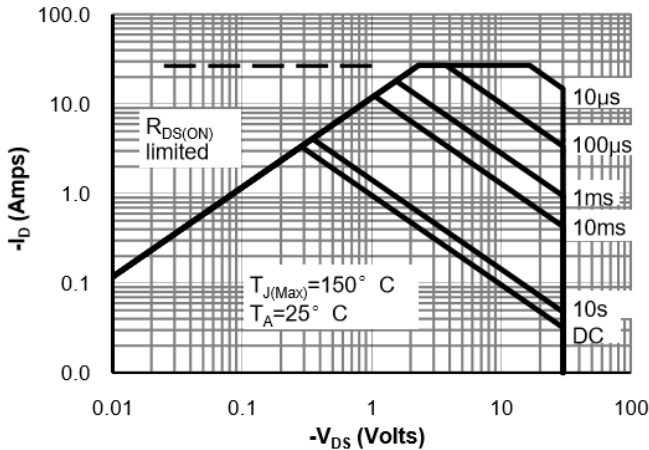


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

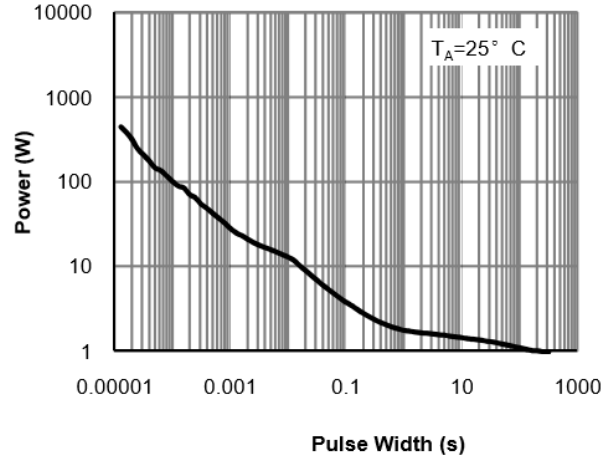


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

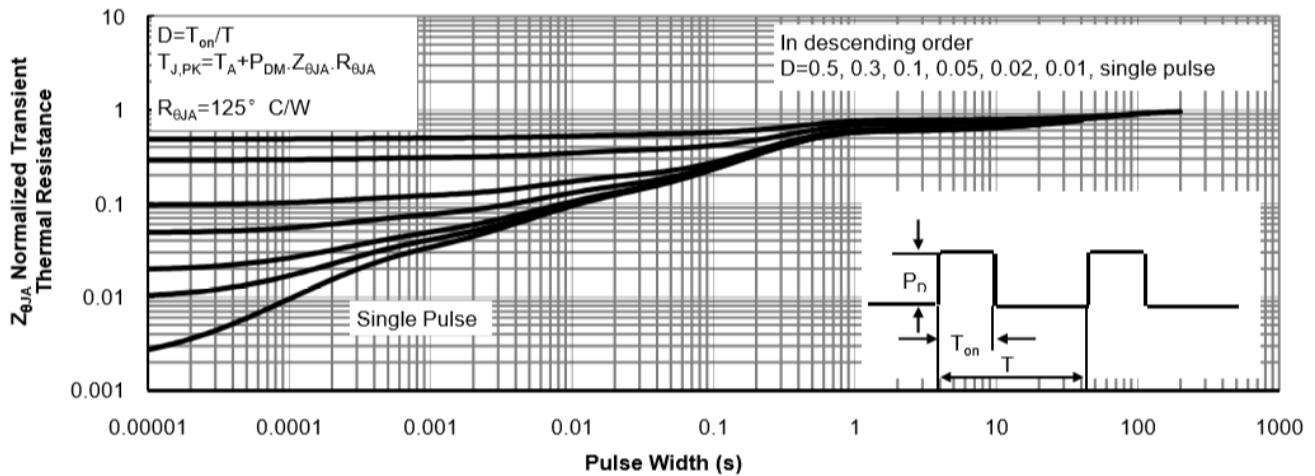
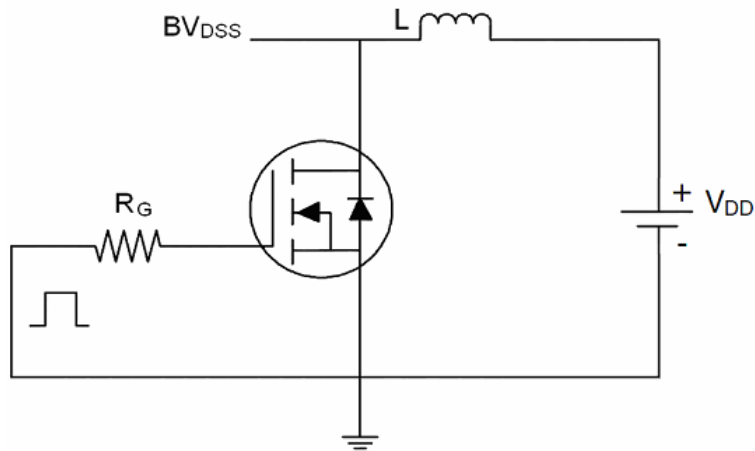


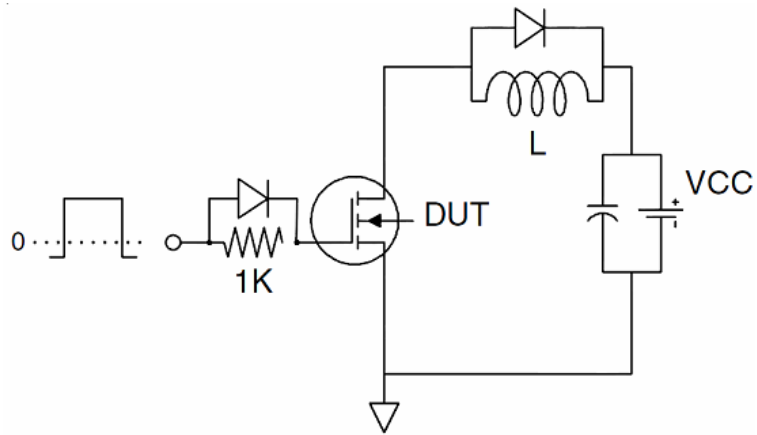
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Test Circuit:

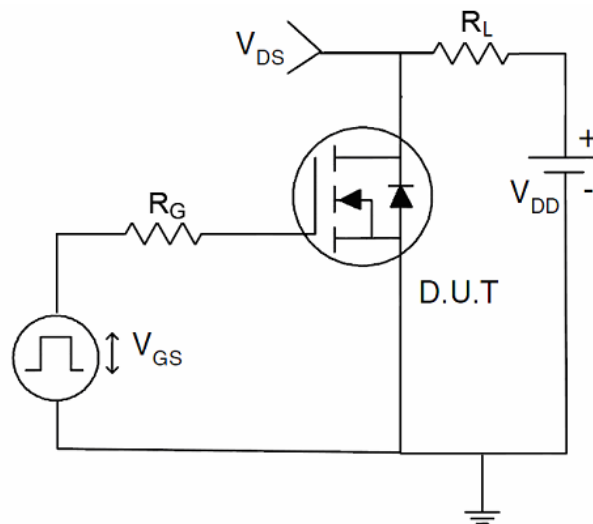
(1)、EAS Test Circuit



(2)、Gate Charge Test Circuit

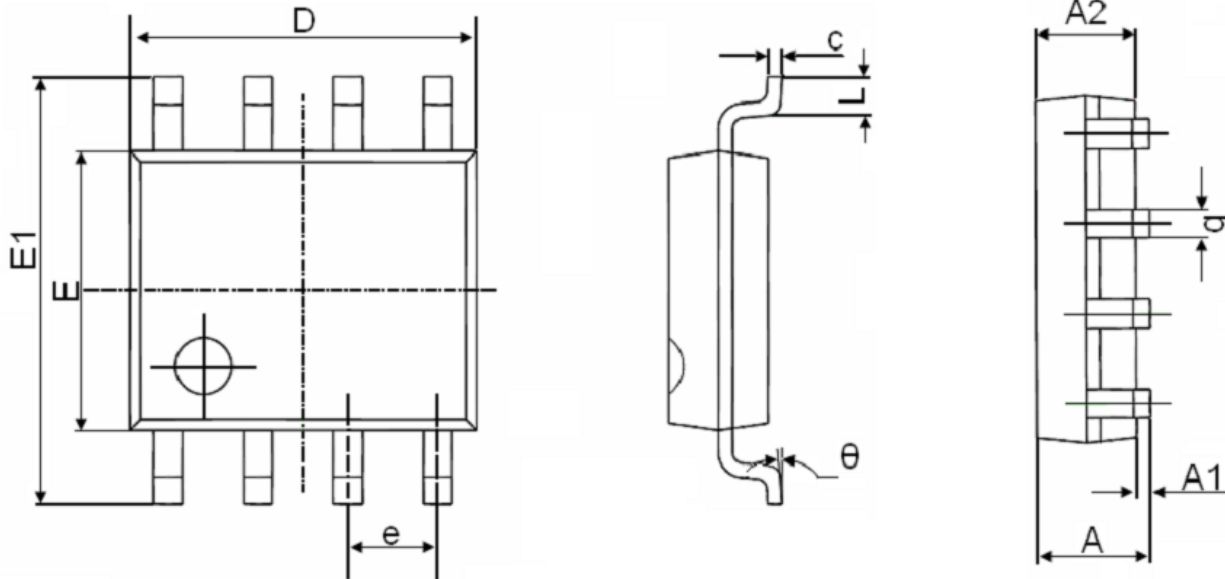


(3)、Switch Time Test Circuit



Package Information

- SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°