MICROCHIP

TN2130

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from Secondary Breakdown
- Low Power Drive Requirement
- Ease of Paralleling
- Low C_{ISS} and Fast Switching Speeds
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and High Gain

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

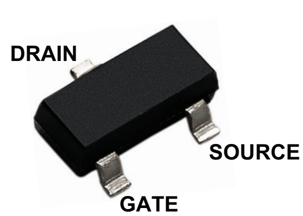
General Description

The TN2130 low-threshold, Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Type

3-lead SOT-23
(Top view)



See Table 3-1 for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage .... BV_{DSS}
Drain-to-Gate Voltage .... BV_{DGS}
Gate-to-Source Voltage .... ±20V
Operating Ambient Temperature, T_A .... –55°C to +150°C
Storage Temperature, T_S .... –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS – COMMERCIAL

Electrical Specifications: $T_A = T_J$ = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	300	—	—	V	V_{GS} = 0V, I_D = 1 mA
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2.4	V	$V_{GS} = V_{DS}$, I_D = 1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	–5.5	mV/°C	$V_{GS} = V_{DS}$, I_D = 1 mA (Note 1)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ± 20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	100	µA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 1)
On-State Drain Current	$I_{D(ON)}$	250	—	—	mA	V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	25	Ω	V_{GS} = 4.5V, I_D = 120 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.1	%/°C	V_{GS} = 4.5V, I_D = 120 mA (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

Electrical Specifications: $T_A = T_J$ = (–55°C, 25°C, and 150°C) unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	**300**	—	—	V	V_{GS} = 0V, I_D = 1 mA
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	**2.4**	V	$V_{GS} = V_{DS}$, I_D = 1 mA
		0.7	—	**2.4**	V	$V_{DS} = V_{GS}$, I_D = 1 mA, T_A = 150°C
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	–3.6	—	mV/°C	$V_{GS} = V_{DS}$, I_D = 1 mA (Note 1)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ± 20V, V_{DS} = 0V
		—	—	**200**	nA	V_{GS} = ± 20V, V_{DS} = 0V, T_A = 150°C

Note 1: Specification is obtained by characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE (CONTINUED)

Electrical Specifications: $T_A = T_J$ = (–55°C, 25°C, and 150°C) unless otherwise specified. All DC parameters are 100% tested at all three temperatures unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle.)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	**100**	µA	V_{GS} = 0V, V_{DS} = Maximum rating, T_A = 150°C
On-State Drain Current	$I_{D(ON)}$	**250**	—	—	mA	V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	25	Ω	V_{GS} = 4.5V, I_D = 120 mA
		—	—	**66**	Ω	V_{GS} = 4.5V, I_D = 120 mA, T_A = 150°C
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	1.1	—	%/°C	V_{GS} = 4.5V, I_D = 120 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS – COMMERCIAL

Electrical Specifications: $T_A = T_J$ = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	—	250	—	mmho	V_{DS} = 25V, I_D = 100 mA
Input Capacitance	C_{ISS}	—	—	50	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	—	15	pF	
Reverse Transfer Capacitance	C_{RSS}	—	—	5	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = 25V, I_D = 120 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	—	7	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	12	ns	
Fall Time	t_f	—	—	15	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS} = 0V, I_{SD} = 120 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	400	—	ns	V_{GS} = 0V, I_{SD} = 120 mA

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

AC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE

Electrical Specifications: T_A = 25°C unless otherwise specified. All AC parameters are sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	—	205	—	mmho	V_{DS} = 25V, I_D = 100 mA
Input Capacitance	C_{ISS}	—	29	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	6	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	1.2	—	pF	

Note 1: 100% Production Tested at $T_A = T_J$ = (–55°C, 25°C, and 150°C).

AC ELECTRICAL CHARACTERISTICS – AUTOMOTIVE (CONTINUED)

Electrical Specifications: T_A = 25°C unless otherwise specified. All AC parameters are sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Turn-On Delay Time	$t_{d(ON)}$	—	6.8	—	ns	V_{DD} = 25V, I_D = 120 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	3	—	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	12	—	ns	
Fall Time	t_f	—	7	—	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	**1.8**	V	V_{GS} = 0V, I_{SD} = 120 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	450	—	ns	V_{GS} = 0V, I_{SD} = 120 mA

Note 1: 100% Production Tested at T_A = T_J = (–55°C, 25°C, and 150°C).

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead SOT-23	θ_{JA}	—	203	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (mA)	Power Dissipation at T_A = 25°C (W)	I_{DR} (Note 1) (mA)	I_{DRM} (mA)
3-lead SOT-23	85	200	0.36	85	200

Note 1: I_D (continuous) is limited by maximum rated T_J.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

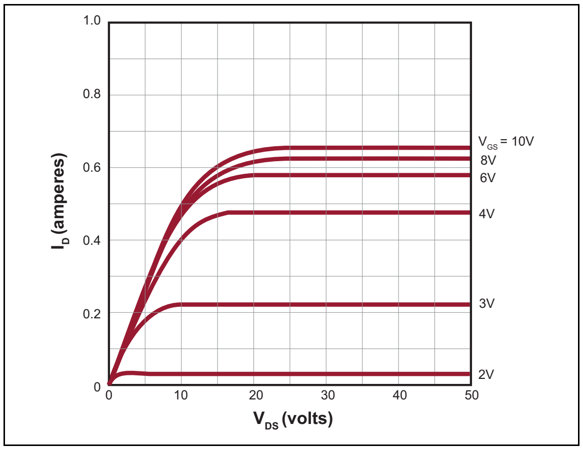


FIGURE 2-1: *Output Characteristics.*

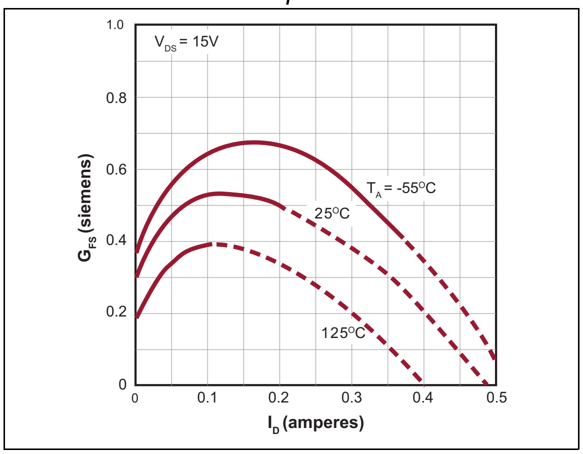


FIGURE 2-2: *Transconductance vs. Drain Current.*

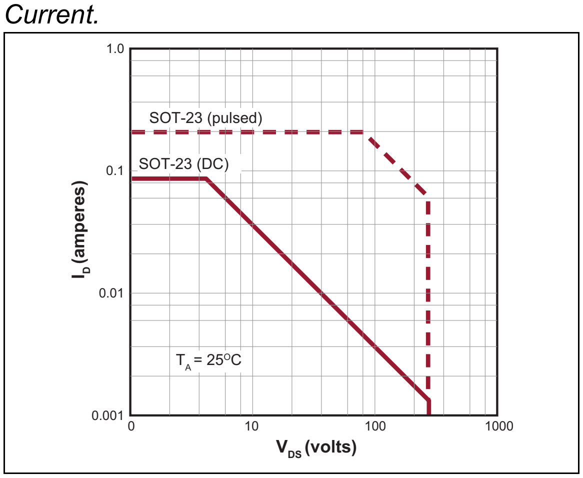


FIGURE 2-3: *Maximum Rated Safe Operating Area.*

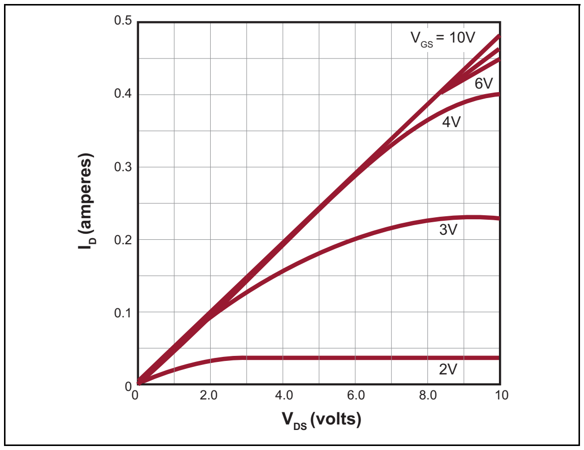


FIGURE 2-4: *Saturation Characteristics.*

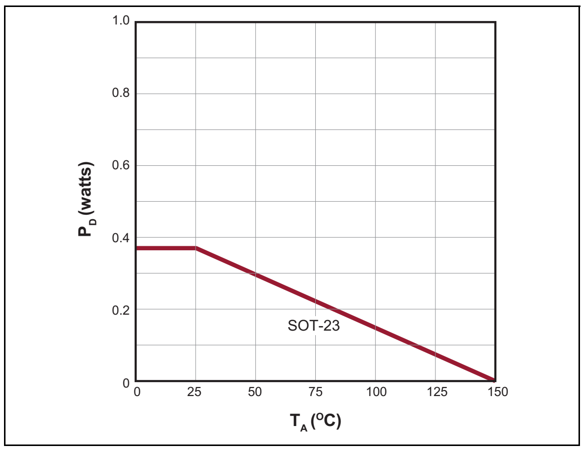


FIGURE 2-5: *Power Dissipation vs. Case Temperature.*

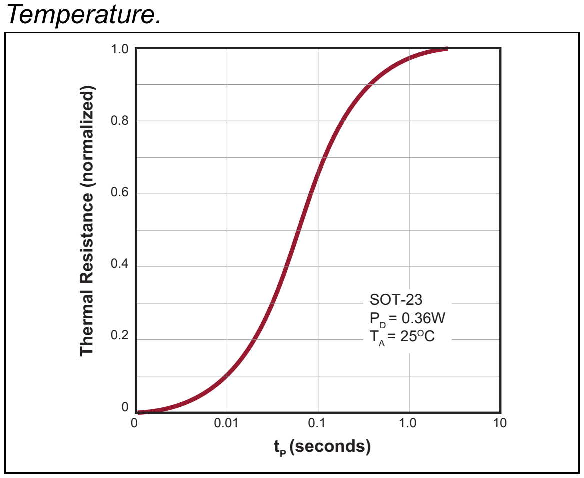


FIGURE 2-6: *Thermal Response Characteristics.*

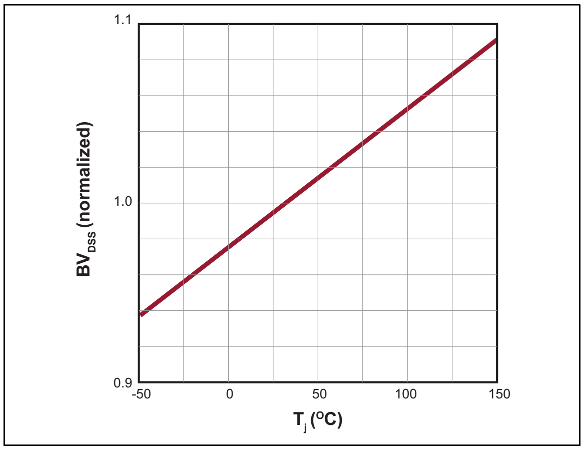


FIGURE 2-7: *BV_{DSS} Variation with Temperature.*

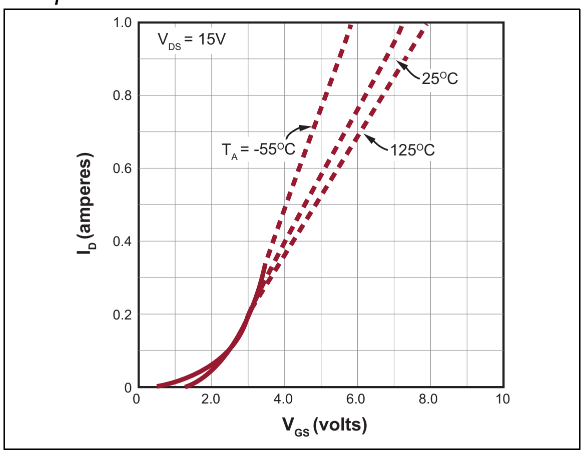


FIGURE 2-8: *Transfer Characteristics.*

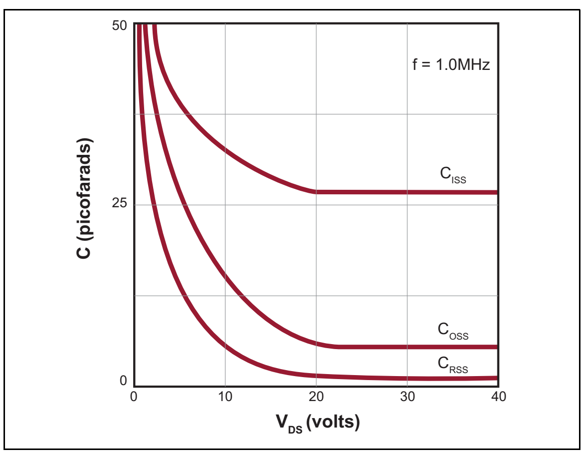


FIGURE 2-9: *Capacitance vs. Drain-to-Source Voltage.*

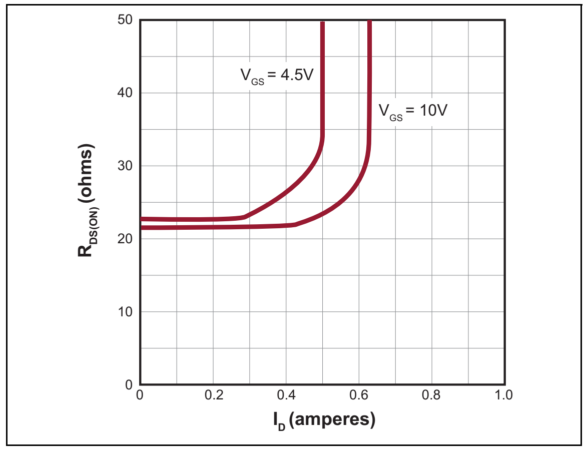


FIGURE 2-10: *On-Resistance vs. Drain Current.*

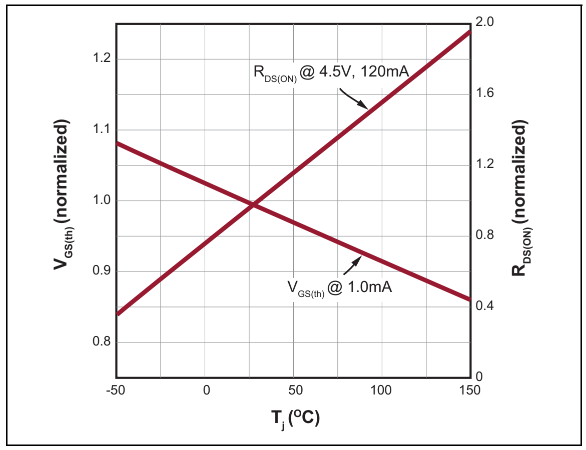


FIGURE 2-11: *$V_{GS(th)}$ and R_{DS} Variation with Temperature.*

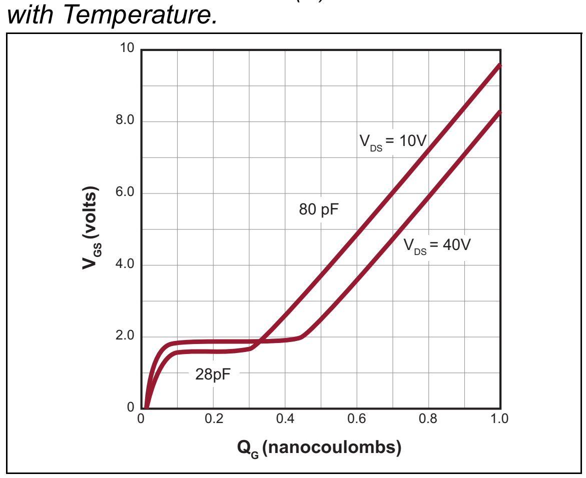


FIGURE 2-12: *Gate Drive Dynamic Characteristics.*

3.0 PIN DESCRIPTION

The details on the pins of TN2130 are listed in Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
2	Source	Source
3	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2130.

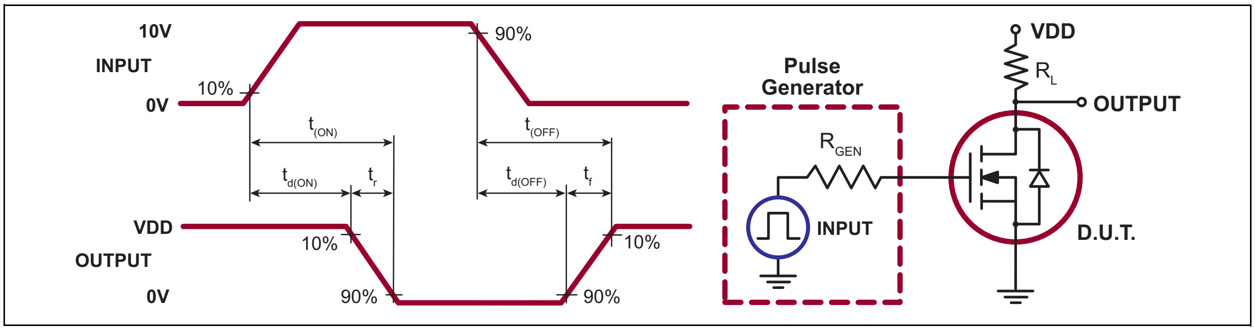


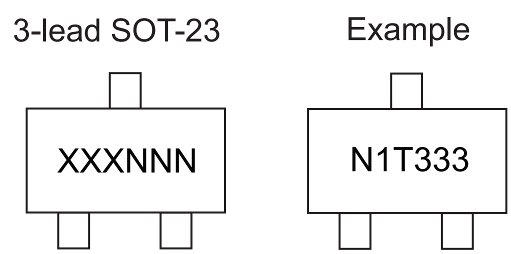
FIGURE 4-1: *Switching Waveforms and Test Circuit.*

TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$V_{GS(th)}$ (Maximum) (V)
300	25	2.4

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

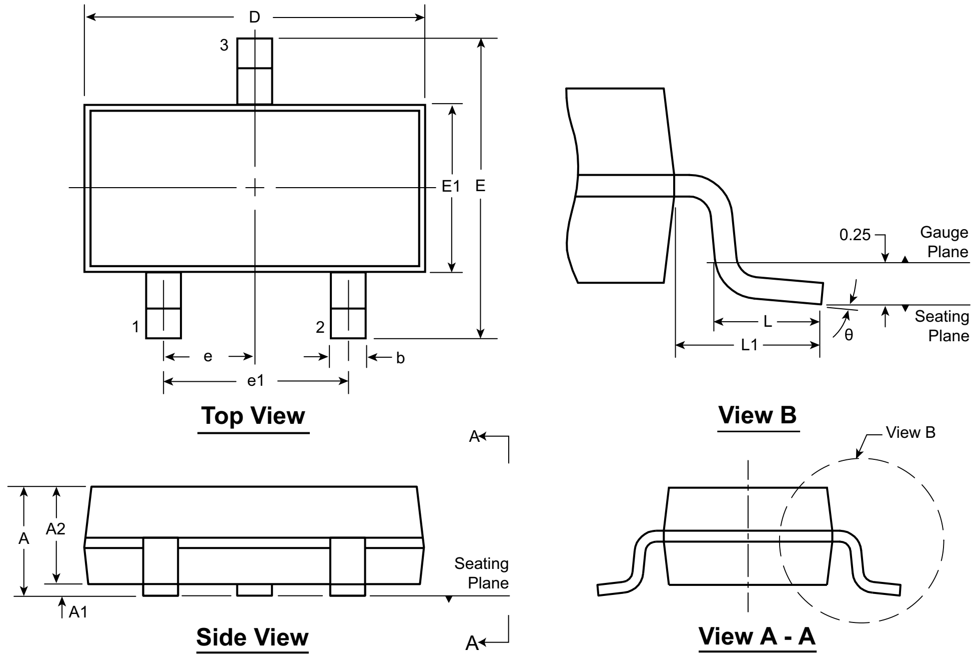


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-236AB (SOT-23) Package Outline (K1/T)

2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Converted Supertex Doc# DSFP-TN2130 to Microchip DS20005944A
- Changed the package marking format
- Made minor text changes throughout the document

Revision B (June 2020)

- Added automotive specifications to the Electrical Characteristics section
- Added automotive specifications to the Product Information System section
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X	-	X
Device	Package Options		Environmental		Media Type		Option

Device:	TN2130	=	N-Channel Enhancement-Mode Vertical DMOS FET
Package:	K1	=	3-lead SOT-23
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3000/Reel for a K1 Package
Option:	VAO	=	Automotive Grade

Example:

a)	TN2130K1-G:	N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-23 package, 3000/Reel
b)	TN2130K1-G-VAO:	N-Channel Enhancement-Mode, Vertical DMOS FET, Automotive Grade, 3-lead SOT-23 package, 3000/Reel

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