Leadtrend

Preliminary Datasheet
LD7841

11/18/2020

High Performance Constant-Voltage Primary-Side-Regulation PWM Controller with Power Factor Correction

REV: P00

The values contained in this preliminary datasheet are for reference only and not for approval. Users should verify for a current and complete document before placing orders

General Description

The LD7841 is a controller targeting for isolated and non−Isolated constant voltage LED drivers. Designed to support flyback, buck-boost topologies, its proprietary voltage mode control algorithm provides near−unity power factor and tightly regulates a constant output voltage from the primary side, thus eliminating the need for a secondary side feedback circuitry or an optocoupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device is specifically intended for very compact space efficient designs and also provides a constant voltage regulation of the output if no load is connected to the LED driver.

Feature

- Wide universal input range (85V_{AC} ~ 305 V_{AC})
- High Voltage Startup: Start-up time : < 0.5 sec.
- Low standby power
  - No load power saving : < 0.2W
  - Standby power consumption: < 0.4W at 150mW output
- Precise CV regulation in the steady state : < ± 5 %
- CV regulation in the load transient: < ± 15%
- Total Harmonic Current Optimization : THDi < 10%
- High Power Factor : PF > 0.92
- Robust Protection Features
  - Brown−In/Out Detection on HV pin
  - AC Over Voltage Protection on HV pin
  - Programmable Output OVP on FB pin
  - Cycle−by−cycle Peak Current Limit on CS pin
  - Over Load Protection
  - Secondary Diode short Protection
  - Pin Short/Open Circuit Protection on CS and FB pin
  - Winding Short Circuit Protection on FB pin
  - Output Short Circuit Protection
- 250 mA / -700 mA Totem Pole Driving capability

Applications

- LED Driver Power Supplies
- Off Line Appliances Requiring Power Factor Correction

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Typical Application

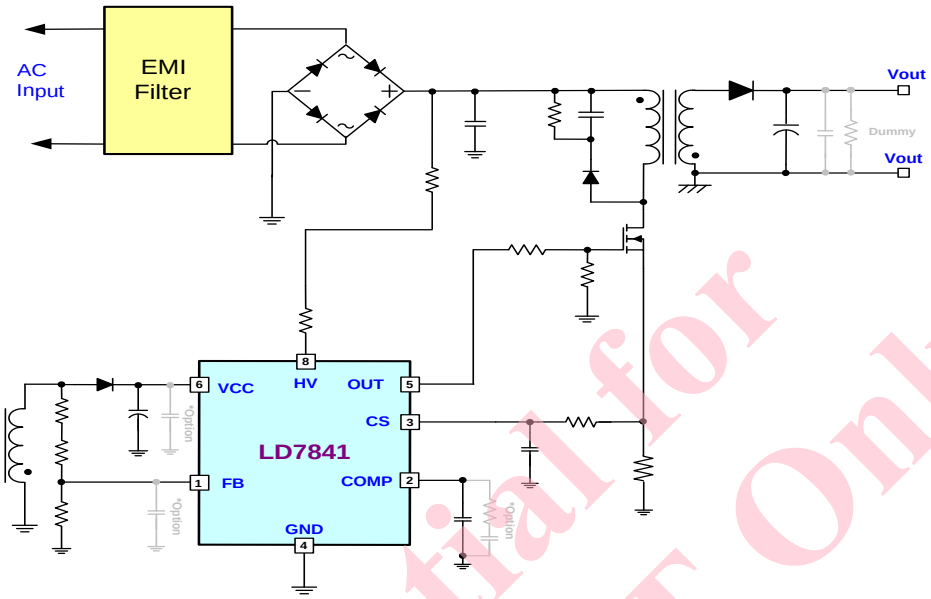

Fig. 1 Reference Circuit Design Topology

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Pin Configuration

SOP-8 (TOP VIEW)

YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		Top Mark	Shipping
LD7841GS	SOP-8	Green package	LD7841GS	2500 /tape & reel

The LD7841 GS is ROHS compliant/ green packaged.

Protection Mode

Item	ACOVP	BNO	VCCOVP	FBOVP	SDSP	CSSP	CSOP	FBUVP (OSCP)	OLP	Int. OTP
LD7841	Auto (VCC 1hiccup)	Auto (VCC 1hiccup)	Auto (VCC 1hiccup)	Auto (VCC 1hiccup)	Auto (VCC 8hiccups)	Auto (VCC 8hiccups)	Auto (VCC 1hiccup)	Auto (VCC 4hiccups)	Auto (VCC 4hiccups)	Auto (VCC 1hiccup)

Pin Descriptions

Pin No	NAME	FUNCTION
1	FB	This pin senses the auxiliary winding voltage for accurate output voltage control and detects the core reset event.
2	COMP	This pin receives a compensation network to stabilize the CV loop.
3	CS	This pin monitors the primary peak current. It is connected to sense resistor of MOSFET for cycle by cycle limitation.
4	GND	The controller ground.
5	OUT	Gate drive output to drive the external MOSFET.
6	VCC	IC operating current and MOSFET driving current are supplied by this pin. This pin is connected to an external auxiliary voltage.
7	NC	Not connection with chip.
8	HV	This pin connects to the bridge diode for providing the startup current and internal high voltage sensing function.

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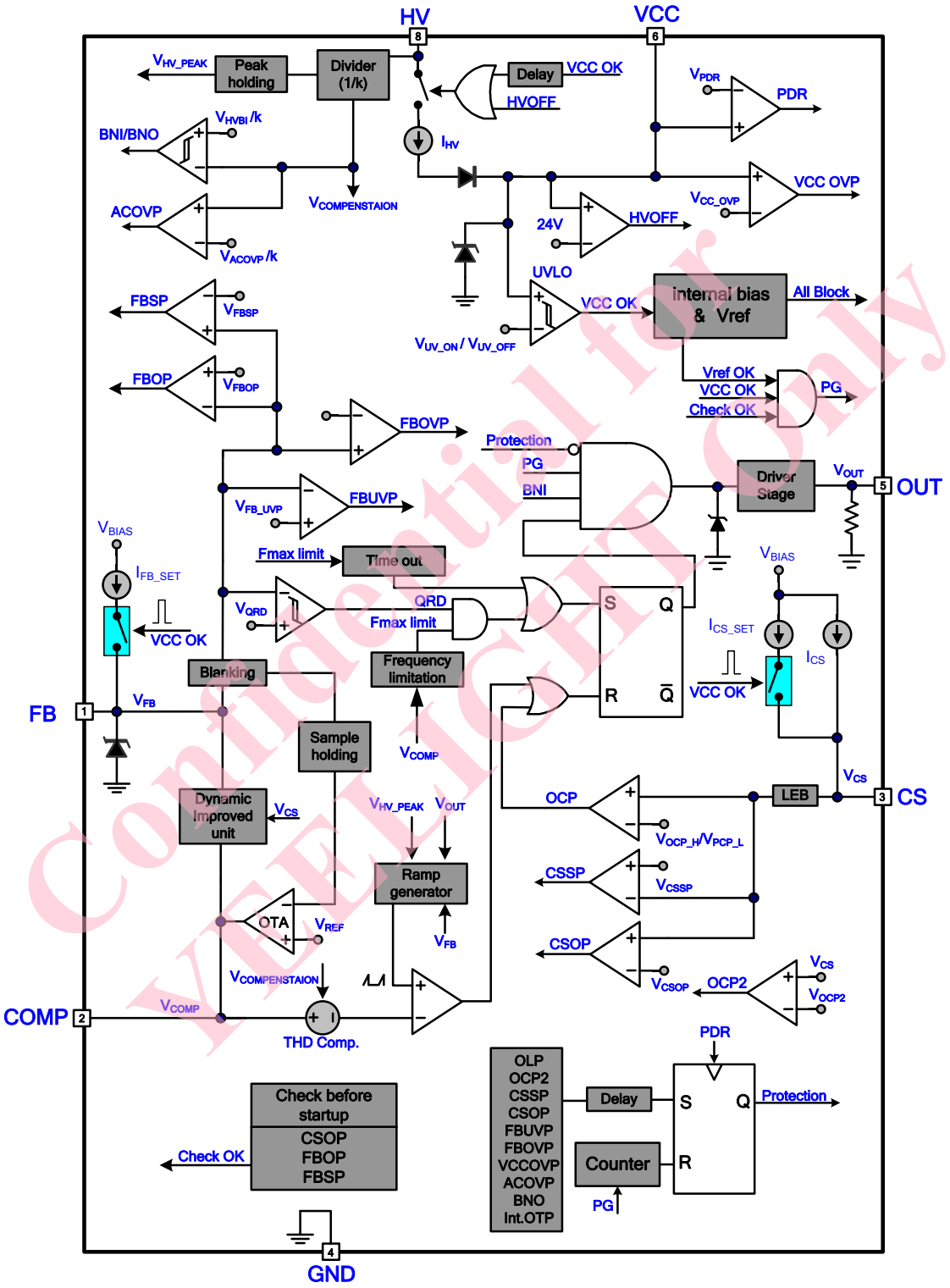
Block Diagram



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Absolute Maximum Ratings

High voltage pin, HV	-0.3 ~ 700V
Supply Voltage VCC	-0.3 ~ 30V
OUT	-0.3 ~ VCC+0.3V
COMP, CS, FB	-0.3 ~ 6V
Source /Sink current on FB	3mA / -1.5mA
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOP-8 at Ambient Temperature = 85 °C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (HV pin)	1.5 KV
ESD Voltage Protection, Human Body Model (except HV pin)	2.5KV
ESD Voltage Protection, Machine Model	250 V
Gate Output Current	250 mA / -700 mA

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature Note3	-40	125	°C
Supply Voltage of VCC	10	24	V
HV Pin Resistance	5	45	kΩ
HV Pin Bypass Capacitance	-	220	pF
VCC pin Capacitance Note3	22	47	μF
COMP pin Capacitance	47	2200	nF
CS pin Filter Capacitance	-	220	pF
CS pin Filter Resistance	0.1	1	kΩ
FB pin Source Current	-	2	mA
FB pin Sink Current	-	0.5	mA

Note：

1) Exceeding these ratings may damage the device.
2) This product guarantees robust performance from -20°C to 105°C ambit temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
3) When operation at harsh environment condition, as temperature and humidity or climate change …etc . Please pay attention to impedance variation between pin to pin or ground to avoid ripple remover closing loop and being failure.

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Electrical Characteristics

V_{CC}=15V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High voltage Supply (HV Pin)						
High voltage current source	V_{HV} = 100V_{DC}, V_{VCC} ≦ V_{PDR}	I_{HV1}		1.5		mA
	V_{HV} = 100V_{DC}, V_{PDR}< V_{VCC} ≦ V_{UV_ON} -0.5V	I_{HV2}		5		mA
Off state leakage current	*;V_{VCC} > V_{UV_ON}, V_{HV}=500 V_{DC}	I_{HV_OFF}			30	μA
Brown-in threshold voltage	V_{VCC} > V_{UV_ON}, V_{FB} = 0V	V_{HVBI}		100		V_{DC}
Brown-in de-bounce time		T_{BNI}		15		ms
Hysteresis of brown-in/out	V_{HVBI} - V_{HVBO}	ΔV_{HV}		15		V_{DC}
Brown-out de-bounce time		T_{BNO}		15		ms
High line threshold voltage	V_{HV_PEAK} is rising.	V_{HLINE}	215	230	245	V_{DC}
Low line threshold voltage	V_{HV_PEAK} is falling	V_{LLINE}	190	205	220	V_{DC}
The de-bounce Time of change V_{OCP} by low to high line	*; V_{OCP_L} change to V_{OCP_H}	T_{DEB_HVLH}		15		ms
The de-bounce Time of change V_{OCP} by high to low line	*; V_{OCP_H} change to V_{OCP_L}	T_{DEB_HVHL}		15		ms
ACOVP threshold voltage		V_{ACOVP}		485		V_{DC}
Hysteresis of ACOVP	*	V_{ACOVP_H}	-	20	-	V_{DC}
The de-bounce time of ACOVP detect function	*	T_{D_ACOVP}		150		μs
Supply Voltage (VCC Pin)						
Startup Current	V_{VCC} < V_{UV_ON}	I_{ST}		75	100	μA
Operating Current	3.45V ≦ V_{FB} ≦ 3.6V @ F_{MIN} , C_{OUT} ≦ 1nF, C_{COMP}=1μF	I_{OP_L}		2.0		mA
	VCCOVP, OLP, CSSP, SDSP, CSOTP… etc.	I_{OP_PRO}		0.35		mA
UVLO (OFF)		V_{UV_OFF}		8.5		V
UVLO (ON)		V_{UV_ON}		17.5		V
VCCOVP threshold voltage		V_{CC_OVP}		28		V
VCCOVP de-bounce Time	*	T_{DEB_OVP}		150		μs

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V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Voltage Feedback (COMP Pin)						
Short circuit current	*; V_{COMP}=0V.	I_{COMP}		1		mA
Open loop voltage		V_{CMP_OPEN}		4.7		V
Over load protection threshold voltage		V_{OLP}	V_{CMP_OPEN} -0.2			V
Over load protection de-bounce Time	*; $V_{COMP} \geqq V_{LOP}$.	T_{DEB_OLP}	-	210	-	ms
Frequency limit reducing start threshold voltage	F_S=F_{S_MAX}	V_{CMP_FLH}		3.0		V
Frequency limit reducing end threshold voltage	*; F_S=F_{S_MIN}	V_{CMP_FLL}		0.3		V
Minimum on time threshold voltage	T_{ON}=T_{ON_MIN}	$V_{CMP_TON_MIN}$		1.0		V
COMP clamping low threshold voltage	*	V_{CMP_LOW}		0.35		V
MAX. turn on time setting	22kΩ ≧ R_{FB} ≧ 18kΩ, V_{HV}=100V_{DC}	T_{MAX_1}		27		μs
	12.5kΩ ≧ R_{FB} ≧ 7.5kΩ, V_{HV}=100V_{DC}	T_{MAX_2}		17		μs
MIN. turn on time	V_{HV}=100V_{DC}, V_{COMP}=$V_{CMP_TON_MIN}$, Maximum on time setting=T_{MAX_1}	T_{MIN_L}		2.1		μs
Minimum frequency	$V_{COMP} \leqq V_{CMP_FLL}$	F_{MIN}		500		Hz
Green frequency	*; V_{COMP} = 1.3V	F_{GREEN}		14		kHz
Maximum frequency	$V_{COMP} \geqq V_{CMP_FLH}$	F_{MAX}		90		kHz
Zero Current Detector and Feedback (FB Pin)						
Upper clamp voltage	I_{FB} = 0.2mA	V_{ZH}	4.6	4.8	5.0	V
Lower clamp voltage	I_{FB} = -2mA	V_{ZL}	0		-0.6	V
Blanking time of FB pin		T_{BLA}		850		ns
Input voltage rising threshold voltage		V_{FBR}		0.5		V
QRD threshold voltage		V_{QRD}		0.3		V
FBOVP threshold voltage for SET0	$R_{CS} \leqq$ 500Ω	$V_{FB_OVP_0}$		4.0		V
FBOVP threshold voltage for SET1	$R_{CS} \geqq$ 800Ω	$V_{FB_OVP_1}$		4.2		V
Hysteresis of FBOVP	*	ΔV_{FB_OVP}		-0.1		V
FBOVP De-bounce	*	T_{DEB_FBOV}	-	4	-	Cycle

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V_{CC}=15.0V, T_A = 25°C unless otherwise specified.)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Zero Current Detector and Feedback (FB Pin)						
FBUVP Threshold		V_{FB_UVP}	0.7	0.8	0.9	V
Output Short Protection De-bounce time	*; Not including T_{SS1}.	T_{DEB_OSCP}		56		ms
Reference voltage during start up time	*	V_{REF_SS}		3.2		V
Soft start of Reference voltage	*	T_{VREF_SS}		300		ms
Internal reference voltage	Steady state ; Tj=25 ℃	V_{REF}	3.465	3.500	3.535	V
	Steady state ; Tj=--40~125 ℃			+/-2		%
Current Sensing (CS Pin)						
V_{CS} Soft Start Time	*; After T_{CCMP} end	T_{SS1}		39		ms
V_{CS} soft start 1	*; After T_{CCMP} end. During T_{SS11}, Fsw=22kHz and V_{CS} limit = 0.2V	T_{SS11}		5		ms
V_{CS} soft start 2	*; After T_{SS11} end, V_{CS} limit rising from 0.2 to 0.7V and 100mV/step	T_{SS12}		34		ms
Leading edge blanking time	*; When 90KHz,max	T_{LEB_CS}		300		ns
Programming delay to OUT pin	*	T_{PD}		100		nS
Over Current Limit	When $V_{HV} \geqq V_{HLINE}$ & T_{DEB_HVLH}	V_{OCP_H}		0.80		V
	When $V_{HV} \leqq V_{LLINE}$ & T_{DEB_HVHL}	V_{OCP_L}		1.00		V
Current Limit-2 for secondary diode short protection		V_{OCP2}		0.7		V
Counter times of Diode Short Protection	*; SDSP is triggered and continuously.	T_{DEB_DSP}		7		cycles
CSSP Threshold Voltage		V_{CSSP}		100		mV
CSSP de-bounce time	*; And $V_{COMP} \geqq$ 2V continuous	T_{CSSP}		56		ms
Gate Drive Output (OUT Pin)						
Output Low Level		V_{G_LO}			0.5	V
Output High Level		V_{G_HI}		13		V
Rising Time	*; C_L=1000pF	T_{G_RISE}		250		ns
Falling Time	*; C_L=1000pF	T_{G_FALL}		35		ns
Internal OTP (Over Temp. Protection)						
OTP Trip level	*; No switching	OTP		140		°C
OTP Hysteresis	*	ΔOTP		20		°C

*: Guaranteed by design.

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Application Information

Operation Overview

LD7841 is an excellent single-stage flyback PFC controller with constant voltage output and primary side regulation (PSR) control algorithm for LED lighting applications. It drives converter operating in quasi-resonant or DCM mode to achieve high efficiency and low THD performance. By PSR, LD7841 is feedback accurately with primary side auxiliary winding without the shunt regulator and optocoupler at secondary side. By voltage-mode control, the turn-on time of the switch is fixed while the turn-off time is varied in steady state. Therefore, the switching frequency varies in accordance with the input voltage or output loading variation. The maximum switching frequency is limited about 90kHz and minimum switching frequency is limited about 500Hz. LD7841 provides robust protections as over load protection, over voltage protection, over current protection, under voltage lockout and LEB of the current sensing. Its major features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. It will take longer time to start up.

To achieve optimized topology, as shown in Fig. 2, LD7841 is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current (I_{HV}) from the full-bridge rectifier to provide the startup current and charge Vcc capacitor (C_{VCC}) at the same time. If the voltage of VCC pin (V_{VCC}) is lower than V_{PDR} (V_{UV_OFF}-1.5V, typ.), I_{HV} is limited about 1.5mA (typ.). Once V_{VCC} is higher than V_{PDR}, I_{HV} increases to 5mA (typ.) around to speed up startup sequence. Meanwhile, the VCC supply current (I_{ST}) consumes only 75μA (typ.), that most of the I_{HV} is reserved to charge C_{VCC}. In using such configuration, the turn on delay time will be almost no difference either in low line or high line conditions.

Once the V_{VCC} is higher than V_{UV_ON} (17.5V, typ.) and all of condition are checked (BNI, setting and CSSP…etc.), LD7841 powers on and further to deliver the gate drive signal, I_{HV} will not disabled right away and keeping provide current about 65ms (=T_{IHV_MAX}) around for smaller C_{VCC} application. During T_{IHV_MAX} period, if V_{VCC} is higher than 23V (typ.), I_{HV} is disabled immediately.

The supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect V_{CC} to ensure the supply voltage enough to power on and in addition to drive the power MOSFET. As shown in Fig. 3, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

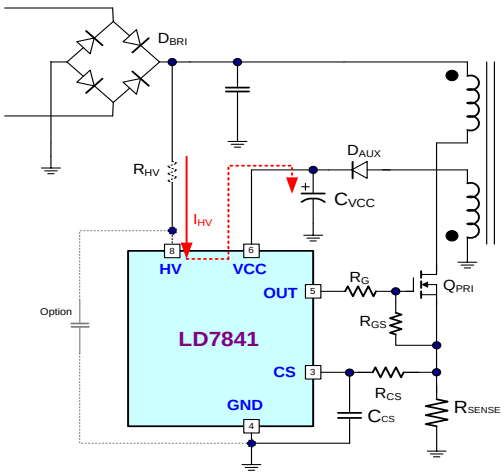

Fig. 2 Startup circuit

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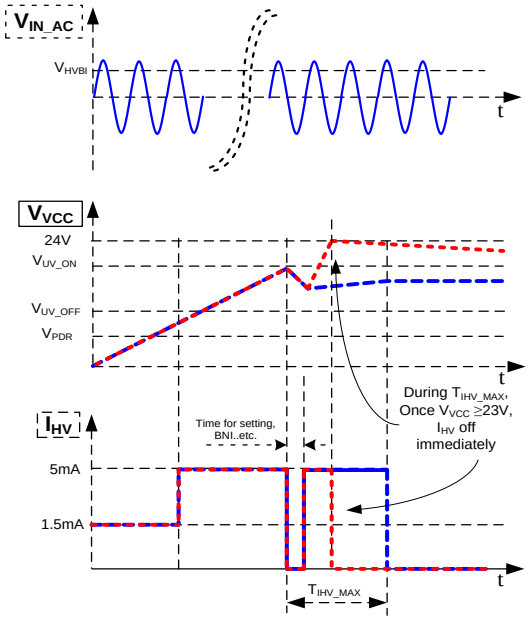

Fig. 3 I_{HV} Typically waveform

Brown-In/Out

LD7841 provides brown-in/out function on HV pin. Fig. 4 and Fig. 5 show the operation. When V_{HV} is always lower than V_{HVBI} (100V, typ.) during each period of T_{BNI} (15ms, typ.), the gate output will remain off even when the V_{VCC} already reaches V_{UV_ON}. It therefore forces the V_{VCC} hiccup between V_{UV_ON} and V_{UV_OFF} until V_{HV} is higher than V_{HVBI}. A hysteresis ($\triangle V_{HV}$, 15V, typ.) is implemented to prevent the false-triggering during turn-on and turn off.

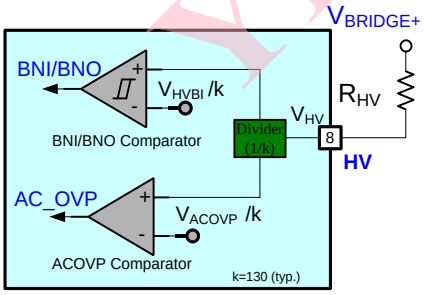

Fig. 4 BNI/BNO and AC_OVP block

After brown in condition is triggered, once V_{HV} is always lower than V_{HVBI} -$\triangle V_{HV}$ and longer than de-bounce time (T_{BNO}, 15ms, typ.), LD7841 will shut off to prevent from any damage.

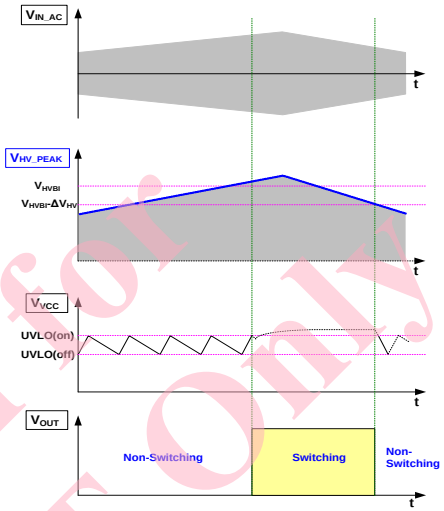

Fig. 5 BNI/BNO function

Maximum On-Time Setting

LD7841 provides the maximum on time (T_{ON_MAX}) programmable function on FB pin. T_{ON_MAX} should be set according to the condition of the transformer, lowest AC line voltage, and maximum output power. A choice of optimum T_{ON_MAX} would result in best performance. As Fig.6, after V_{VCC} is higher than V_{UV_ON}, and BNI is triggered, the internal current source provides a constant current (I_{FB_SET}, 90 μA, typ.) about 450 μs (typ.) passed thought R_{FB_T} to check this voltage then set T_{MAX_N}.

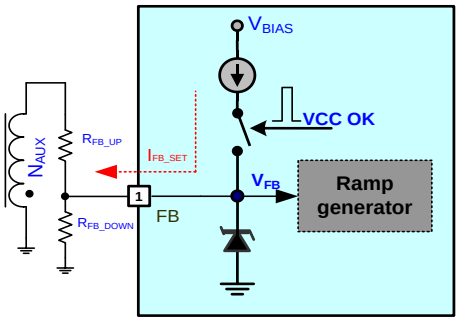

Fig. 6 Maximum on time setting block

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Where:

$$R_{FB_T} = \frac{(R_{FB_{UP}} \times R_{FB_{DOWN}})}{(R_{FB_UP} + R_{FB_DOWN})} \quad \text{(eq.1)}$$

The following table is the resistance suggestion for maximum on-time setting.

T_{MAX_N}	Condition	Max. on Time @V_{HV}=100V_{DC}	R_{FB_T} suggestion
T_{MAX_1}	25kΩ≧R_{FB_T}≧18kΩ	27μs	22kΩ
T_{MAX_2}	12.5kΩ≧R_{FB_T}≧7.5kΩ	17μs	10kΩ

Table. 1 Maximum on Time Setting

LD7841 implements the compensation of on time by monitor HV pin, as shown in below,

$$T_{ON_MAX} = T_{MAX_N} \times K_{TON} \quad \text{(eq.2)}$$

$$K_{TON} = \frac{100V}{V_{HV_PEAK}} \quad \text{(eq.3)}$$

Where: V_{HV_PEAK} is from 100V_{DC} to 420V_{DC}. For abnormal condition, if FB pin is shorted to GND or floating (badly soldered), LD7841 will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

FB Short / Open Circuit Protection Before Startup

For abnormal condition, if the FB pin is floating (Open condition), I_{FB_SET} will pull high the V_{FB}, once V_{FB} is higher than 2.7V (typ.). LD7841 will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

If the FB pin is shorted to GND, V_{FB} will be pull low, once V_{FB} is lower than 0.35V (typ.). LD7841 will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

Dynamic Improved Threshold Level Setting

LD7841 provides the dynamic improved threshold level programmable function. As Fig.7, after V_{CC} is higher than V_{UV_ON}, and BNI is triggered, the internal current source provides a constant current (I_{CS_SET}, 270 μA, typ.) about 600 μs (typ.) passed thought R_{CS} to set threshold level.

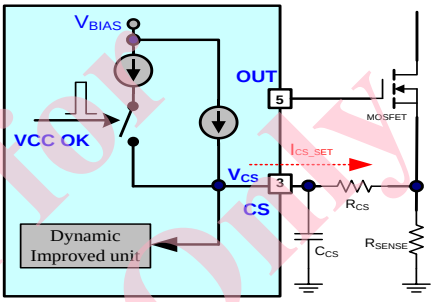

Fig. 7 Dynamic improved threshold level setting block

Table.2 is the resistance suggestion for dynamic improved threshold level setting.

ITEM	R_{CS} (Ω)	USD	OSD1	OSD2	OSD3	V_{FB_OVP} (V)
		Percentage to V_{REF} (%)				
SET0	≦500	-4.3	+4.3	+7.85	+12.5	4.0V
SET1	≧800	-7.85	+7.85	+12.5	+17.5	4.2V

Table. 2 Dynamic and Over Voltage Setting

For abnormal condition, if the CS pin is floating, I_{CS_SET} will pull high the V_{CS}, once V_{CS} is higher than 2V (min.) LD7841 will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

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Current Sense Short Circuit Protection before Startup

After settings are done, LD7841 delivers one pulse gate drive signal to turn on the MOSFET and check the condition of CS pin. This pulse width is given by the following equation.

$$T_{ON_CSSP} \approx 0.3 \times (K_{TON}) \times T_{MAX_N} \quad \text{(eq.4)}$$

If V_{CS} is higher than V_{CSSP} (100mV, typ.) during T_{ON_CSSP}, it means the function of current sense is normal, LD7841 will operate into soft start after T_{CCMP} (3ms, typ.). If V_{CS} is higher than 200mV, gate off immediately to avoid the saturation of transformer. Once V_{CS} is lower than V_{CSSP}, the protection of current sense short circuit before startup triggered, LD7841 will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

Soft Start

LD7841 provides soft start function by steps current sense limitation and steps reference voltage (V_{REF}) of feedback loop. At startup, the output voltage is very low, system operates into CCM and causes higher stress. So, V_{CS} is limited at 0.2V and the switching frequency (F_{SW}) is fixed at 22kHz (typ.) in first 3ms during soft start (T_{SS1}). After T_{SS1}, V_{CS} is rising from 0.2V to 0.7V step by step about 34ms (T_{SS2}, typ.) and F_{SW} is controlled by the voltage of COMP pin (V_{COMP}). Fig. 8 is shown typical waveforms.

Besides the current sense limitation for soft start, LD7841 also provide the reference voltage steps to avoid the overshoot during startup. As shown in Fig.9, the V_{REF} is set as V_{REF_SS} (3.2V, typ.) initial until feedback regulation. Once V_{COMP} is pulled low to appropriate level during soft start, the V_{REF} is rising from 3.2V to 3.5V step by step about 300ms (T_{VREF_SS}, typ.).

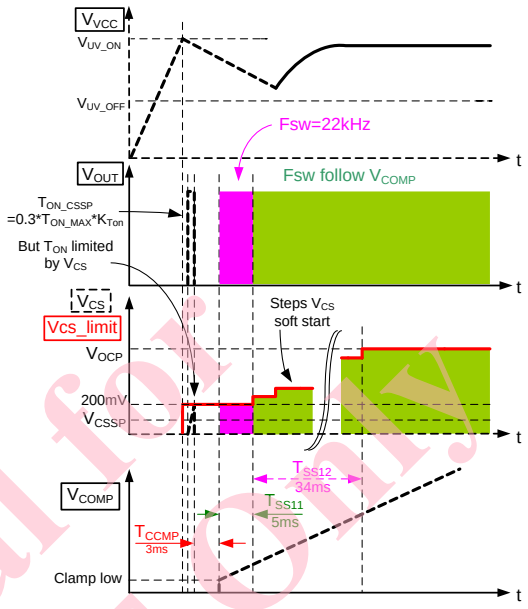

Fig. 8 current sense limitation steps function

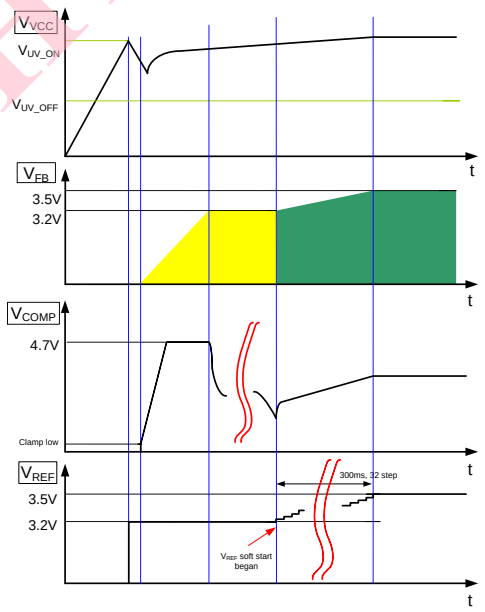

Fig. 9 reference voltage steps function

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Primary Side Regulation

LD7841 detects the auxiliary winding to achieve constant voltage regulation. The typically waveform is shown in Fig.10. When the current of secondary side discharging to zero, the primary side V_{FB} is at knee point, then LD7841 samples the voltage at knee point and holds it until next switching cycle. This signal ($V_{FB_S\&H}$) is compared to V_{REF} by the internal error amplifier. As shown in Fig.11. In order to keep the system is stable, place the compensation network at COMP pin to GND as closed as possible.

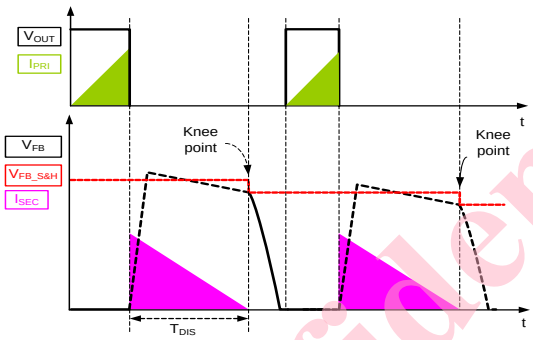

Fig. 10 V_{FB} Typically waveform

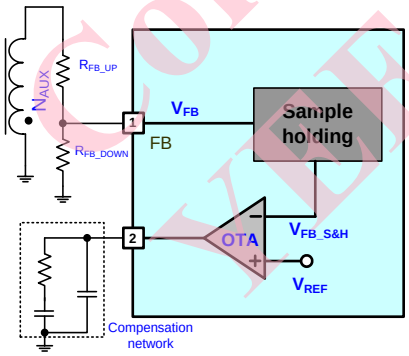

Fig. 11 Feedback function block

Principle of Constant Voltage Operation

The output voltage is given by the following equation.

$$V_{OUT} = (V_{REF} \times \frac{N_{SEC}}{N_{AUX}} \times \frac{R_{FB_UP}+R_{FB_DOWN}}{R_{FB_DOWN}}) - V_F \quad \text{(eq.5)}$$

Where:

N_{SEC} is the turns of secondary main output winding.

N_{AUX} is the turns of auxiliary winding voltage to supply for VCC.

V_{REF} is the reference voltage of constant voltage feedback.

V_F is forward voltage of secondary rectifier diode.

Frequency Limitation

LD7841 implements the frequency limitation function to improve efficiency at light load. As shown in Fig.12, the maximum switching frequency is controlled by V_{COMP}.

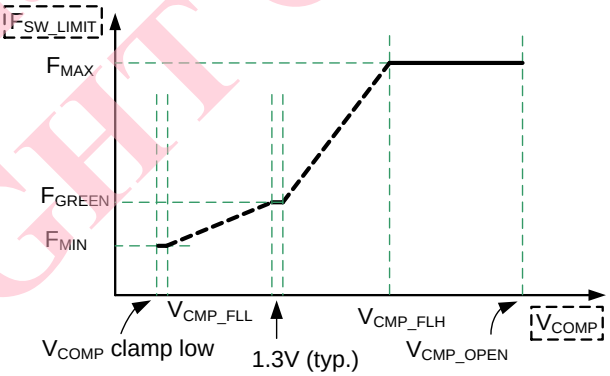

Fig. 12 Frequency limitation curve

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 13 shows typical function block. V_{COMP} and the output of the ramp generator block are compared to determine the MOSFET on-time.

A greater V_{COMP} produces more on-time. Using an external resistor connected to FB pin to set the desired slope of the internal ramp, the user may program the T_{ON_MAX}. Alternatively, the on-time will also achieve its maximum when V_{COMP} trip to V_{CMP_OPEN} (4.7V, typ.).

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As shown in Fig.14, The block of zero current detection will detect auxiliary winding signal to drive MOSFET. If V_{FB} rises over V_{FBR} (0.5V, typ.) after T_{BLA}+400ns then drops under V_{QRD} (0.3V, typ.), the QRD signal is triggered and turn on MOSFET. As V_{FB} first drops to V_{QRD}, the current through the transformer is below zero. This feature enables transition-mode operation.

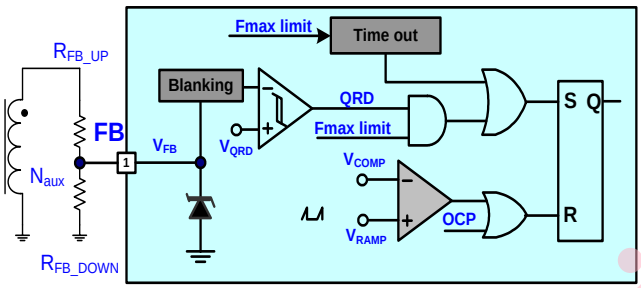

Fig. 13 QRD function block

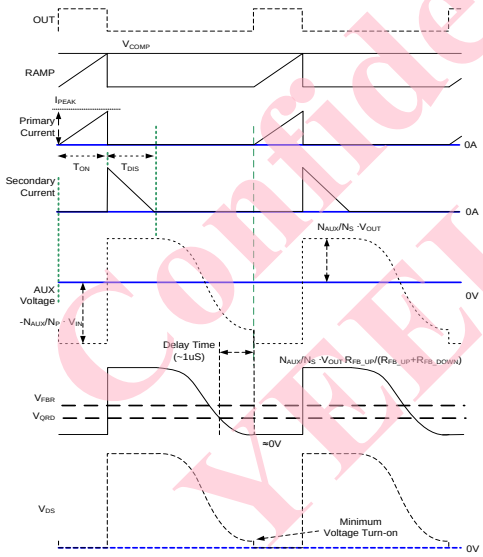

Fig. 14 QRD detection on FB pin

Quasi-Resonant / DCM Operation

According to the difference of V_{FB}, LD7841 could operate at quasi-resonant mode or DCM mode. As shown in Fig. 15. If QRD signal is triggered after the end of TO1 but before TO2, LD7841 operates at quasi-resonant mode.

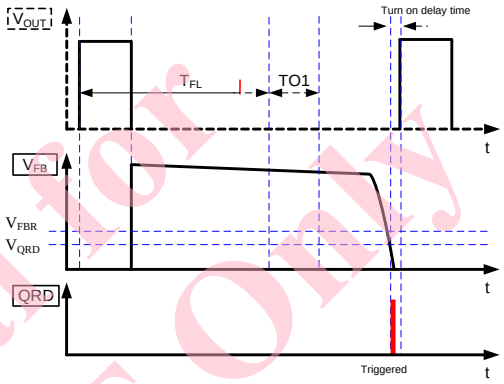

Fig. 15 QR mode

As shown in Fig. 16. If QRD signal is triggered before the end of T_{FL}, the QRD signal is triggered but blanked to turn on MOSFET. After T_{FL}, QRD signal is triggered again and turn on the MOSFET during TO1 (~5μs.), LD7841 operates at DCM mode with valley switching. Where:

$$T_{FL} = \frac{1}{F_{SW_LIMIT}} \quad \text{(eq.6)}$$

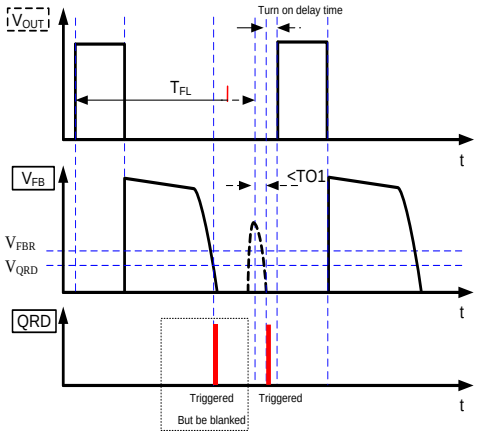

Fig. 16 DCM mode with valley switch

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Same as previous condition but If QRD signal is not triggered again, the MOSFET will be turn on at the end of TO1 directly. LD7841 operates at DCM mode. As shown in Fig. 17.

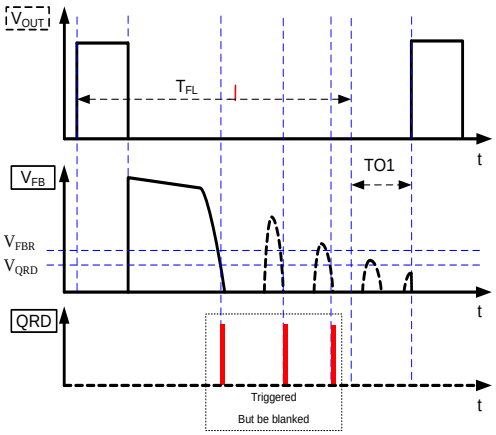

Fig. 17 DCM mode

Output Drive Stage

With typical 250mA/-700mA peak driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at 13V to protect the MOSFET gate even when the V_{CC} voltage is higher than 13V.

Leading-Edge Blanking and Cycle by Cycle limitation

A 300ns (typ.) leading-edge blanking time (T_{LEB}) is included in the input of CS pin to prevent the false-trigger from the current spike. In the different rated power application, if the total pulse width of the turn-on spikes is lower than and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

LD7841 detects the primary side peak current from the CS pin, which is used for cycle by cycle peak current limit. The maximum voltage threshold of the CS pin set as V_{OCP_L} (1.0V, typ.) or V_{OCP_H} (0.8V, typ.) which are controlled by V_{HV}, once V_{CS} is higher than V_{OCP_X}, gate off immediately.

Protection Function

VCC Over Voltage Protection - 1 Hiccup

The maximum rating of the VCC pin is limited below 30V. To prevent VCC from the fault condition, LD7841 is implemented with OVP function on VCC pin. When V_{VCC} higher than V_{CC_CLAMP} (25V, typ.), LD7841 will sink a current about 2mA (typ.) first from VCC pin. But if supplier voltage keeps rising and higher than V_{CC_OVP} (28V, typ.) and de-bounce about 250μs, LD7841 will enforce the gate off until the 1st cycle of VCC hiccup is tripped and the fault condition is removed.

FB Over Voltage Protection - 1 Hiccup

If R_{FB_UP} is shorted or R_{FB_DOWN} is opened during operating, the feedback signal is incorrect. LD7841 is implemented with OVP function on FB pin. Once V_{FB} is higher than $V_{FB_OVP_0}$ (4.0V, typ.) or $V_{FB_OVP_1}$ (4.2V, typ.) and de-bounce about 4 switching cycles continuously, LD7841 will enforce the gate off until the 1st cycle of VCC hiccup is tripped and the fault condition is removed.

FB Under Voltage Protection (OSCP) - 4 Hiccups

When the output short circuit occurs, the reflected output voltage of auxiliary winding will cause V_{FB} down. If V_{FB} is lower than V_{FB_UVP} (0.8V, typ.) and de-bounce about 56ms, LD7841 will enforce the gate off until the 4th cycle of VCC hiccup is tripped and the fault condition is removed. For abnormal condition, if R_{FB_UP} is opened or R_{FB_DOWN} is shorted, FB under voltage protection is triggered too.

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CS Short Circuit Protection - 8 Hiccups

To avoid the damaged which is caused by CS pin short circuit during operating, LD7841 implemented a smart and robust CS short circuit protection function. If such fault condition occurs and V_{CS} is lower than V_{CSS} (100mV, typ.) then V_{COMP} is higher than 2V (typ.), after de-bounce about 56ms (T_{CSSP}), LD7841 will enforce the gate off until the 8th cycle of VCC hiccup is tripped and the fault condition is removed. As shown in Fig. 18.

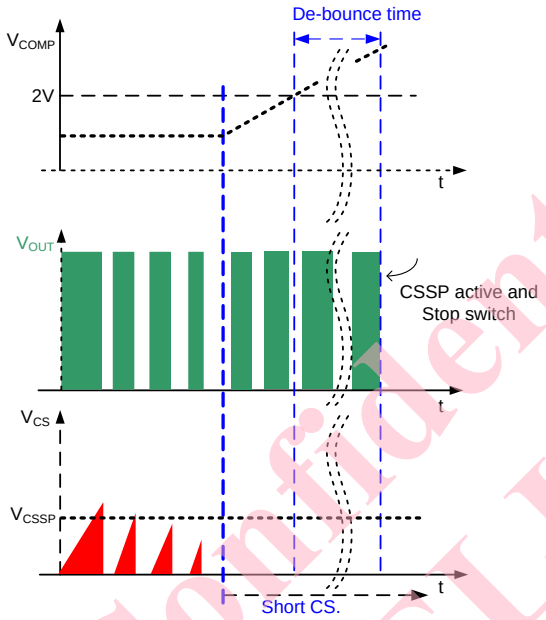

Fig. 18 Current Sense Short Circuit Protection

CS Open protection - 1 Hiccup

If R_{CS} is opened during operating, The internal current source (I_{CS}, 10 μA, typ.) from CS pin to output , once V_{CS} is higher than V_{OCP_X}, LD7841 will enforce the gate off until the 1ST cycle of VCC hiccup is tripped and the fault condition is removed.

AC Over Voltage protection - 1 Hiccup

To avoid the input voltage is too high to cause circuit damaged, LD7841 implemented the AC over voltage protection function on HV pin to monitor it. If such fault condition occurs and V_{HV} is higher than V_{ACOVP} (485V, typ.), after de-bounce about 150 μs (T_{D_ACOVP}), LD7841 will enforce the gate off until the 1st cycle of VCC hiccup is tripped and the fault condition is removed.

Over Loading protection - 4 Hiccups

LD7841 implemented the over loading protection, once V_{COMP} is higher than V_{OLP} (V_{CMP_OPEN}-0.2V, typ.) and after de-bounce about 210ms (T_{DEB_OLP}, typ.), LD7841 will enforce the gate off until the 4th cycle of VCC hiccup is tripped and the fault condition is removed.

Secondary Diode Short Protection – 8 Hiccups

The circuit detects output diode short condition if 7 consecutive switching cycles occur within which the CS pin voltage exceeds V_{OCP2} (0.7V ,typ) during leading-edge blanking time (T_{LEB}), LD7841 will enforce the gate off until the 8th cycle of VCC hiccup is tripped and the fault condition is removed.

Internal Over Temperature Protection - 1 Hiccup

When the junction temperature reaches 140°C approximately, the thermal sensor signals would stop IC's switching. If the IC's junction temperature cools by 20°C or VCC restart again.

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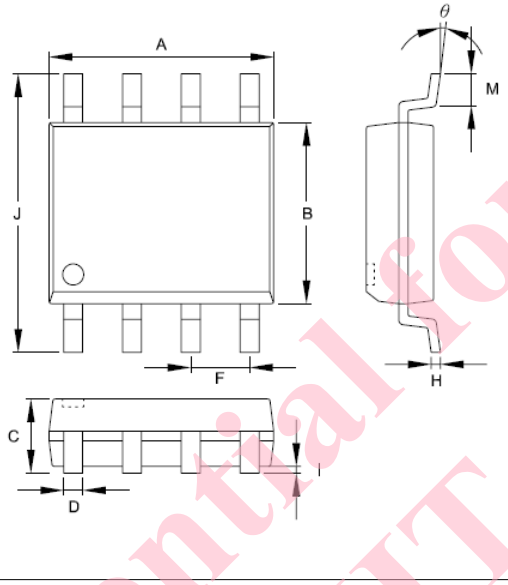
Package Information

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

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Revision History

REV.	Date	Change Notice
P00	11/18/2020	Original Specification.

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