

30V N-Channel Enhancement Mode MOSFET

Description

The AP150N03P/T uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

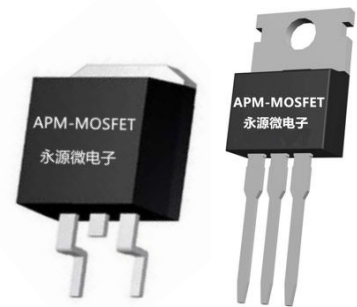
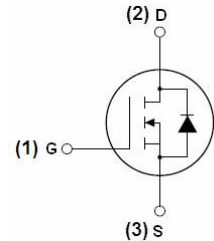
General Features

$V_{DS} = 30V$ $I_D = 150A$

$R_{DS(ON)} < 4m\Omega$ @ $V_{GS} = 10V$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP150N03P	TO-220-3	AP150N03P XXX YYYY	1000
AP150N03T	TO-263-3	AP150N03T XXX YYYY	1000

Absolute Maximum Ratings (TC=25°C unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	150	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	72	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	17	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	14	A
I_{DM}	Pulsed Drain Current ²	225	A
EAS	Single Pulse Avalanche Energy ³	145	mJ
I_{AS}	Avalanche Current	53.8	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	86.8	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	1.44	°C/W

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Electrical Characteristics (at $T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=1\text{mA}$	---	0.0213	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	---	4	m Ω
		$V_{GS}=4.5V, I_D=15A$	---	---	6	
$V_{GS(th)}$	Gate Threshold Voltage		1.0	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}, I_D=250\mu A$	---	-5.73	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	26.5	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.4	---	Ω
Q_g	Total Gate Charge (4.5V)		---	31.6	---	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=20V, V_{GS}=4.5V, I_D=12A$	---	6.1	---	
Q_{gd}	Gate-Drain Charge		---	13.8	---	
$T_{d(on)}$	Turn-On Delay Time		---	11.2	---	ns
T_r	Rise Time	$V_{DD}=15V, V_{GS}=10V, R_G=1.5$	---	49	---	
$T_{d(off)}$	Turn-Off Delay Time	$I_D=20A$	---	35	---	
T_f	Fall Time		---	7.8	---	
C_{iss}	Input Capacitance		---	3075	---	pF
C_{oss}	Output Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	400	---	
C_{rss}	Reverse Transfer Capacitance		---	315	---	
I_S	Continuous Source Current ^{1,5}		---	---	110	A
I_{SM}	Pulsed Source Current ^{2,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	225	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3 .The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=53.8A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

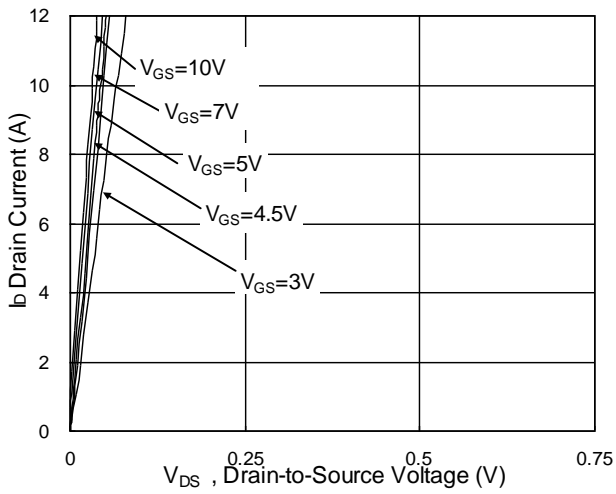


Fig.1 Typical Output Characteristics

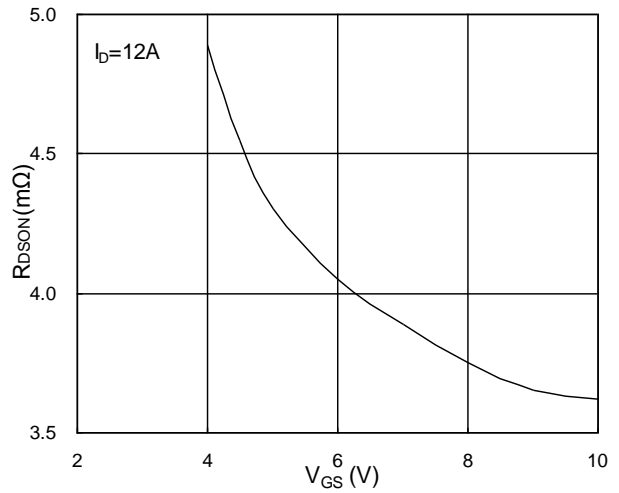


Fig.2 On-Resistance vs. G-S Voltage

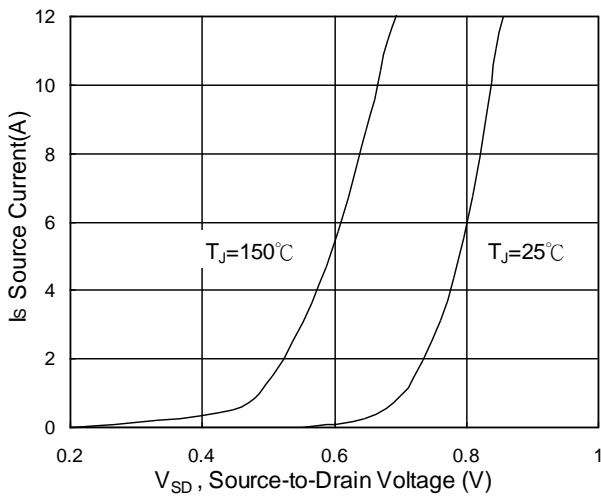


Fig.3 Forward Characteristics of Reverse

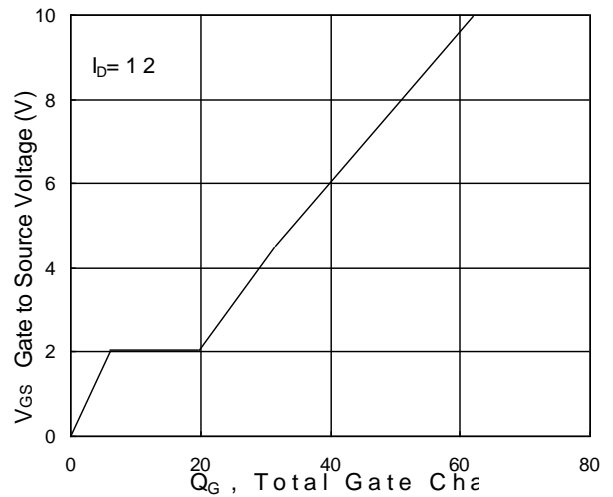


Fig.4 Gate-Charge Characteristics

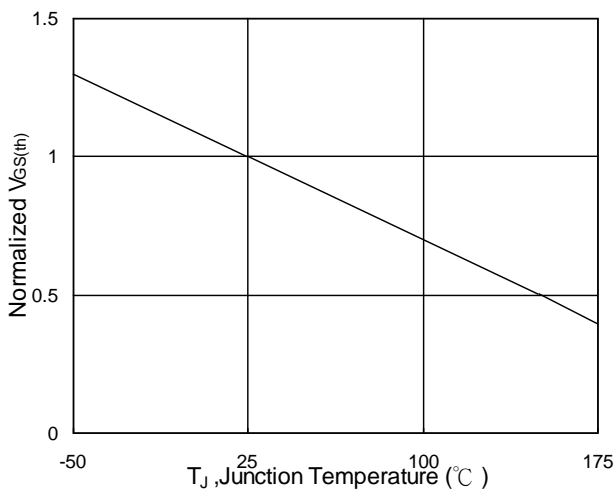


Fig.5 Normalized V_{GS(th)} vs. T_J

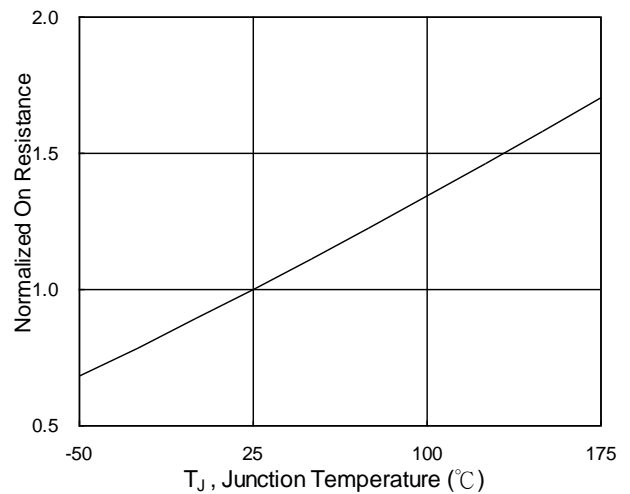


Fig.6 Normalized R_{DS(on)} vs. T_J



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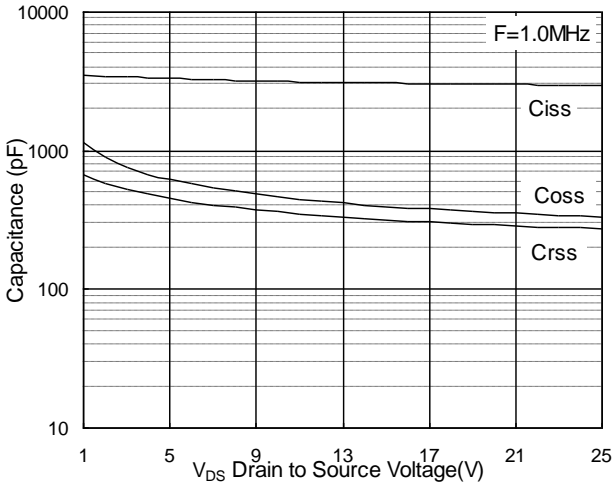


Fig.7 Capacitance

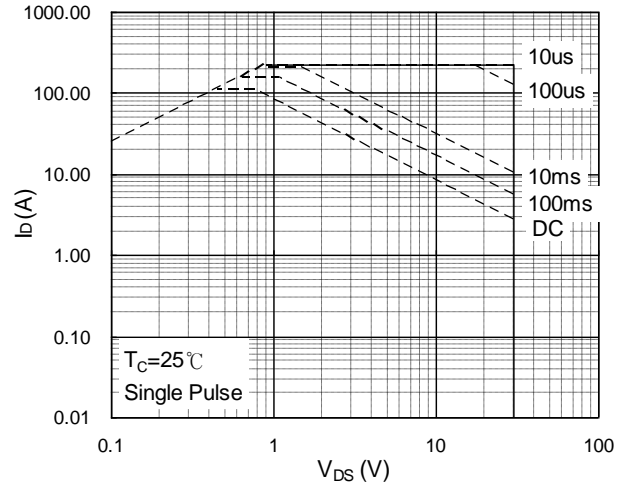


Fig.8 Safe Operating Area

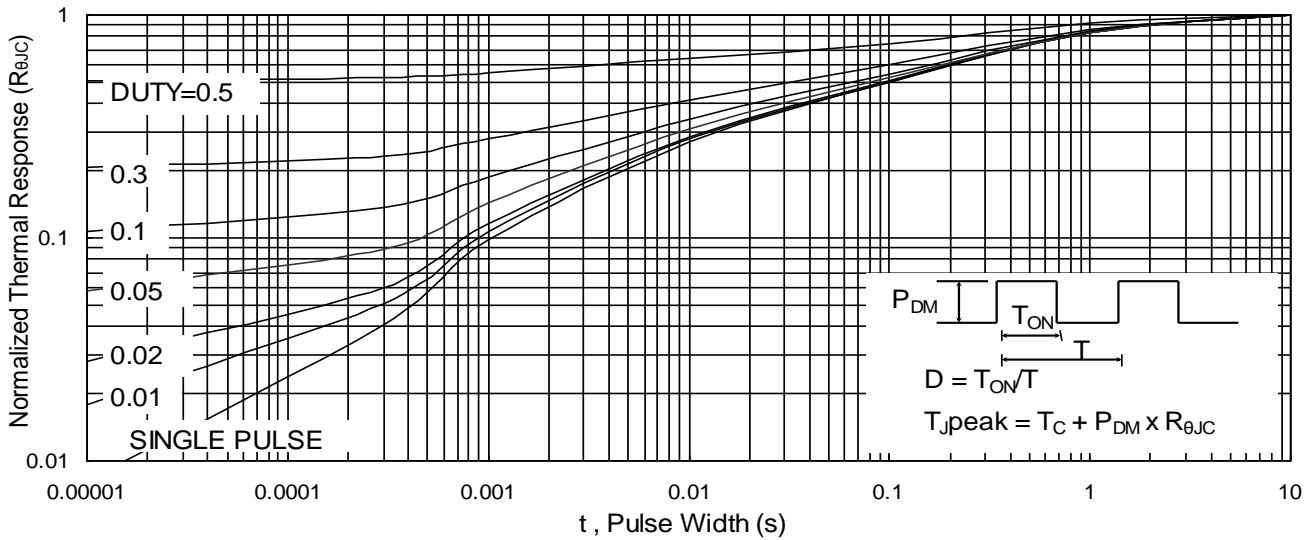


Fig.9 Normalized Maximum Transient Thermal Impedance

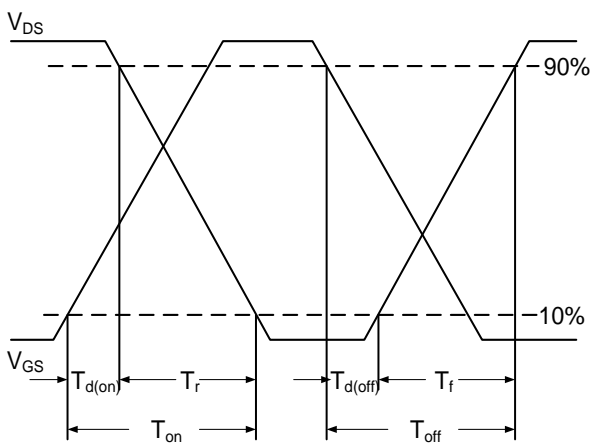


Fig.10 Switching Time Waveform

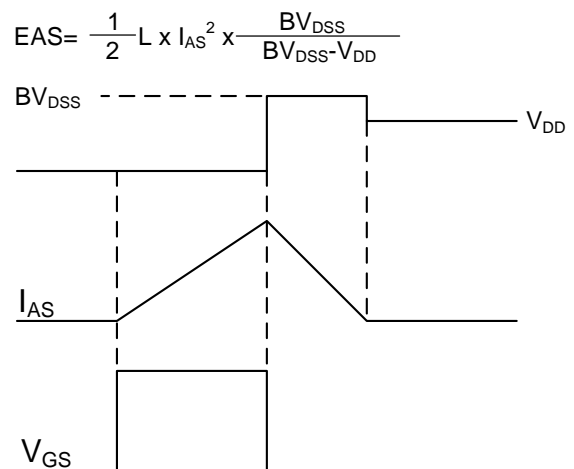
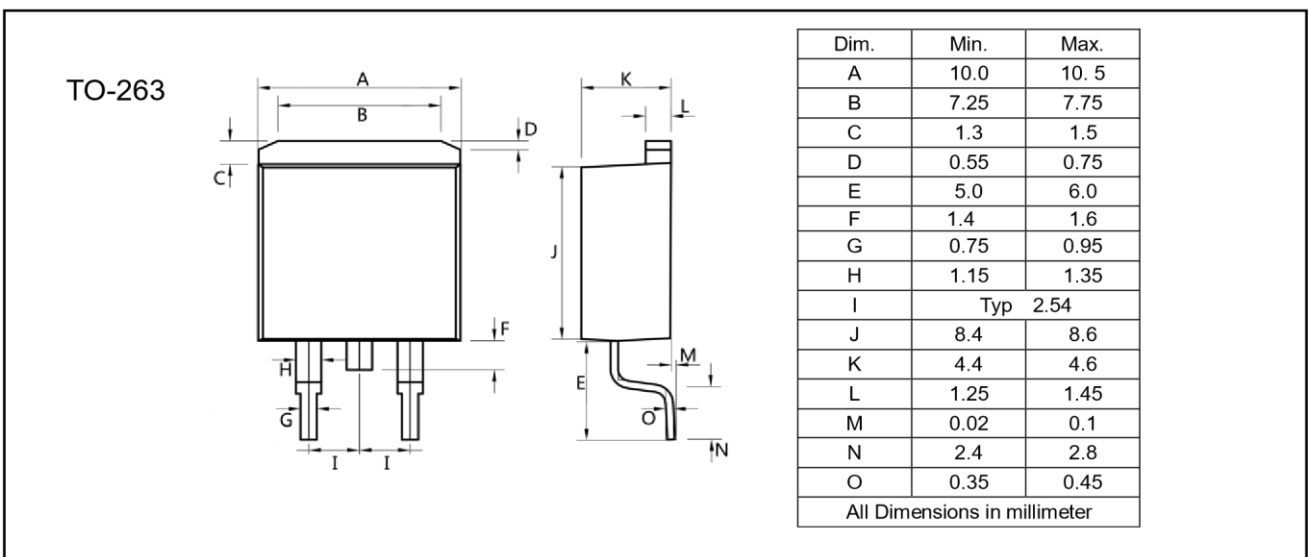
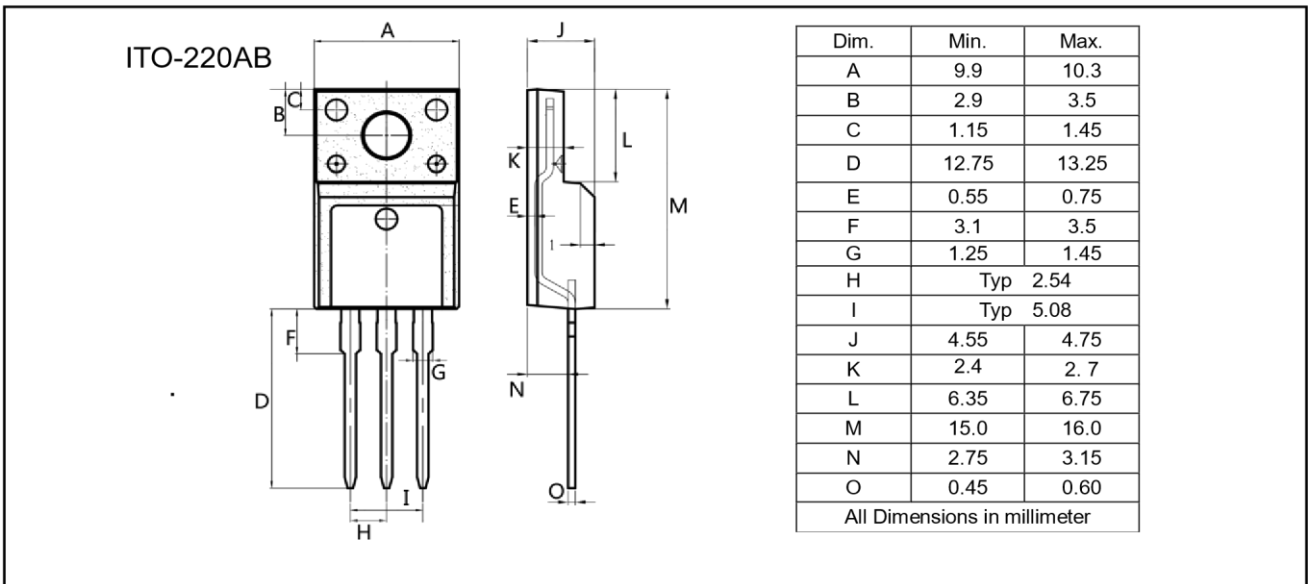
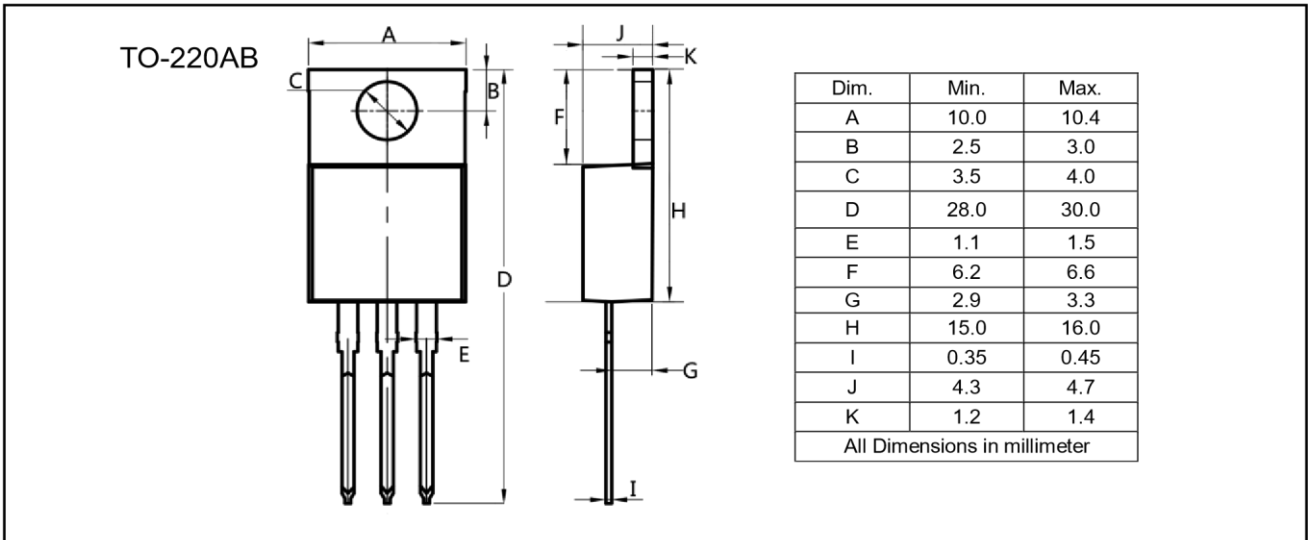


Fig.11 Unclamped Inductive Switching Waveform



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