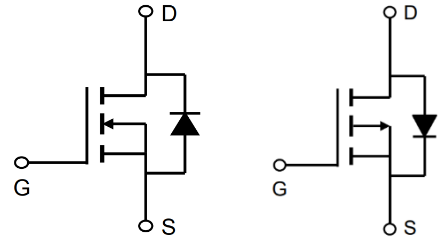


40V N+P-Channel Enhancement Mode MOSFET

Description

The AP10G04DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



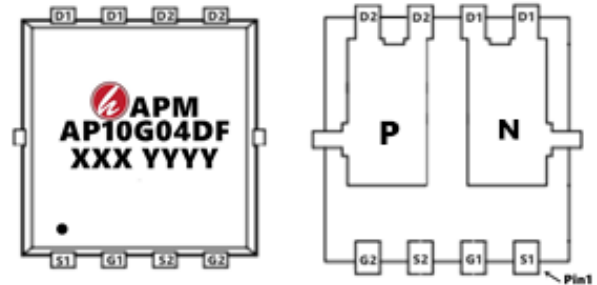
General Features

$V_{DS} = 40V$ $I_D = 9.8A$

$R_{DS(ON)} < 17m\Omega$ @ $V_{GS}=10V$

$V_{DS} = -40V$ $I_D = -7.5A$

$R_{DS(ON)} < 45m\Omega$ @ $V_{GS}=-10V$



Application

Wireless charging

Boost driver

Brushless motor



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10G04DF	PDFN3*3-8L	AP10G04DF XXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_{D@T_A=25^\circ C}$	Continuous Drain Current, V_{GS} @ 10V ¹	9.8	-7.5	A
$I_{D@T_A=70^\circ C}$	Continuous Drain Current, V_{GS} @ 10V ¹	5.2	-4.8	A
I_{DM}	Pulsed Drain Current ²	23	-22	A
EAS	Single Pulse Avalanche Energy ³	16.2	39	mJ
I_{AS}	Avalanche Current	18	-28	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	1.67	1.67	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	75		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	30		$^\circ C/W$

40V N+P-Channel Enhancement Mode MOSFET

N-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	---	---	V
ΔBVDSS/ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.034	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =5A	---	17.5	26	mΩ
		V _{GS} =4.5V, I _D =4A	---	25.0	35	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.6	2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-4.56	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =32V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =32V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =5A	---	14	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.6	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =20V, V _{GS} =4.5V, I _D =5A	---	5.5	---	nC
Q _{gs}	Gate-Source Charge		---	1.25	---	
Q _{gd}	Gate-Drain Charge		---	2.5	---	
Td(on)	Turn-On Delay Time	V _{DD} =20V, V _{GS} =10V, R _G =3.3Ω I _D =1A	---	8.9	---	ns
T _r	Rise Time		---	2.2	---	
Td(off)	Turn-Off Delay Time		---	41	---	
T _f	Fall Time		---	2.7	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	593	---	pF
C _{oss}	Output Capacitance		---	76	---	
Crss	Reverse Transfer Capacitance		---	56	---	
I _s	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	6.1	A
ISM	Pulsed Source Current ^{2,5}		---	---	23	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=10A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

40V N+P-Channel Enhancement Mode MOSFET

P-Channel Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-40	---	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.02	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-6A	---	38	45	mΩ
		V _{GS} =-4.5V, I _D =-3A	---	48	60	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	-1.6	-2.5	V
ΔVGS(th)	V _{GS(th)} Temperature Coefficient		---	3.72	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =-32V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-32V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =-5V, I _D =-6A	---	13	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-6A	---	11.5	---	nC
Q _{gs}	Gate-Source Charge		---	3.5	---	
Q _{gd}	Gate-Drain Charge		---	3.3	---	
Td(on)	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	22	---	ns
T _r	Rise Time		---	15.7	---	
Td(off)	Turn-Off Delay Time		---	59	---	
T _f	Fall Time		---	5.5	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1415	---	pF
C _{oss}	Output Capacitance		---	134	---	
C _{rss}	Reverse Transfer Capacitance		---	102	---	
I _s	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-6	A
ISM	Pulsed Source Current ^{2,5}		---	---	-22	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%
- 3、 The EAS data shows Max. rating. The test condition is V^{DD}=-25V, V^{GS}=-10V, L=0.1mH, I^{AS}=-10A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

N-Typical Characteristics

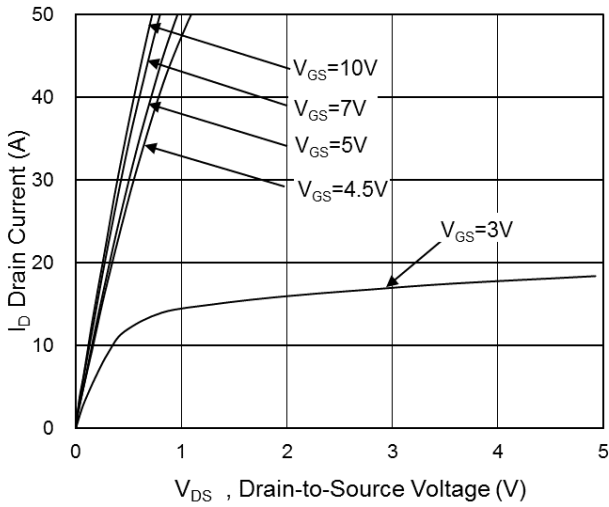


Fig.1 Typical Output Characteristics

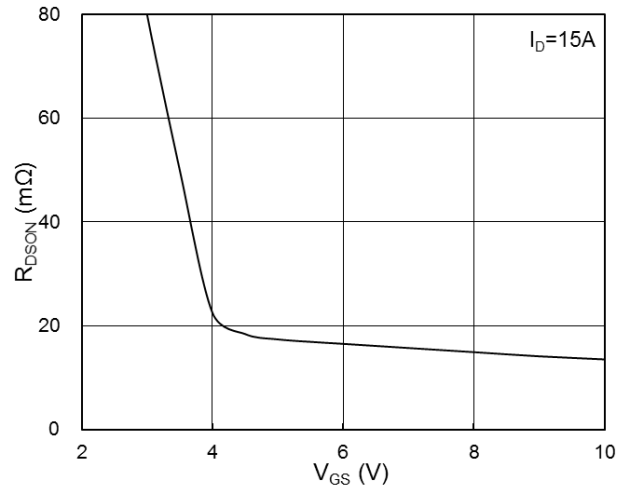


Fig.2 On-Resistance vs. G-S Voltage

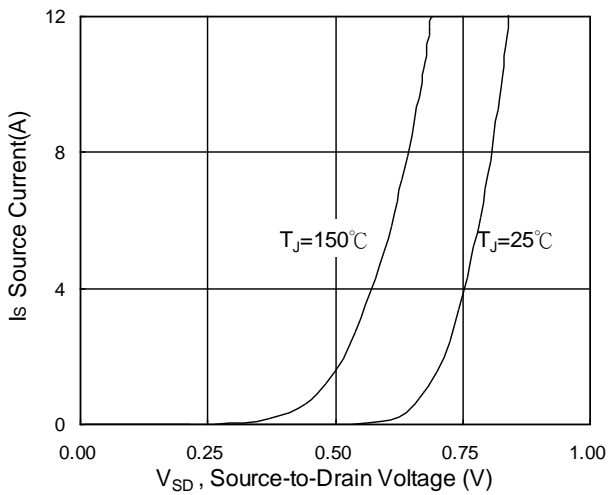


Fig.3 Forward Characteristics of Reverse

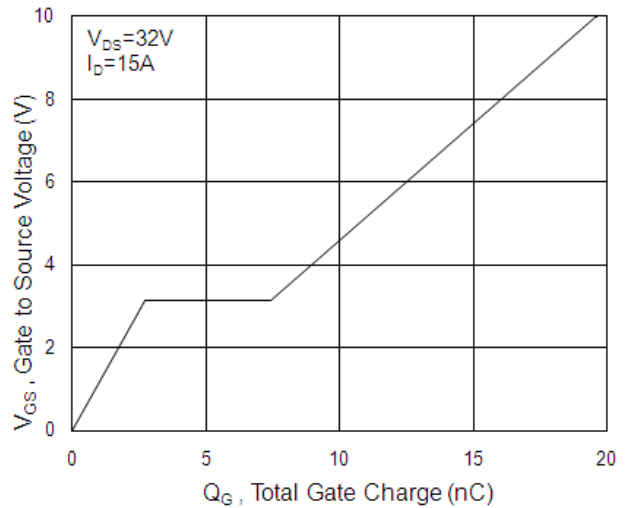


Fig.4 Gate-Charge Characteristics

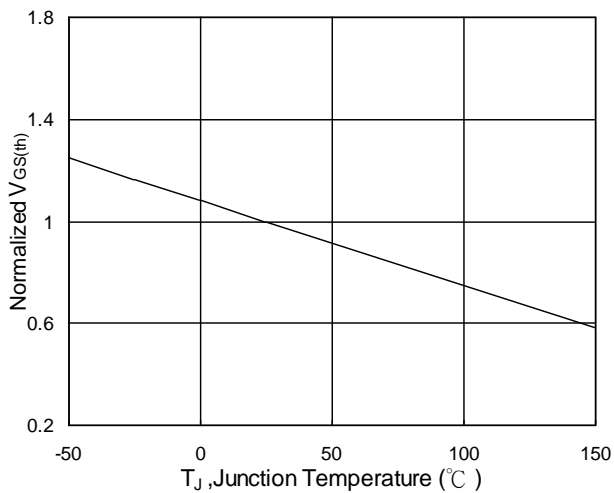


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

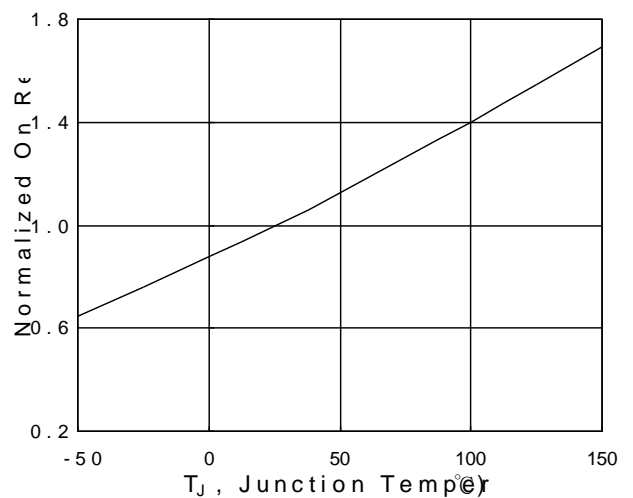


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

40V N+P-Channel Enhancement Mode MOSFET

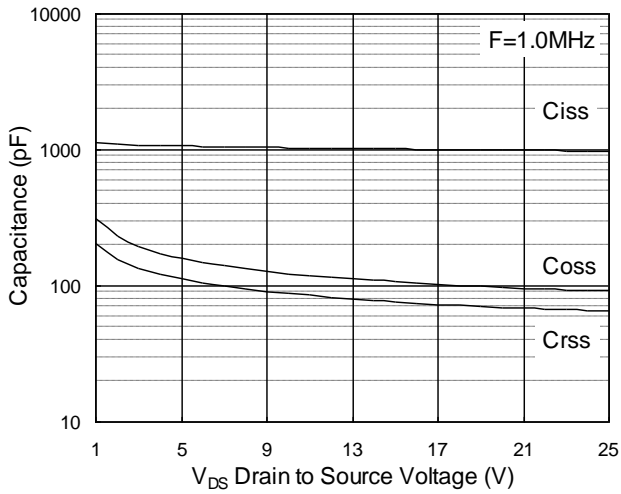


Fig.7 Capacitance

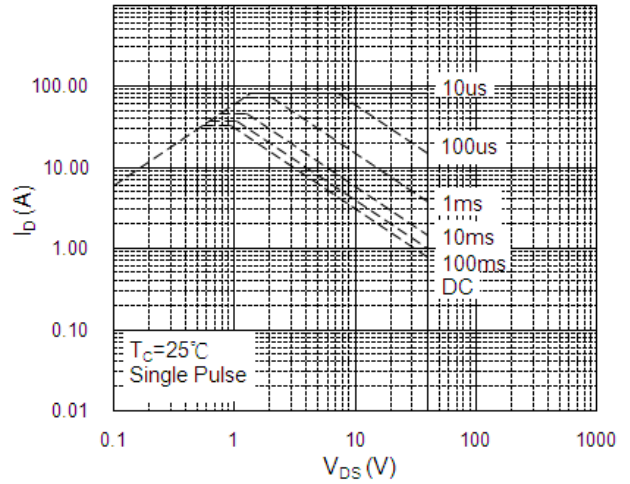


Fig.8 Safe Operating Area

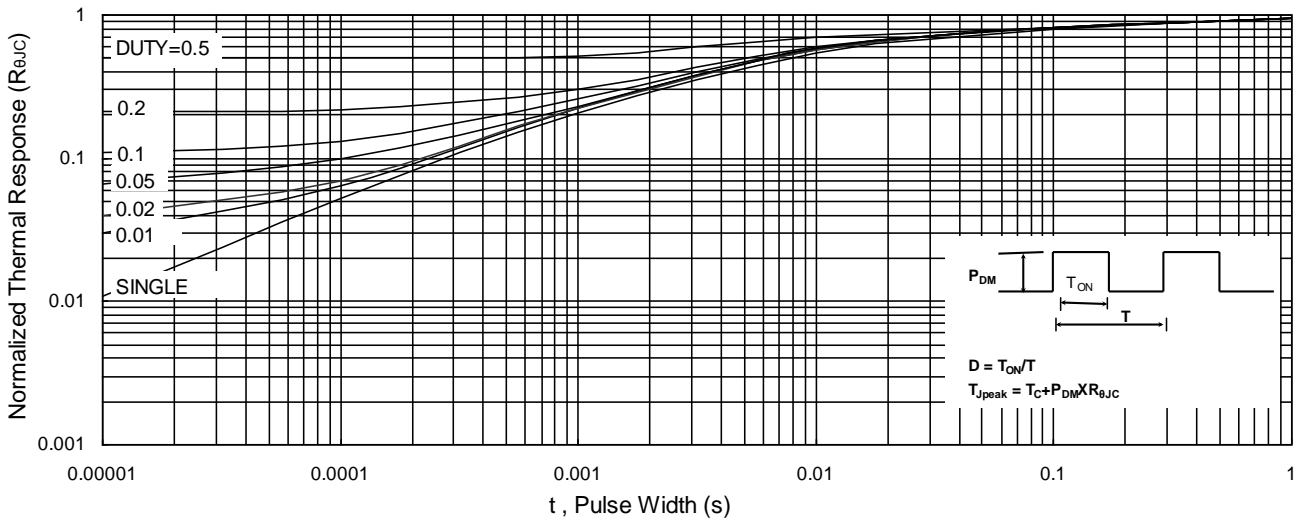


Fig.9 Normalized Maximum Transient Thermal Impedance

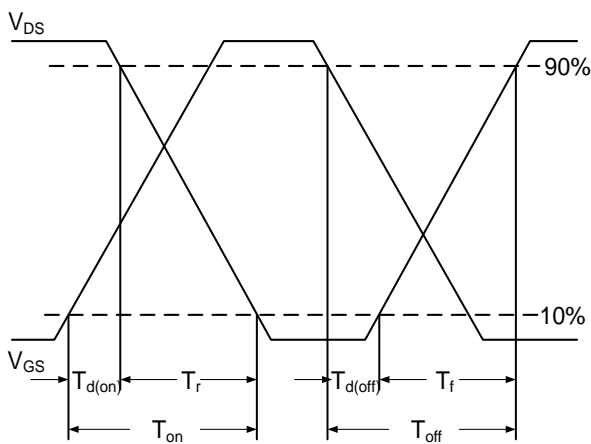


Fig.10 Switching Time Waveform

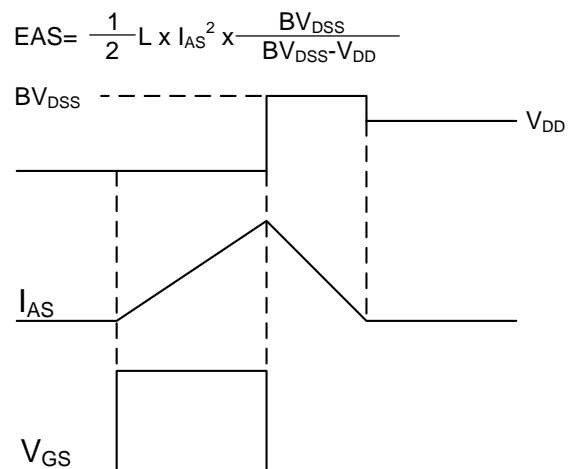


Fig.11 Unclamped Inductive Switching Waveform

P-Typical Characteristics

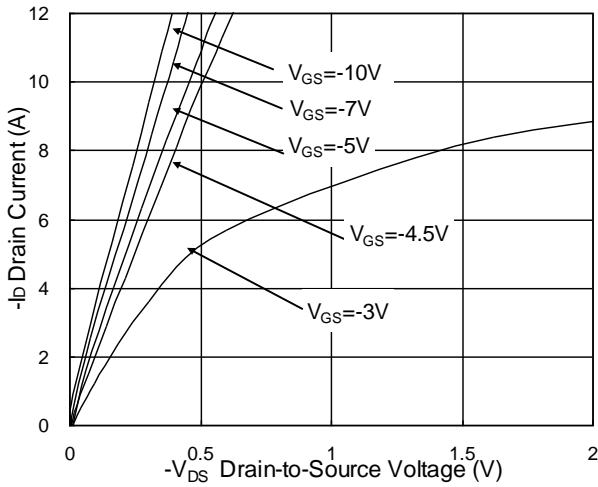


Fig.1 Typical Output Characteristics

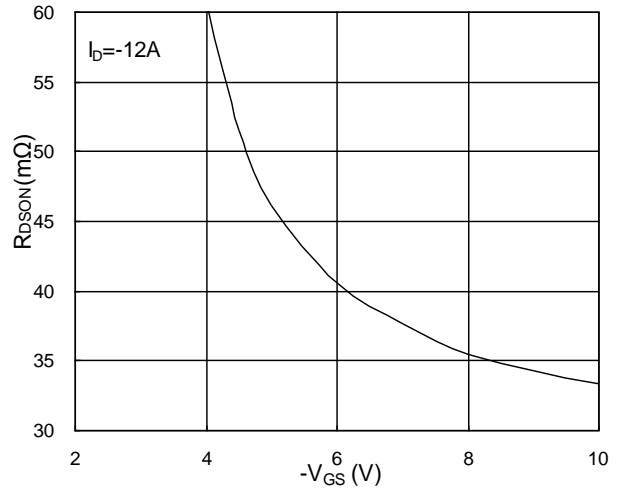


Fig.2 On-Resistance v.s Gate-Source

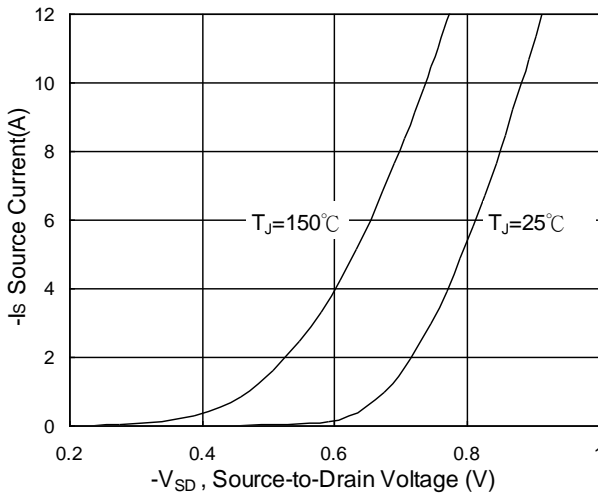


Fig.3 Forward Characteristics of Reverse

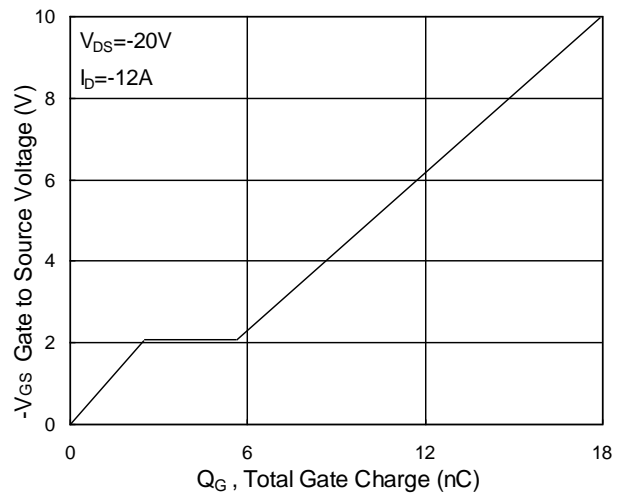


Fig.4 Gate-Charge Characteristics

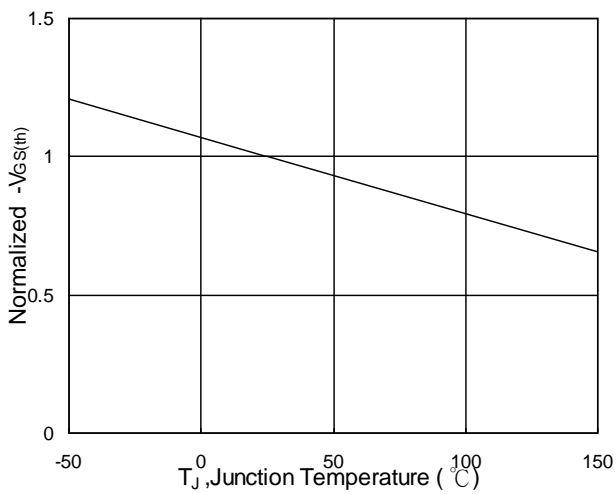


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

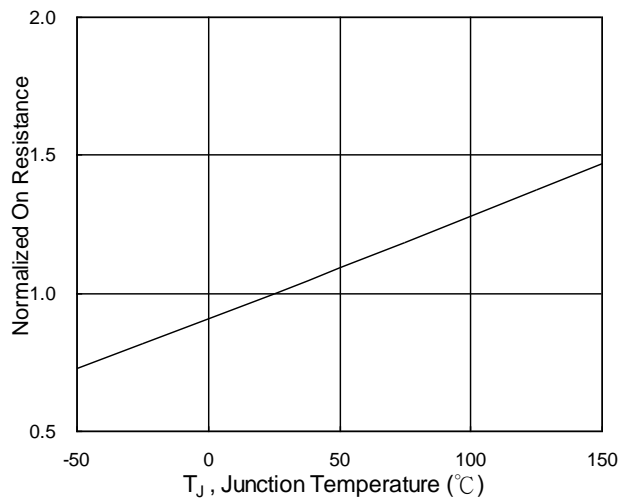


Fig.6 Normalized $R_{DS(on)}$ v.s T_J



40V N+P-Channel Enhancement Mode MOSFET

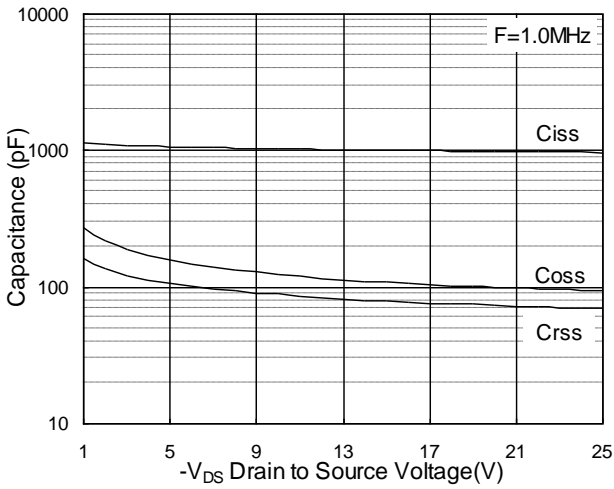


Fig.7 Capacitance

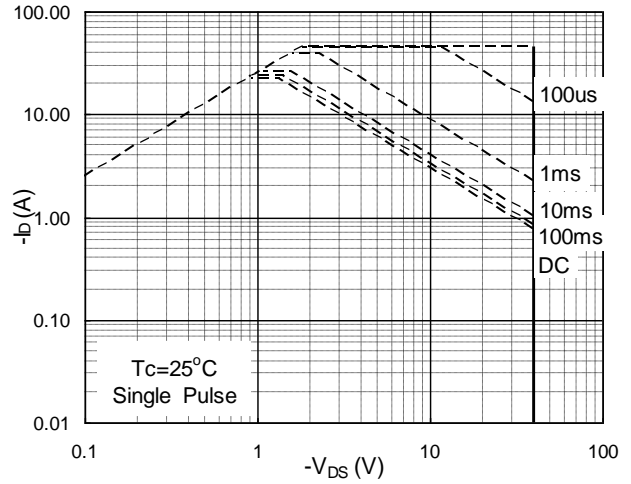


Fig.8 Safe Operating Area

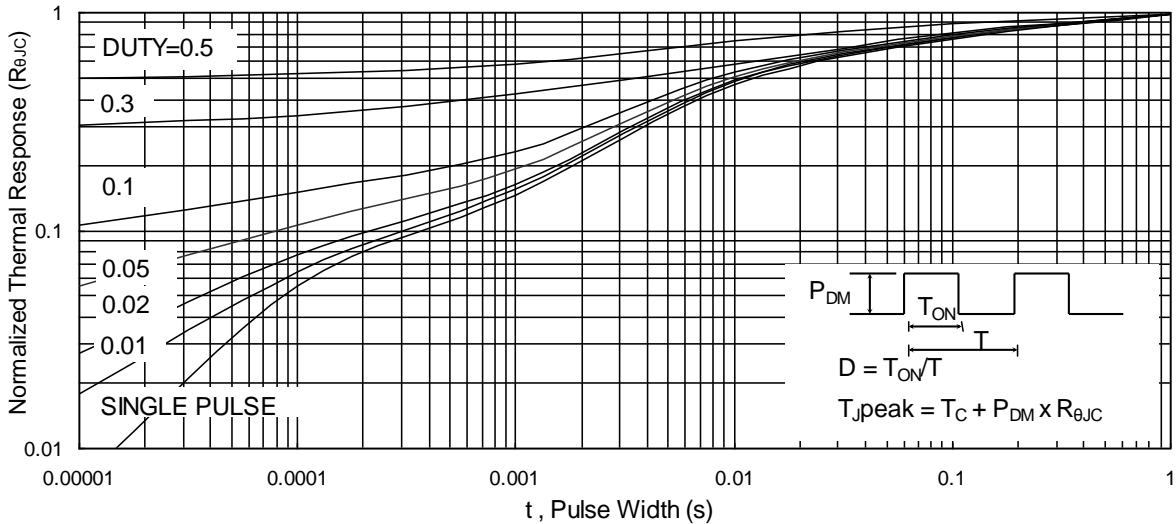


Fig.9 Normalized Maximum Transient Thermal Impedance

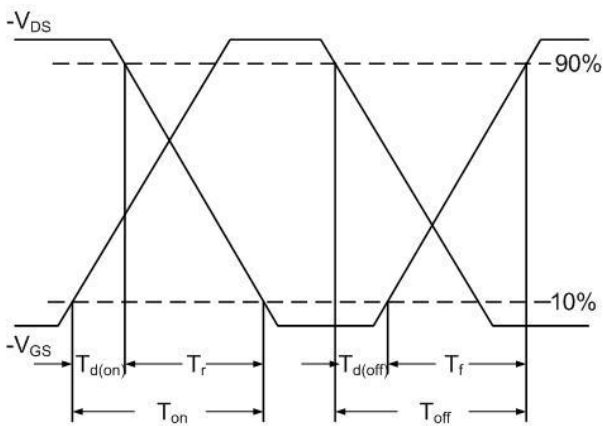


Fig.10 Switching Time Waveform

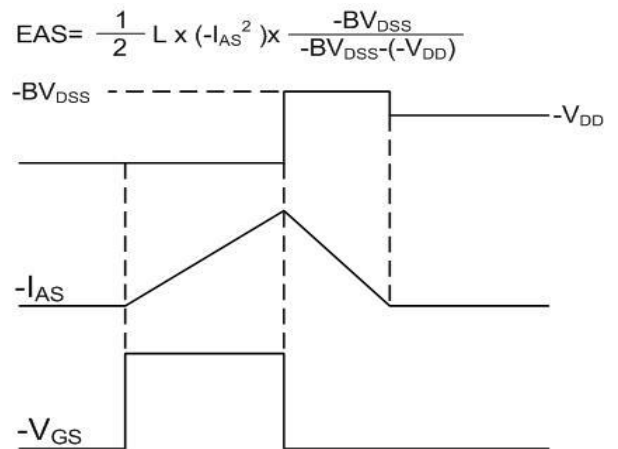
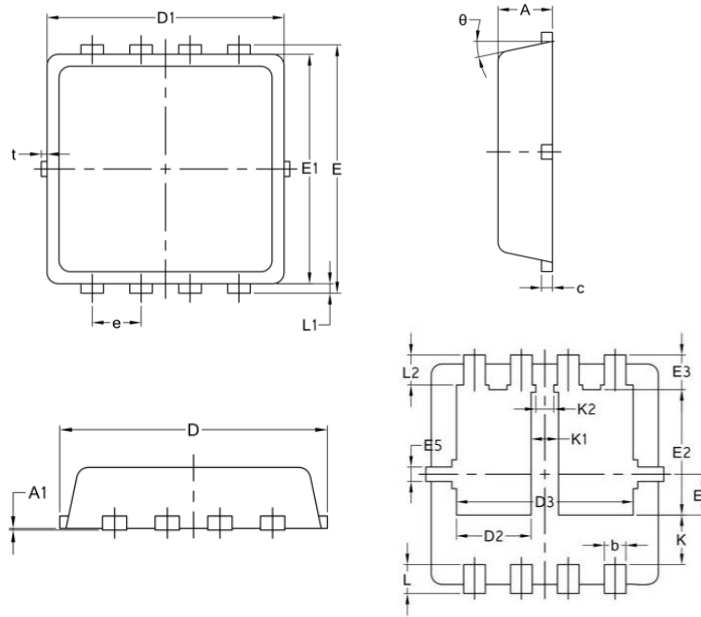


Fig.11 Unclamped Inductive Waveform



Package Mechanical Data-DFN3*3-8L-JQ Double



Symbol	Common		
	Mm		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
Φ	10°	12°	14°



40V N+P-Channel Enhancement Mode MOSFET**Attention**

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