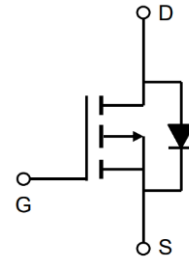


## 40V P-Channel Enhancement Mode MOSFET

### Description

The AP8P04S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = -40V$   $I_D = -8A$

$R_{DS(ON)} < 32m\Omega$  @  $V_{GS} = -10V$

### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8P04S	SOP-8L	AP8P04S XXX YYYYY	3000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-8	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-6.9	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-32	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	41	mJ
$I_{AS}$	Avalanche Current	-28.6	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>4</sup>	2.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	50	$^\circ C/W$

## 40V P-Channel Enhancement Mode MOSFET

### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

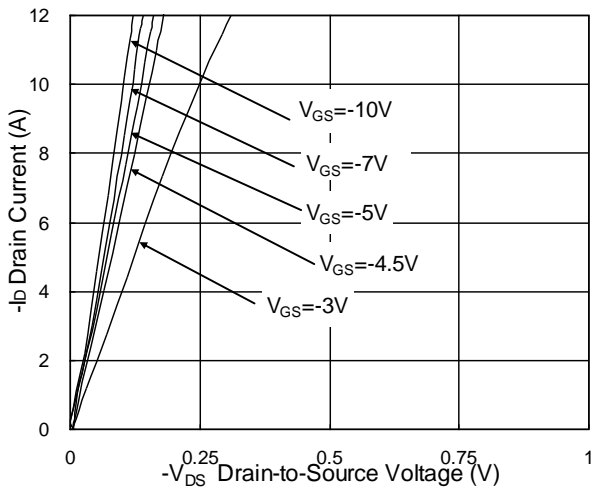
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-40	---	---	V
ΔBVDSS/ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.02	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5A	---	---	32	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A	---	---	46	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.2	---	-2.5	V
ΔVGS(th)	V <sub>GS(th)</sub> Temperature Coefficient		---	3.72	---	V/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	-1	uA
		V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-8A	---	10.7	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A	---	11.5	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	3.5	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	3.3	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-1A	---	22	---	ns
T <sub>r</sub>	Rise Time		---	15.7	---	
Td(off)	Turn-Off Delay Time		---	59	---	
T <sub>f</sub>	Fall Time		---	5.5	---	
Ciss	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	1415	---	pF
Coss	Output Capacitance		---	134	---	
Crss	Reverse Transfer Capacitance		---	102	---	
IS	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-8	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.2	V

#### Note :

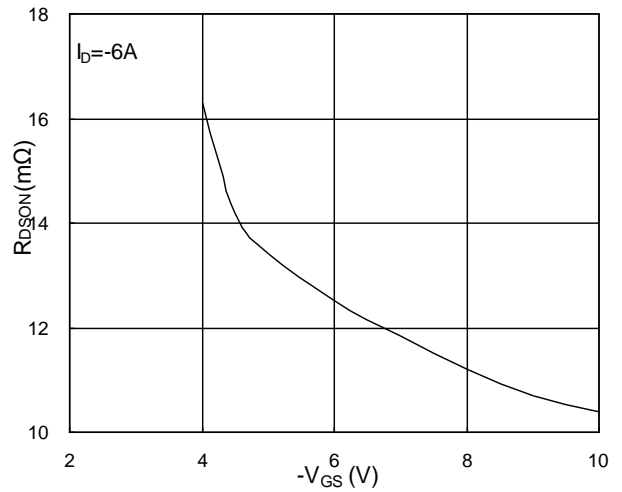
- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is V DD =-25V,V GS =-10V,L=0.1mH,I AS =-28.6A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

**40V P-Channel Enhancement Mode MOSFET**

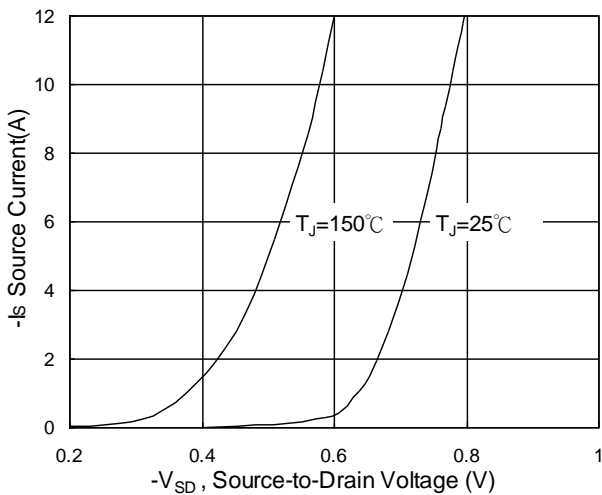
**Typical Characteristics**



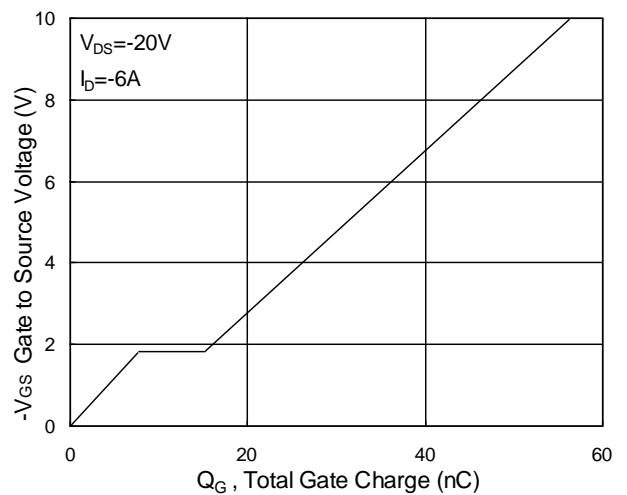
**Fig.1 Typical Output Characteristics**



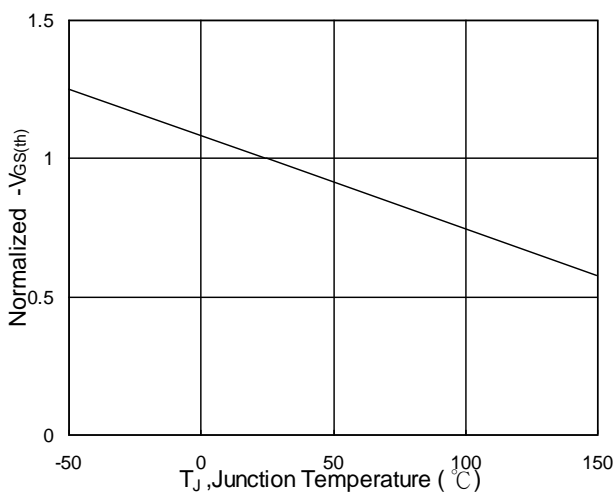
**Fig.2 On-Resistance v.s Gate-Source**



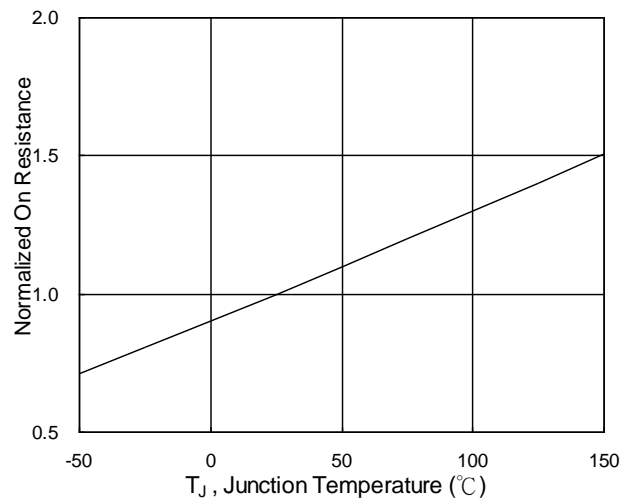
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**



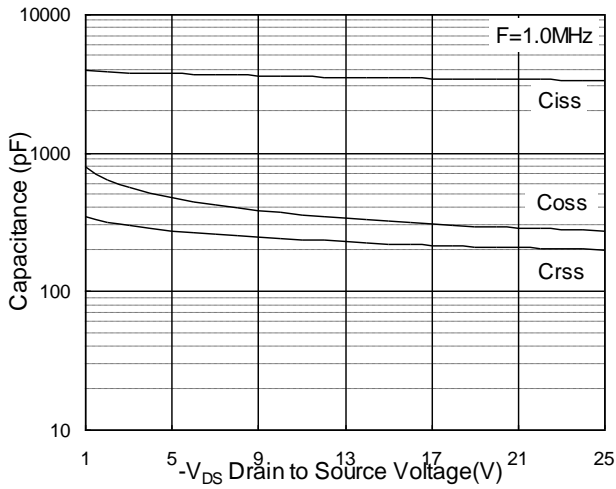
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



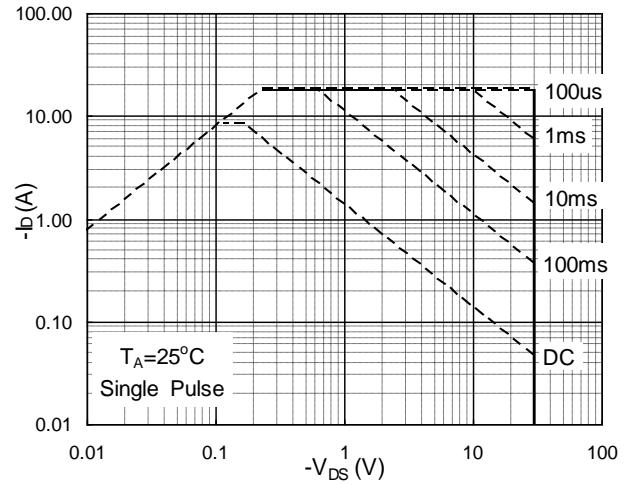
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



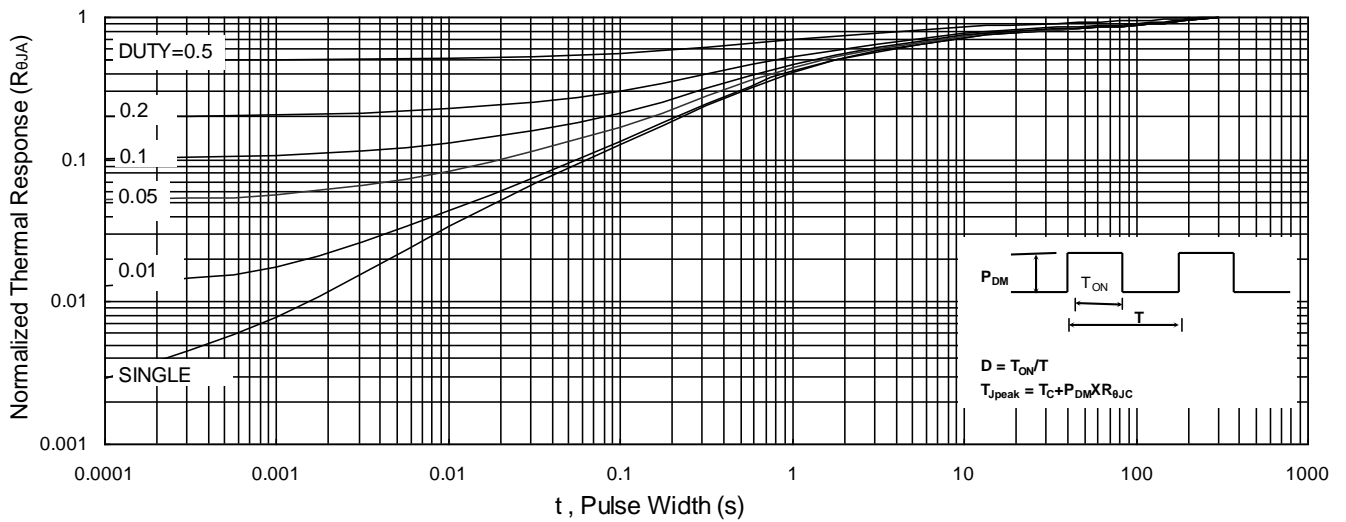
**40V P-Channel Enhancement Mode MOSFET**



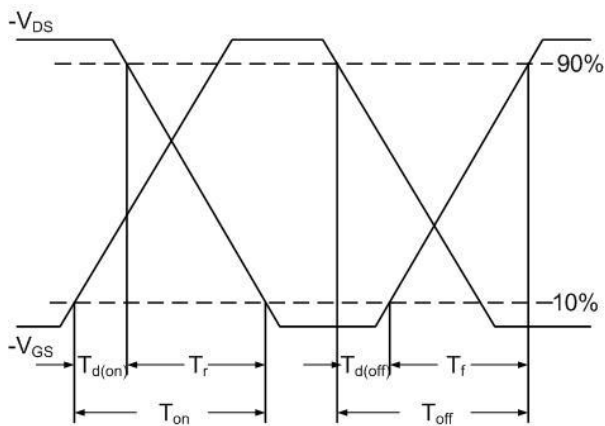
**Fig.7 Capacitance**



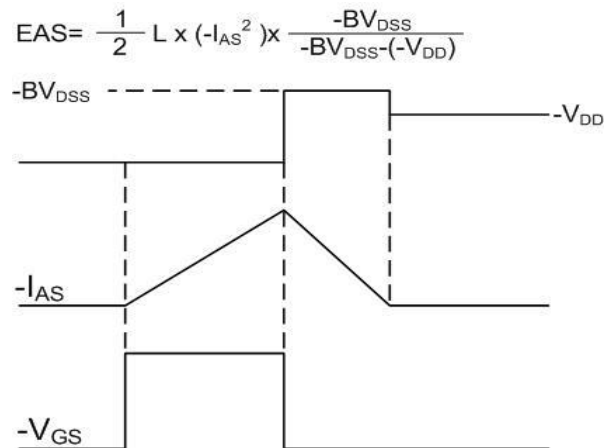
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

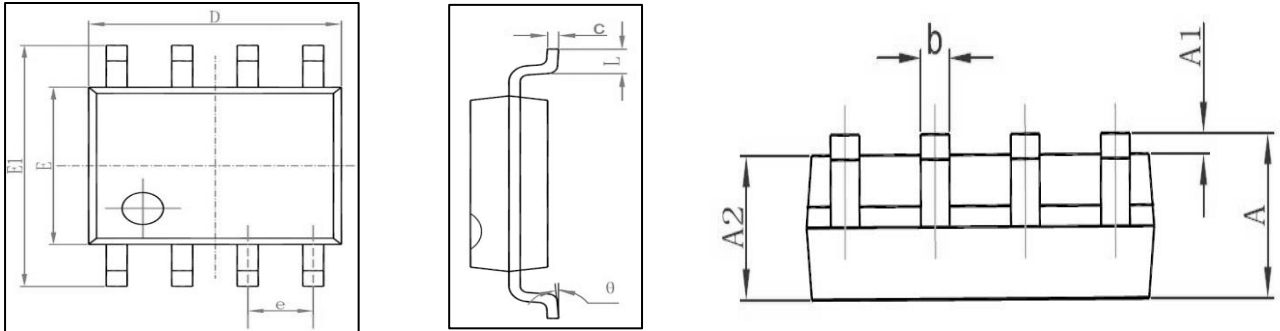


**Fig.10 Switching Time Waveform**

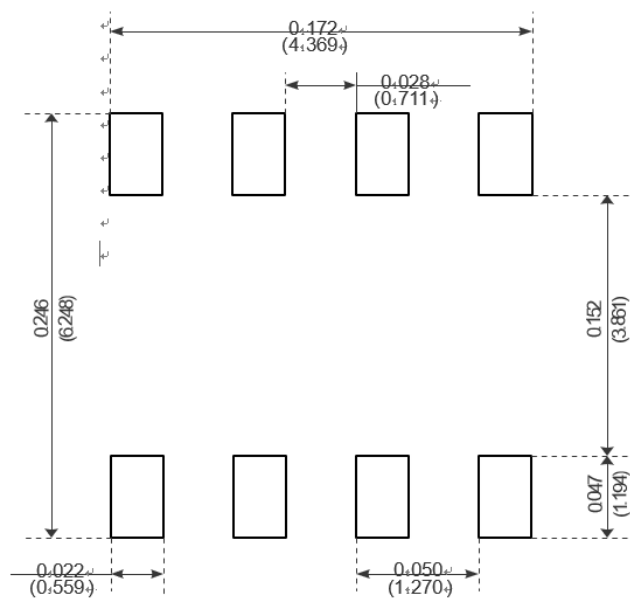


**Fig.11 Unclamped Inductive Waveform**

### Package Mechanical Data-SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

**40V P-Channel Enhancement Mode MOSFET****Attention**

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**40V P-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2020/12/14	Initial release

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