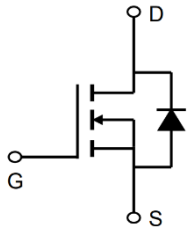
AP130N20MP

200V N-Channel Enhancement Mode MOSFET

Description

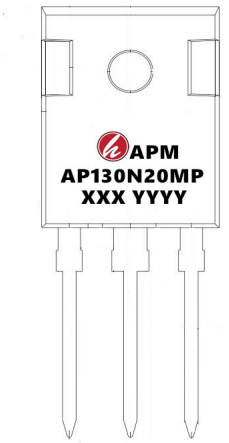
The AP130N20P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

VDS =200V,ID =130A

RDS(ON) <23mΩ@ VGS=10V



Application

Power amplifier

motor drive

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP130N20P	TO-247-3 Plus	AP130N20P XXX YYYY	600

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS} = 0V)	V_{DSS}	200	V
Continuous Drain Current	I_D	130	A
Pulsed Drain Current (note1)	I_{DM}	360	A
Gate-Source Voltage	V_{GSS}	±30	V
Single Pulse Avalanche Energy (note2)	E_{AS}	2000	mJ
Avalanche Current (note1)	I_{AR}	30	A
Repetitive Avalanche Energy (note1)	E_{AR}	25	mJ
Power Dissipation (T_C = 25ºC)	P_D	450	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150	ºC
Thermal Resistance, Junction-to-Case	R_{thJC}	0.28	ºC/W
Thermal Resistance, Junction-to-Ambient	R_{thJA}	60	

200V N-Channel Enhancement Mode MOSFET

Electrical Characteristics at T_j=25 ℃ unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	200	--	--	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} = 200V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
IGSS	Gate-Source Leakage	V_{GS} = ±20V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V_{GS} = 10V, I_D = 45A	--	18	23	mΩ
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	6500	--	pF
C_{oss}	Output Capacitance		--	980	--	
C_{rss}	Reverse Transfer Capacitance		--	370	--	
Q_g	Total Gate Charge	V_{DD} = 160V, I_D = 90A, V_{GS} = 10V	--	200	--	nC
Q_{gs}	Gate-Source Charge		--	28	--	
Q_{gd}	Gate-Drain Charge		--	60	--	
td(on)	Turn-on Delay Time	V_{DD} = 100V, I_D = 90A, R_G = 25 Ω	--	45	--	ns
t_r	Turn-on Rise Time		--	70	--	
td(off)	Turn-off Delay Time		--	110	--	
t_f	Turn-off Fall Time		--	90	--	
IS	Continuous Body Diode Current	T_C = 25 ºC	--	--	90	A
ISM	Pulsed Diode Forward Current		--	--	360	
V_{SD}	Body Diode Voltage	T_J = 25ºC, I_{SD} = 90A, V_{GS} = 0V	--	--	1.4	V
trr	Reverse Recovery Time	V_{GS} = 0V,I_S = 90A, di_F/dt =100A /μs	--	280	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.4	--	μC

Notes

1、Repetitive Rating: Pulse width limited by maximum junction temperature

2、I_{AS} = 30A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 ºC

3、Pulse Test: Pulse

Electrical Characteristics Diagrams

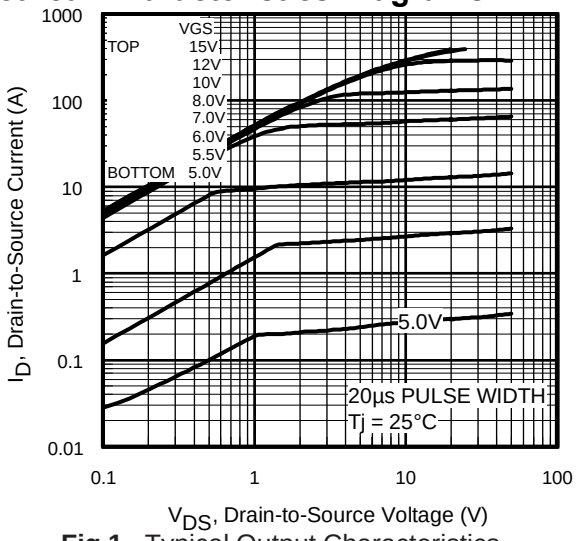


Fig 1. Typical Output Characteristics

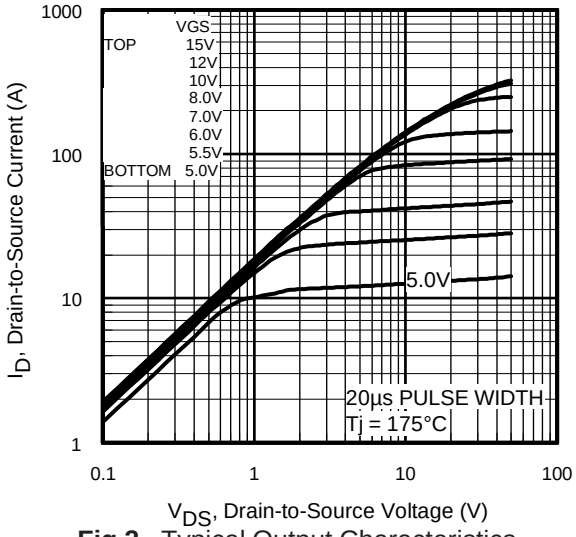


Fig 2. Typical Output Characteristics

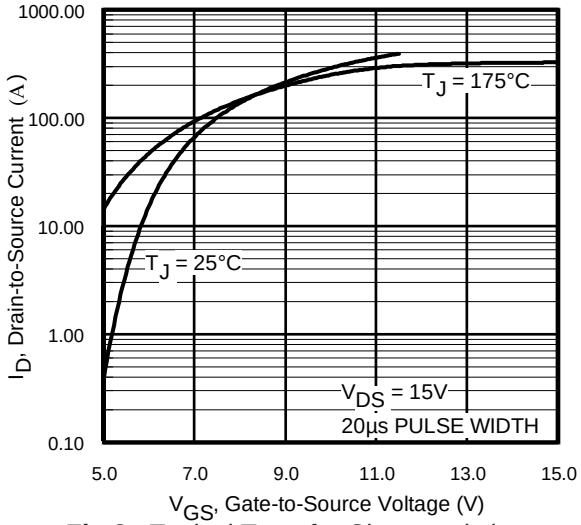


Fig 3. Typical Transfer Characteristics

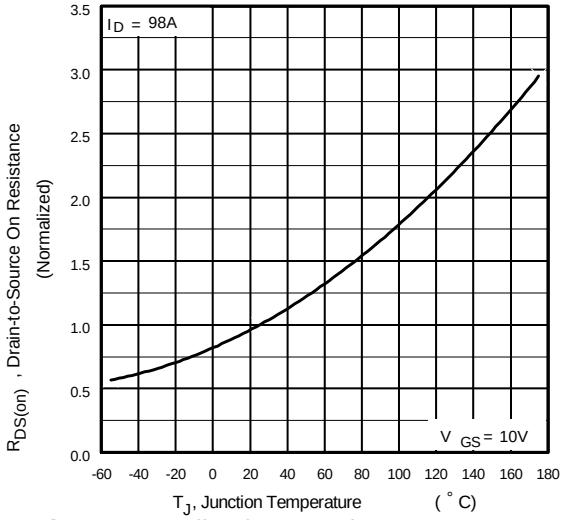


Fig 4. Normalized On-Resistance Vs. Temperature

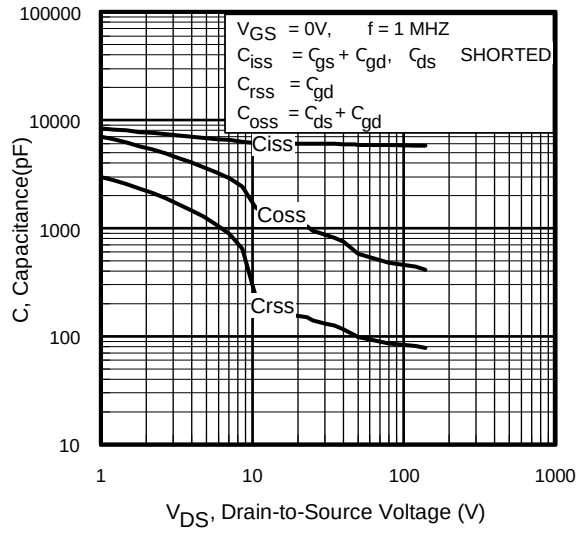


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

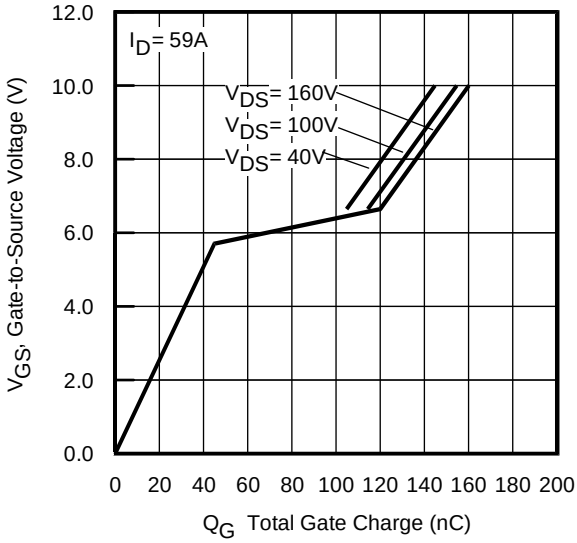


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

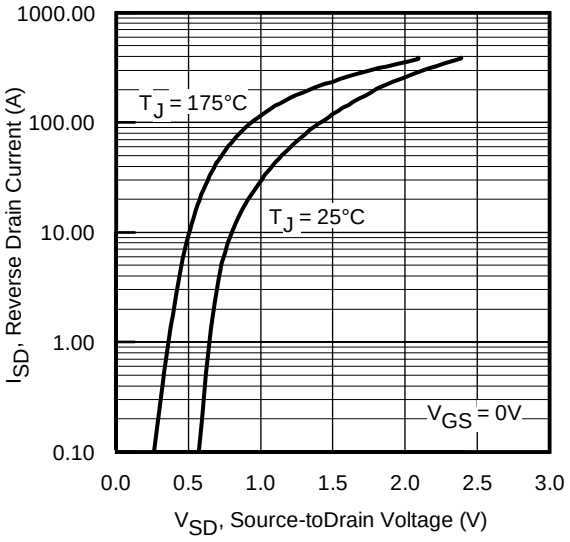


Fig 7. Typical Source-Drain Diode Forward Voltage

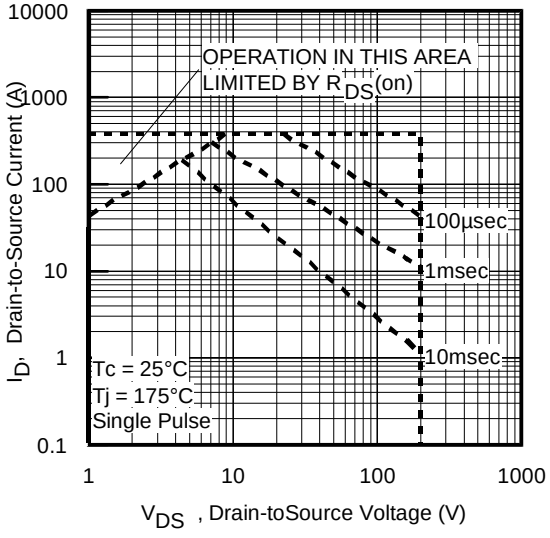


Fig 8. Maximum Safe Operating Area

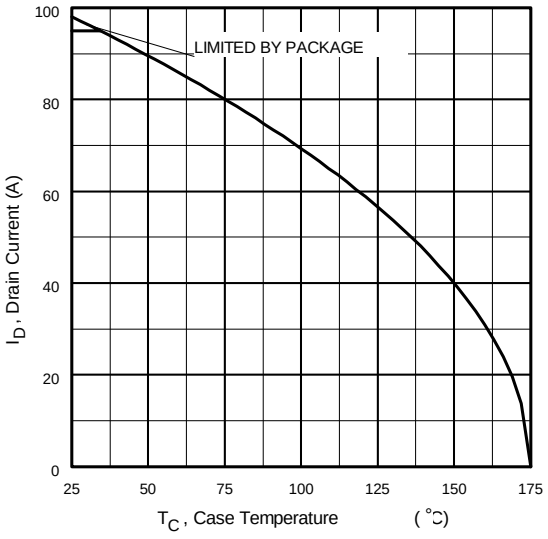


Fig 9. Maximum Drain Current Vs. Case Temperature

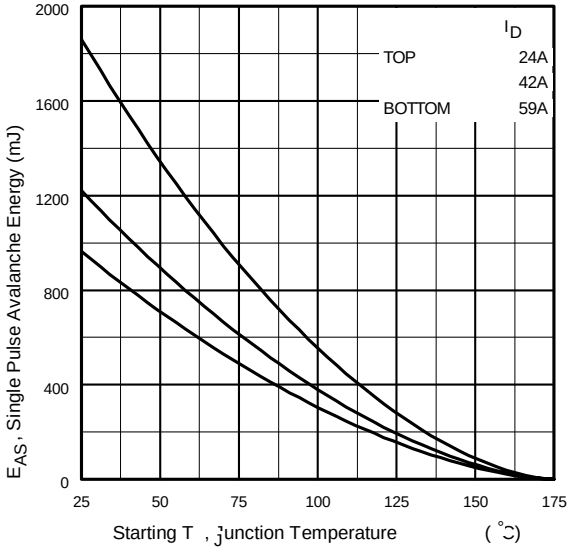


Fig 10. Maximum Avalanche Energy Vs. Drain Current

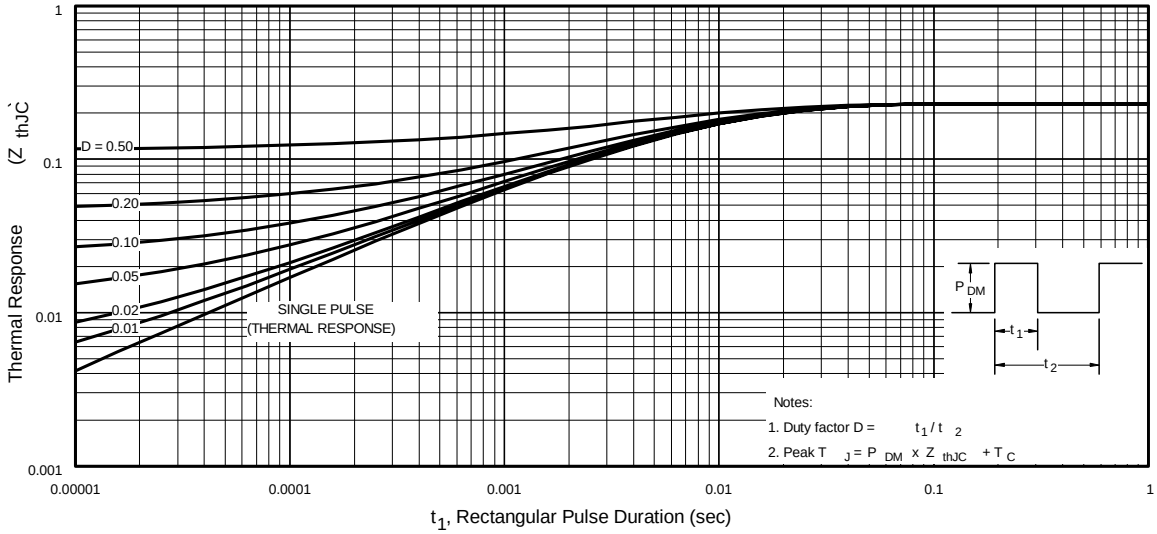
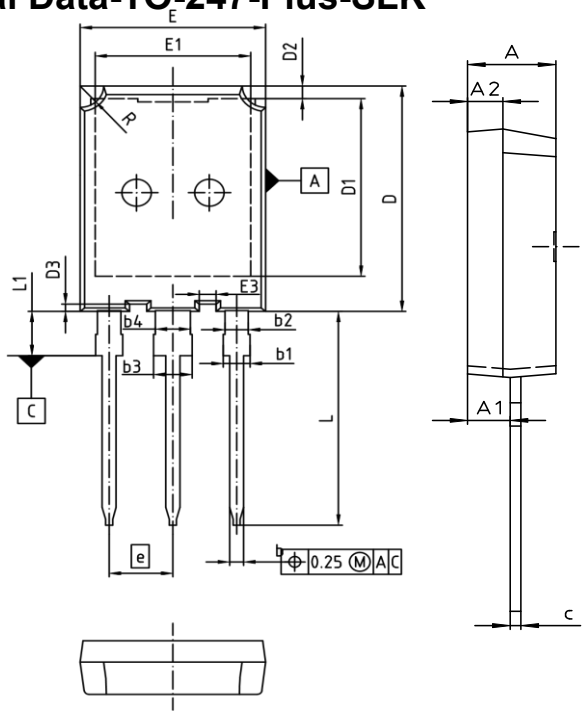


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-TO-247-Plus-SLK



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.201
A1	2.31	2.51	0.091	0.099
A2	1.90	2.10	0.075	0.083
b	1.16	1.26	0.046	0.050
b1	1.96	2.25	0.077	0.089
b2	1.96	2.06	0.077	0.081
c	0.59	0.66	0.023	0.026
D	20.90	21.10	0.823	0.831
D1	16.25	16.85	0.640	0.663
D2	1.05	1.35	0.041	0.053
D3	0.58	0.78	0.023	0.031
E	15.70	15.90	0.618	0.626
E1	13.10	13.50	0.516	0.531
E3	1.35	1.55	0.053	0.061
e	5.44 (BSC)		0.214 (BSC)	
N	3		3	
L	19.80	20.10	0.780	0.791
L1	-	4.30	-	0.169
R	1.90	2.10	0.075	0.083

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