

### **Description**

The AP120N04P/T uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a

Battery protection or in other Switching application.

#### **General Features**

V<sub>DS</sub> = 40V I<sub>D</sub> =120 A

 $R_{DS(ON)}$  < 4.0m $\Omega$  @  $V_{GS}$ =10V

#### **Application**

Battery protection

Load switch

Uninterruptible power supply



# Package Marking and Ordering Information

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Product ID	Pack	Marking	Qty(PCS)
AP120N04P	TO-220-3L	AP120N04P XXX YYYY	10 00
AP120N04T	TO-263-3L	AP120N04T XXX YYYY	800

### Absolute Maximum Ratings (T<sub>C</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	40	V
Vgs	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1,6</sup>	120	А
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1,6</sup>	98	Α
Ідм	Pulsed Drain Current <sup>2</sup>	600	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	272	mJ
las	Avalanche Current	33	Α
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	180	W
Тѕтс	Storage Temperature Range	-55 to 150	℃
TJ	Operating Junction Temperature Range	-55 to 150	°C
R <sub>θ</sub> JA	Thermal Resistance Junction-Ambient <sup>1</sup>	50	°C/W
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	0.7	°C/W





# AP120N04P/T

### **40V N-Channel Enhancement Mode MOSFET**

Electrical Characteristics (TJ=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	44	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V,	-	-	1.0	μΑ
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0	2.8	4.0	V
RDS(on)	Static Drain-Source on-Resistance note3	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	3.0	4.0	mΩ
Ciss	Input Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1.0MHz	-	4900	-	pF
Coss	Output Capacitance		-	528	-	pF
Crss	Reverse Transfer Capacitance		-	317	-	pF
Qg	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	80	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	17	-	nC
$Q_gd$	Gate-Drain("Miller") Charge		-	21	-	nC
td(on)	Turn-on Delay Time		-	21	-	ns
t <sub>r</sub>	Turn-on Rise Time	$V_{DD}$ =20V, $I_{D}$ =30A, $R_{L}$ =1 $\Omega$ , $R_{GEN}$ =3 $\Omega$ ,	ı	32	•	ns
td(off)	Turn-off Delay Time	V <sub>GS</sub> =10V	-	71	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	40	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	150	Α
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	600	Α
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =30A	-	-	1.2	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T <sub>J</sub> =25℃, I <sub>F</sub> =20A,dI/dt=100A/μs	ı	27	ı	ns
Qrr	Body Diode Reverse Recovery Charge		-	46	-	nC

#### Note:

- 1、Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
- 2. The EAS data shows Max. rating . The test condition is T<sub>J</sub>=25  $^{\circ}$ C,V<sub>DD</sub>=20V,V<sub>G</sub>=10V,L=0.5mH,Rg=25 $\Omega$ ,I<sub>AS</sub>=33A
- 3. The data tested by pulsed , pulse width  $\leq 300 \text{us}$  , duty cycle  $\leq 2\%$
- 4. The power dissipation is limited by 150 °C junction temperature
- $5\sqrt{100}$  The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.
- 6. Package limitation current is 180A



### **Typical Characteristics**

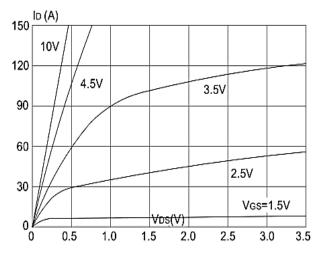
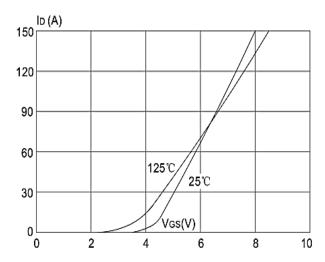


Figure1: Output Characteristics



**Figure 2: Typical Transfer Characteristics** 

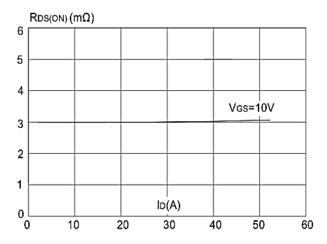
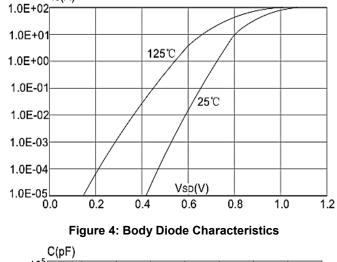


Figure 3:On-resistance vs. Drain Current



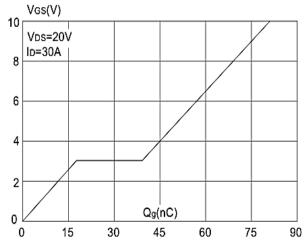


Figure 5: Gate Charge Characteristics

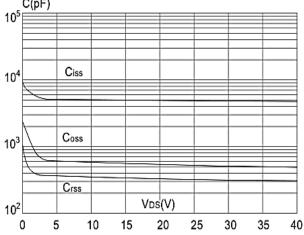


Figure 6: Capacitance Characteristics



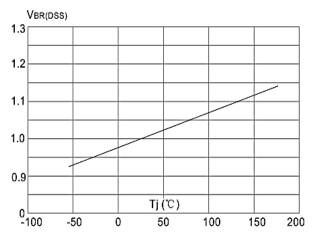


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

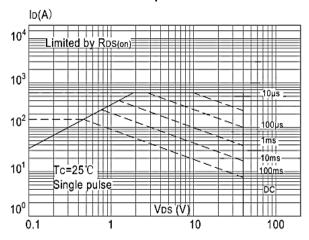


Figure 9: Maximum Safe Operating Area

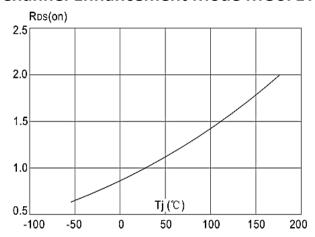


Figure 8: Normalized on Resistance vs.

Junction Temperature

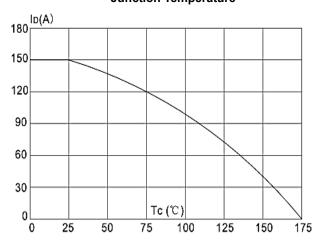


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

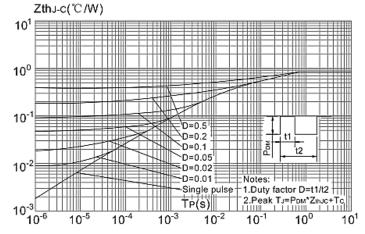
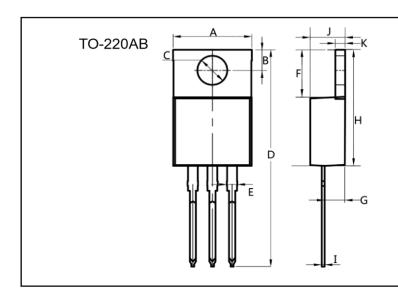
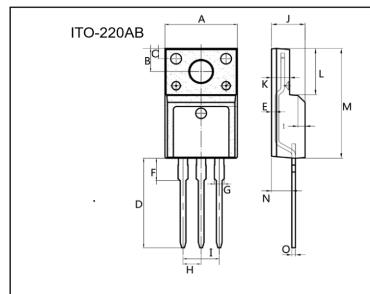


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

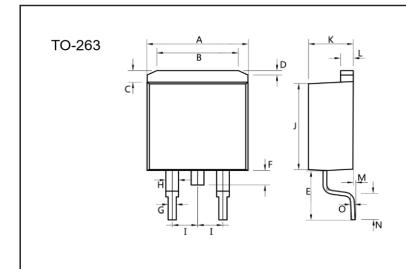




Dim.	Min.	Max.
Α	10.0	10.4
В	2.5	3.0
С	3.5	4.0
D	28.0	30.0
Е	1.1	1.5
F	6.2	6.6
G	2.9	3.3
Н	15.0	16.0
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
All Dimensions in millimeter		



Min.	Max.	
9.9	10.3	
2.9	3.5	
1.15	1.45	
12.75	13.25	
0.55	0.75	
3.1	3.5	
1.25	1.45	
Typ 2.54		
Typ 5.08		
4.55	4.75	
2.4	2. 7	
6.35	6.75	
15.0	16.0	
2.75	3.15	
0.45	0.60	
All Dimensions in millimeter		
	9.9 2.9 1.15 12.75 0.55 3.1 1.25 Typ Typ 4.55 2.4 6.35 15.0 2.75 0.45	



Dim.	Min.   Max.		
Α	10.0	10. 5	
В	7.25	7.75	
С	1.3	1.5	
D	0.55	0.75	
E	5.0	6.0	
F	1.4	1.6	
G	0.75	0.95	
Н	1.15	1.35	
ı	Typ 2.54		
J	8.4	8.6	
K	4.4	4.6	
L	1.25	1.45	
М	0.02	0.1	
N	2.4	2.8	
О	0.35	0.45	
All Dimensions in millimeter			
All Dim	ensions in m	llimeter	





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# AP120N04P/T

# **40V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2020/4/1	Initial release

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