

100V N-Channel Enhancement Mode MOSFET

Description

The AP5N10BI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 100V$ $I_D = 5A$

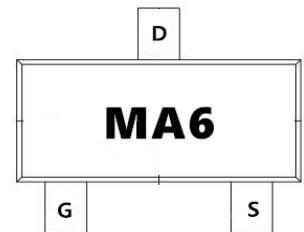
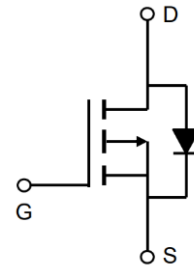
$R_{DS(ON)} < 125m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N10BI	SOT-23	MA6	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_A=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5	A
$I_D @ T_A=70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.2	A
I_{DM}	Pulsed Drain Current ²	16	A
$P_D @ T_A=25^{\circ}C$	Total Power Dissipation ³	3.1	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient(steady state) ¹	100	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance Junction-ambient($t < 10s$) ¹	40	$^{\circ}C/W$

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Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

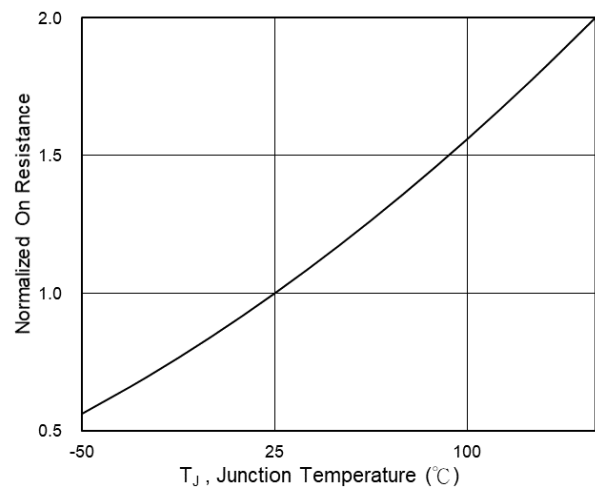
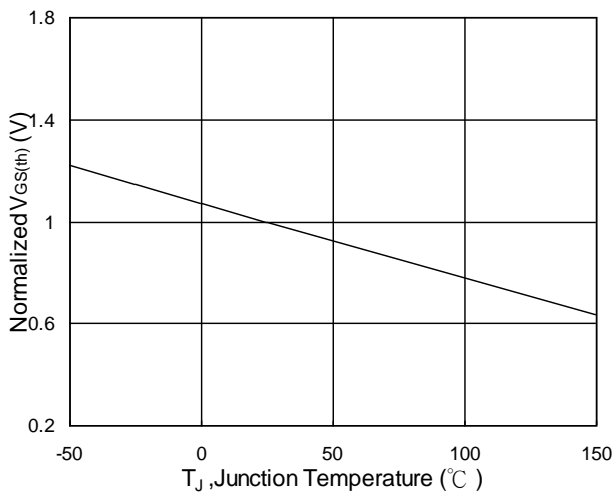
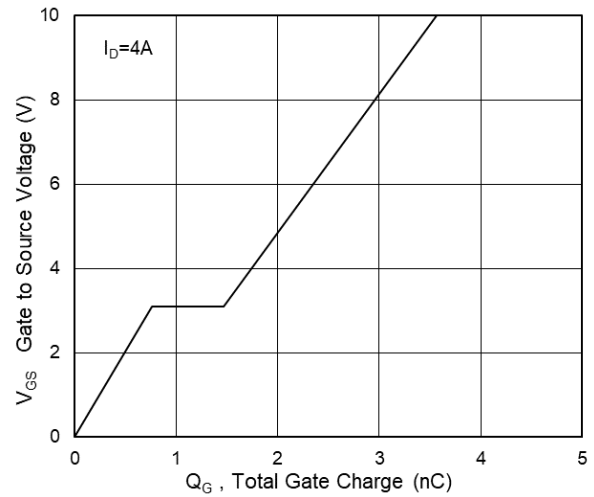
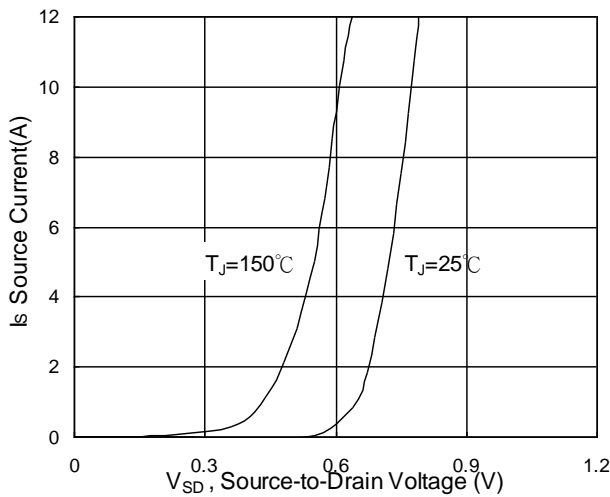
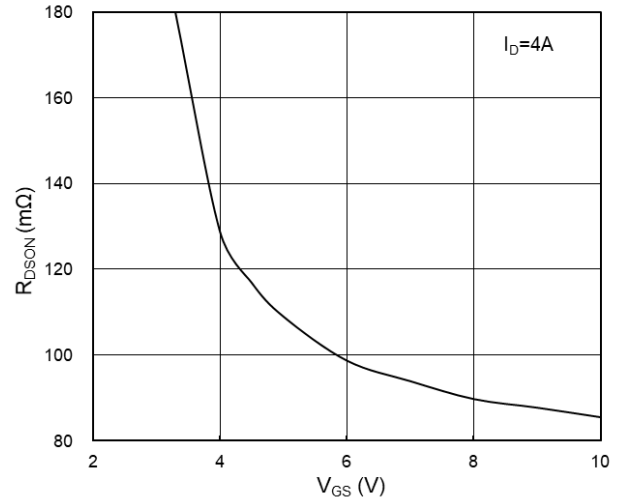
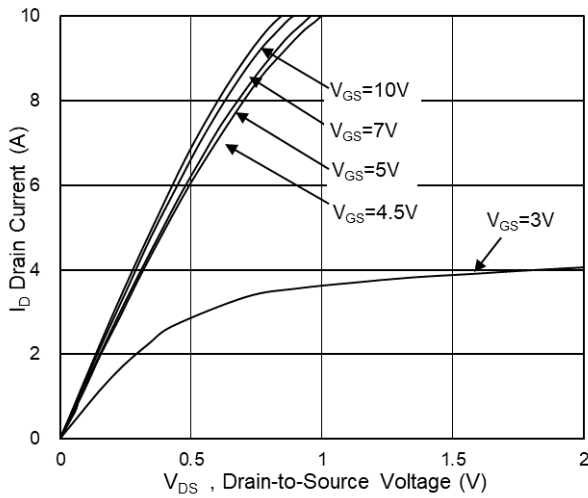
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	100	108	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=4A$	---	105	125	m Ω
		$V_{GS}=4.5V$, $I_D=2A$	---	120	145	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.2	1.7	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=80V$, $V_{GS}=0V$, $T_J=85^{\circ}\text{C}$	---	---	50	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	2.3	4.6	
Q_g	Total Gate Charge (10V)	$V_{DS}=30V$, $V_{GS}=10V$, $I_D=4A$	---	3.57	---	nC
Q_{gs}	Gate-Source Charge		---	0.76	---	
Q_{gd}	Gate-Drain Charge		---	0.71	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V$, $V_{GS}=10V$, $R_G=3.3$ $I_D=1A$	---	11	---	ns
T_r	Rise Time		---	6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	30	---	
T_f	Fall Time		---	4	---	
C_{iss}	Input Capacitance	$V_{DS}=50V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	182	---	pF
C_{oss}	Output Capacitance		---	30	---	
C_{rss}	Reverse Transfer Capacitance		---	3.6	---	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	2	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics



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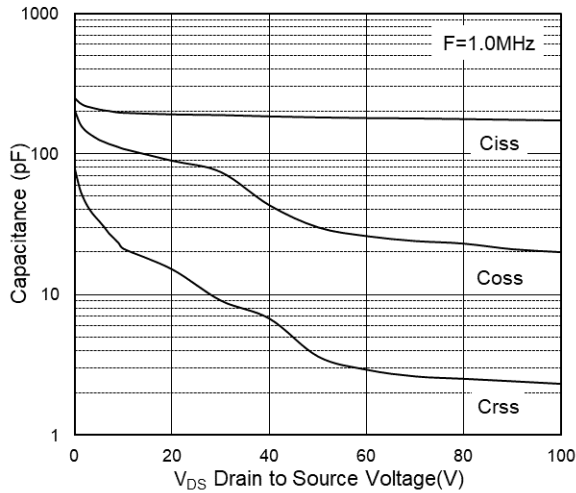


Fig.7 Capacitance

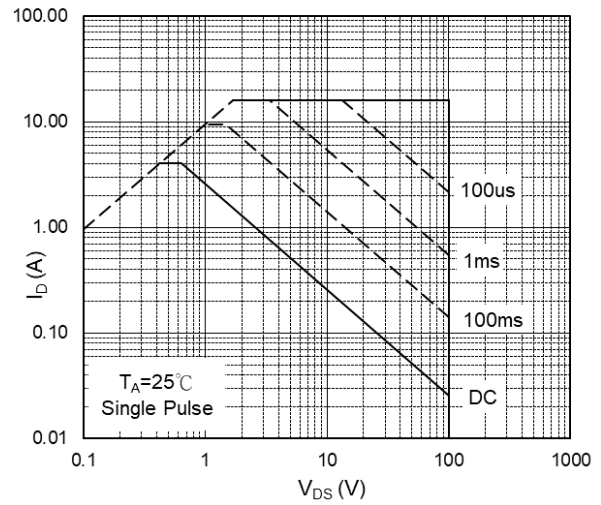


Fig.8 Safe Operating Area

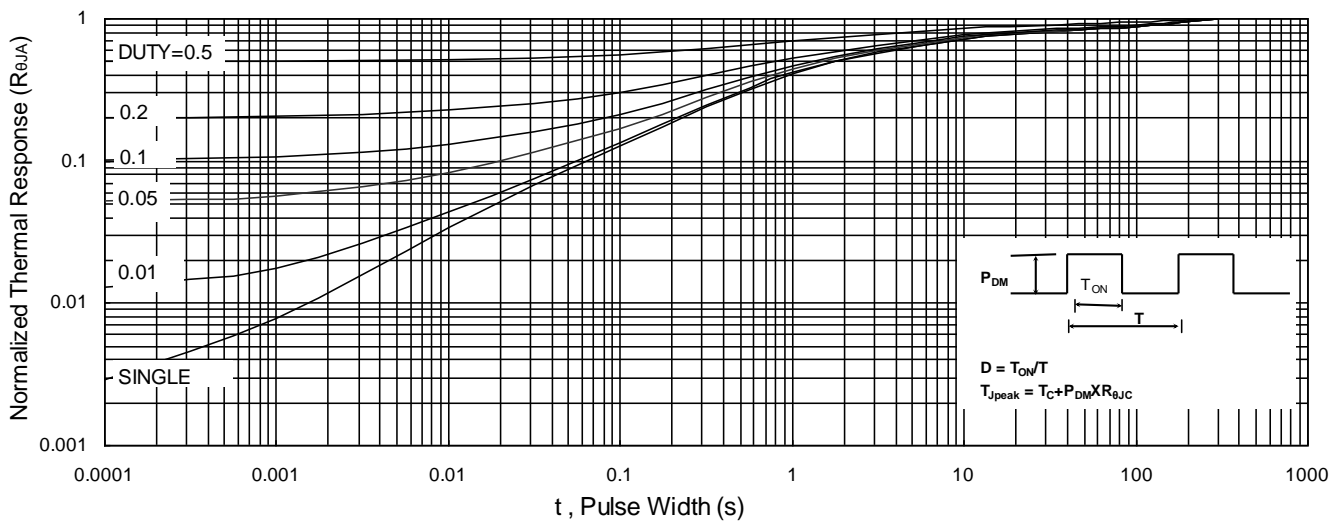


Fig.9 Normalized Maximum Transient Thermal Impedance

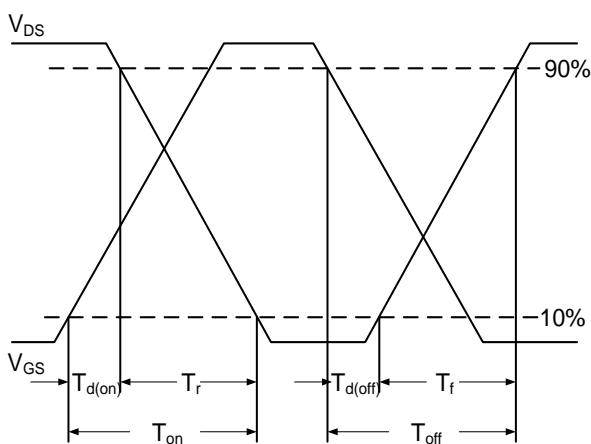


Fig.10 Switching Time Waveform

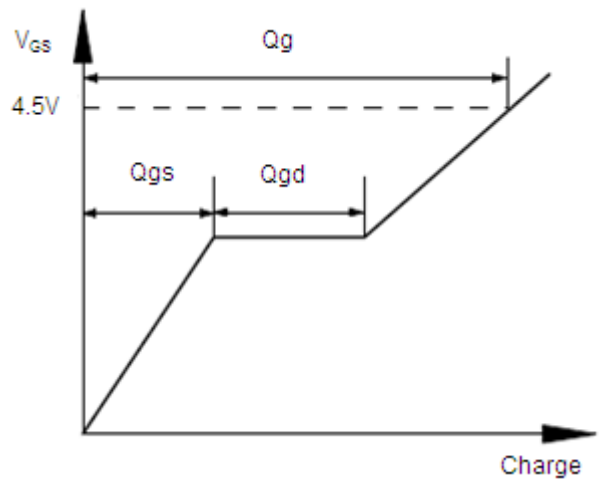
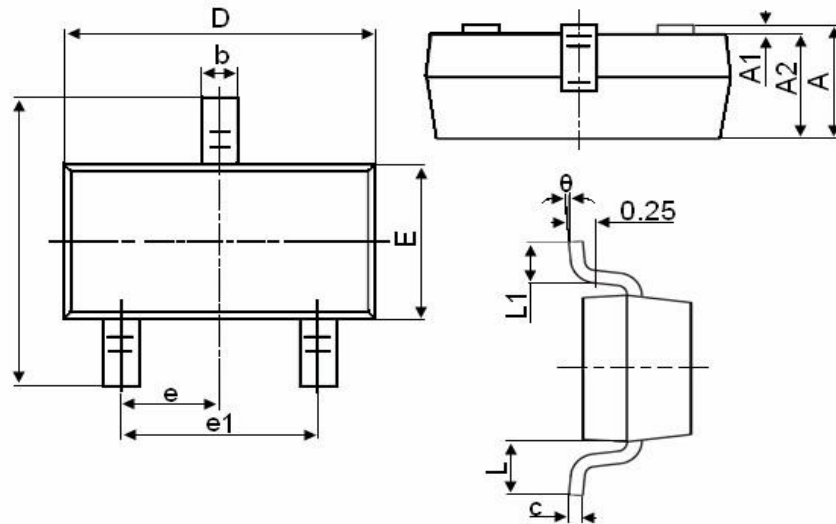


Fig.11 Gate Charge Waveform

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Package Mechanical Data-SOT-23



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

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AP5N10BI**100V N-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2020/9/9	Initial release

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