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RTL8364NB-VB-CG

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LAYER 2 MANAGED 2+2-PORT 10/100/1000M SWITCH CONTROLLER

DRAFT DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8364NB-VB IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.1	2016/07/15	First draft version.
0.2	2017/06/22	Revise some errors.
0.3	2017/11/03	Revise RMII Clock Input/Output Mode description error

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1. General Description

The RTL8364NB-VB is a QFN88, high-performance 2+2-port 10/100/1000M Ethernet switch featuring low-power integrated dual-port 10/100/1000M PHYs that support 1000Base-T, 100Base-TX, and 10Base-T.

The embedded packet storage SRAM in the RTL8364NB-VB features superior memory management technology to efficiently utilize memory space. The RTL8364NB-VB integrates a 2048-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the Slave I^2C-like serial Interface, Slave Media Independent Interface Management (MIIM) Interface, or Salve SPI Interface. Each of the entries can be configured as a static entry. Normal entry aging time is between 200 and 400 seconds. Sixteen Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB implements GMII/RGMII/MII/TMII/RMII/1000Base-X/100FX/SGMII/HSGMII interface. These interfaces could be connected to an external PHY, MAC, CPU, or RISC for specific applications.

Note: The RTL8364NB-VB Extra Interface GMAC1 supports:

Reduced Gigabit Media Independent Interface (RGMII) (3.3V/2.5V/1.8V mode)

Media Independent Interface (MII)

Turbo Media Independent Interface (TMII)

Reduced Media Independent Interface (RMII)

High-Serial Gigabit Media Independent Interface (HSGMII, 3.125Gbps)

Serial Gigabit Media Independent Interface (SGMII, 1.25Gbps)

IEEE 1000Base-X

IEEE 100Base-FX

The RTL8364NB-VB Extra Interface GMAC2 supports:

Gigabit Media Independent Interface (GMII)

Reduced Gigabit Media Independent Interface (RGMII) (3.3V/2.5V/1.8V mode)

Media Independent Interface (MII)

Turbo Media Independent Interface (TMII)

Reduced Media Independent Interface (RMII)

Serial Gigabit Media Independent Interface (SGMII, 1.25Gbps)

IEEE 1000Base-X

IEEE 100Base-FX

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The RTL8364NB-VB Extra Interface GMAC1 and GMAC2 cannot work in SerDes mode (SerDes mode include HSGMII/SGMII/1000Base-X/100FX) at the same time. When the GMAC2 be configured to use GMII interface, the GMAC1 can be configured to SerDes mode only.

The RTL8364NB-VB Extra Interface GMAC1 and GMAC2 cannot work in RGMII 1.8V mode at the same time, as e2 support 3.3V/2.5V Mode only when be configured to RGMII Mode (Refer Figure 4).

The RTL8364NB-VB supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8364NB-VB supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast application, the RTL8364NB-VB can forward IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping protocol packets.

In order to support flexible traffic classification, the RTL8364NB-VB supports 48-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, force output tag and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8364NB-VB supports 16 sets of port configurations: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet security and management application requirements, the RTL8364NB-VB supports IEEE 802.1x Port-based/MAC-based Access Control. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time and multimedia networking applications, the RTL8364NB-VB supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or Weighted Round Robin (WRR) or mixed.

The RTL8364NB-VB provides a 4096-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8364NB-VB supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or Slave I2C-like serial Interface, or Slave Media Independent Interface Management (MIIM) Interface after reset.

In embedded system applications, CPU may want to know the input port of the incoming packet. The RTL8364NB-VB supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8364NB-VB also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, the RTL8364NB-VB will drop all non-tagged packets.

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2. Features

- Single-chip 2+2-port 10/100/1000M non-blocking switch architecture
- Embedded 2 -port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Extra Interface GMAC1 supports
  - Media Independent Interface (MII)
  - Reduced 10/100/1000M Media Independent Interface (RGMII) (support 3.3V/2.5V/1.8V mode)
  - Turbo Media Independent Interface (TMII)
  - Reduced Media Independent Interface (RMII)
  - High-Serial Gigabit Media Independent Interface (HSGMII, 3.125Gbps)
  - Serial Gigabit Media Independent Interface (SGMII, 1.25Gbps)
  - IEEE 1000Base-X
  - IEEE 100Base-FX
- Extra Interface GMAC2 supports
  - Media Independent Interface (MII)
  - Reduced 10/100/1000M Media Independent Interface (RGMII) (support 3.3V/2.5V/1.8V mode, note that the Extension GMAC1 and GMAC2 cannot support 1.8V RGMII at the same time)
  - 1000M Media Independent Interface (GMII)
  - Turbo Media Independent Interface (TMII)
  - Reduced Media Independent Interface (RMII)
  - Serial Gigabit Media Independent Interface (SGMII, 1.25Gbps)
  - IEEE 1000Base-X
  - IEEE 100Base-FX
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Realtek Cable Test (RTCT) function
- Supports 48-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions support mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment
  - Supports five types of user defined ACL rule format for 48 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4096 VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - 2048-entry MAC address table with 4-way hash algorithm
  - Up to 2048-entry L2/L3 Filtering Database

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- Per-port MAC learning limitation
- System base MAC learning limitation

- Supports Spanning Tree Port Behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
- Supports Auto protection from Denial-of-Service attacks
- Support trap IGMP/MLD packets to external CPU
- Supports Quality of Service (QoS)
  - Supports per port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ), Weighted Round Robin (WRR) packet scheduling
  - One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (12 shared meters, with 8kbps granulation)
- Supports RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with eight Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports MAC-based 1:N VLAN
- Supports Port Mirror function for one monitor port for multiple mirroring ports
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports IEEE 802.3az Energy Efficient Ethernet (EEE)
- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Supports one interrupt output to external CPU for notification
- Port 1/3 supports 3 LED outputs per port
- Management Interface Supports configuration register
  - Slave I2C-like interface
  - Slave MII Management interface
  - Slave SPI Interface
- Supports 32K-byte EEPROM space for configuration
- 25MHz crystal or 3.3V OSC input
- 10x10 QFN 88-pin package

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3. System Applications

- 2-Port 1000Base-T Router with Dual MII/RGMII
- 2-Port 1000Base-T Router with MII/RGMII and SGMI/HSGMII
- 2-Port 1000Base-T and 1-Port Fiber Router with MII/RGMII/GMII

4. Application Examples

4.1. 2-Port 1000Base-T Router with Dual MII/RGMII

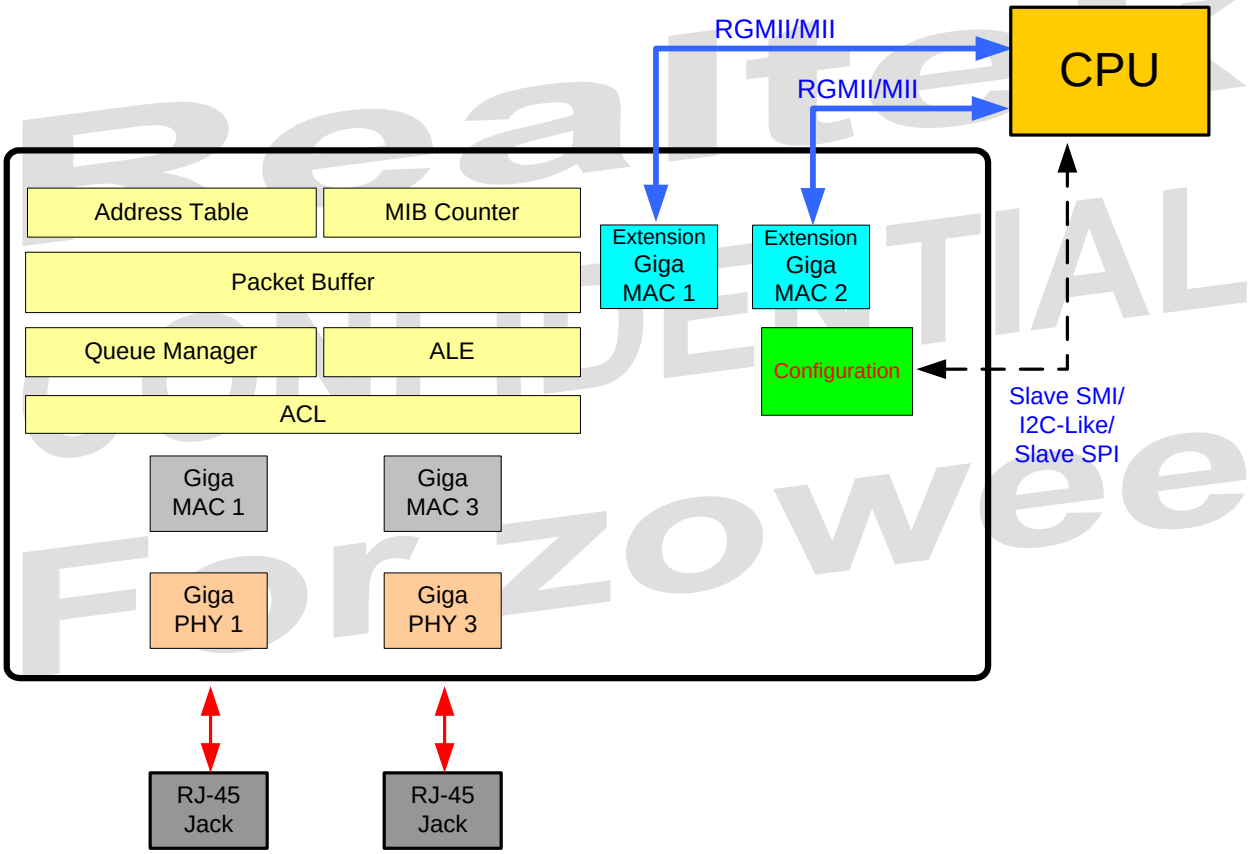


Figure 1. 2-Port 1000Base-T Router with Dual MII/RGMII

Note: Extra Interface (Extension GMAC1 and Extension GMAC2) in MII/RGMII Mode.

4.2. 2-Port 1000Base-T Router with MII/RGMII and SGMII/HSGMII

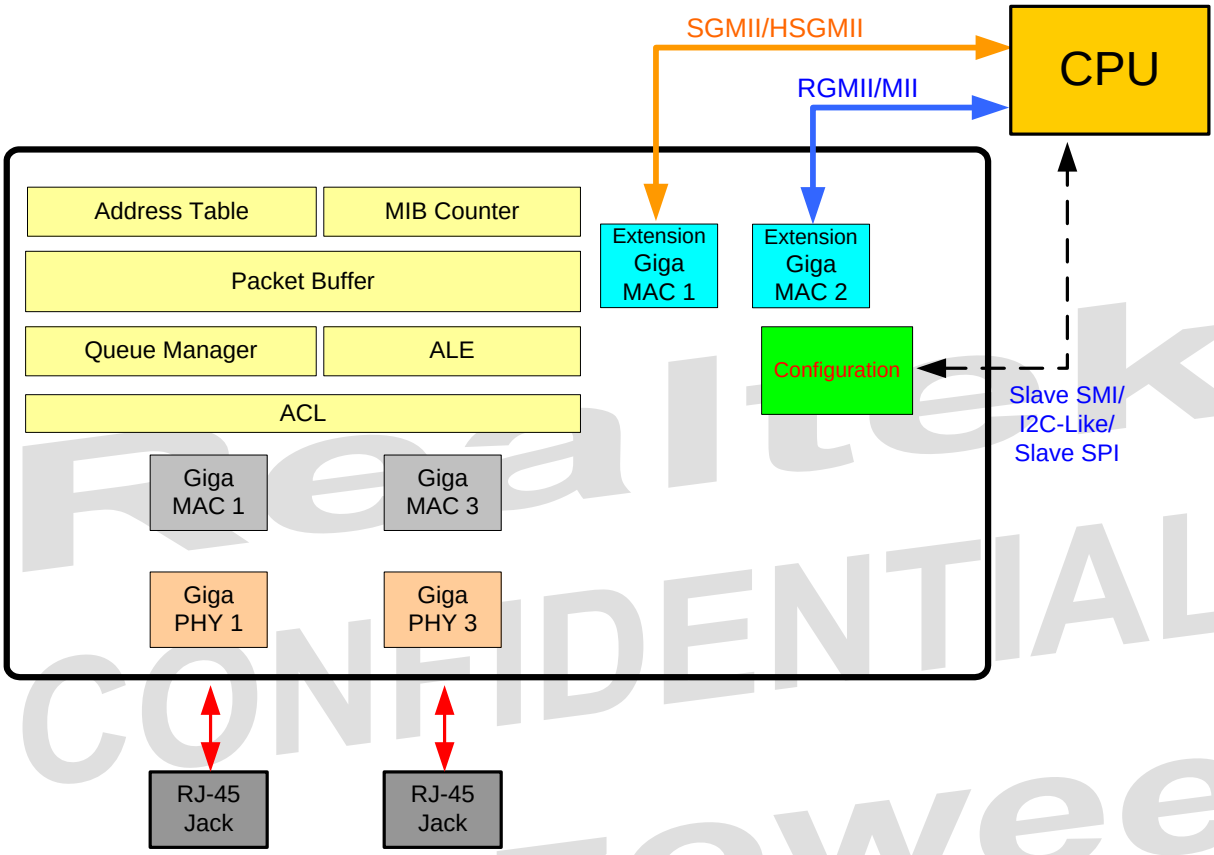


Figure 2. 2-Port 1000Base-T Router with MII/RGMII and SGMII/HSGMII

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Note: Extra Interface GMAC1 in SGMII/HSGMII Mode, and Extension GMAC2 in MII/RGMII Mode.

4.3. 2-Port 1000Base-T and 1-Port Fiber Router with MII/RGMII/GMII

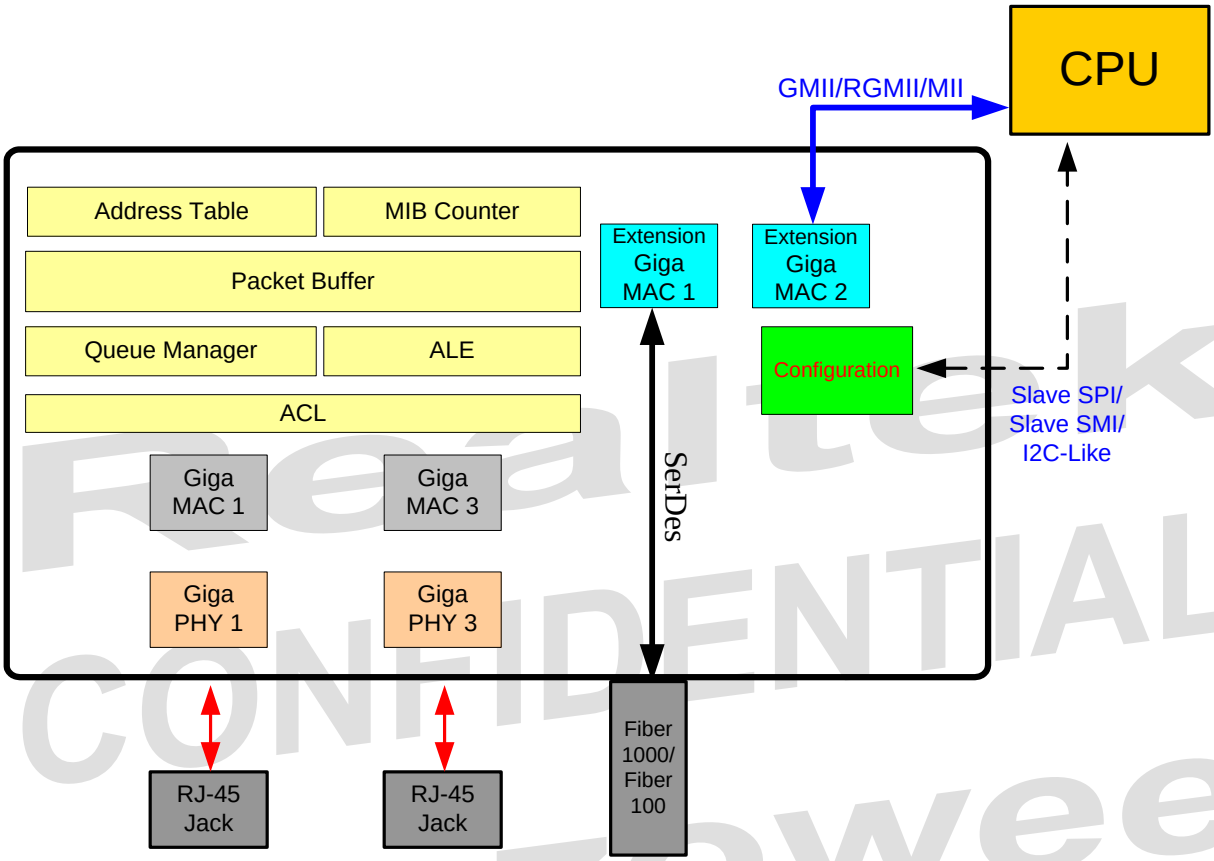
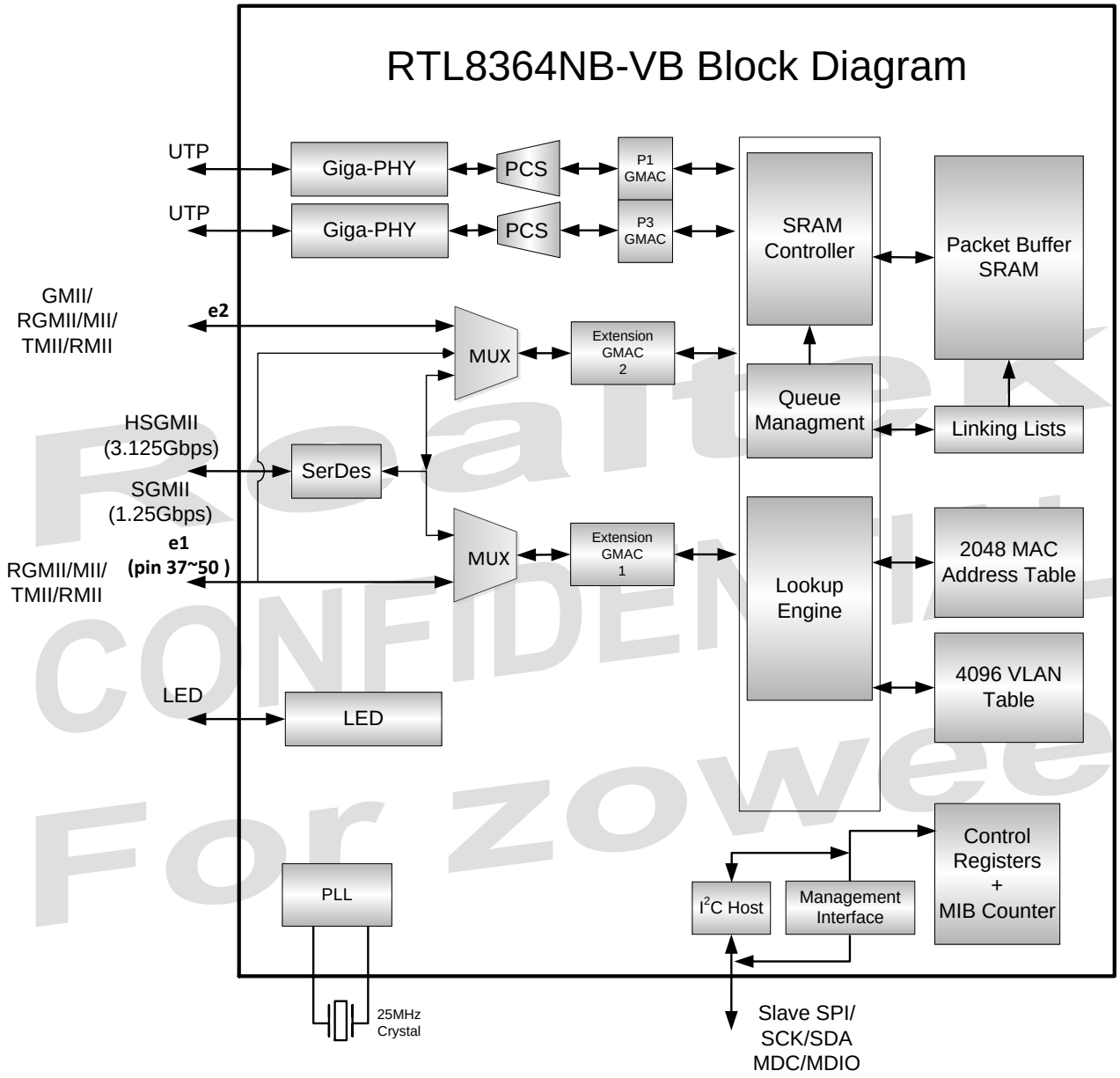


Figure 3. 2-Port 1000Base-T and 1-Port Fiber Router with MII/RGMII/GMII

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Note: Extra Interface GMAC2 in MII/RGMII/GMII Mode, and Extension GMAC1 in 1000Base-X or 100Base-FX Mode.

5. Block Diagram



Note:
1> When Extension GMAC2 connect to SerDes Interface, only SGMII mode/1000Base-X mode/100FX mode be supported (3.125Gbps HSGMII mode is not supported).
2> When Extension GMAC2 connect to GMII Interface, the GMAC1 only can be connect to SerDes interface (HSGMII/SGMII/1000Base-X/100FX).
3> Extension GMAC1 and GMAC2 cannot work in RGMII 1.8V mode at the same time, as e2 support 3.3V/2.5V Mode only when be configured to RGMII Mode.

Figure 4. Block Diagram

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6. Pin Assignments

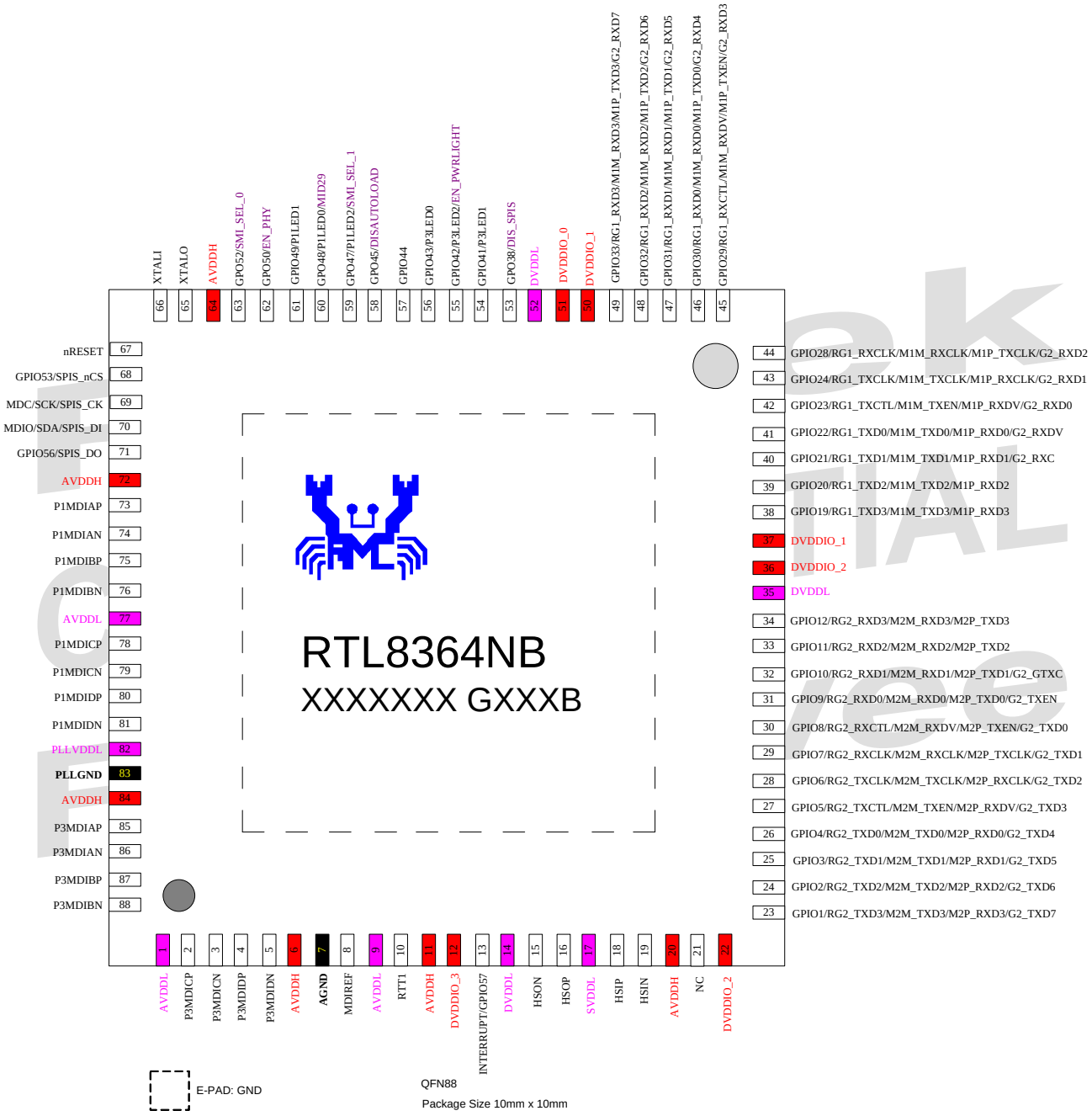


Figure 5. Pin Assignments (QFN-88)

6.1. Package Identification

Green package is indicated by the 'G' in GXXXB (**Figure 5**).

6.2. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Directional Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

I_S: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Directional Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

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Table 1. Pin Assignments Table

Name	Pin No.	Type
AVDDL	1	AP
P3MDICP	2	AI/O
P3MDICN	3	AI/O
P3MDIDP	4	AI/O
P3MDIDN	5	AI/O
AVDDH	6	AP
AGND	7	AG
MDIREF	8	AO
AVDDL	9	AP
RTT1	10	AO
AVDDH	11	AP
DVDDIO_3	12	P
GPIO57/INTERRUPT	13	I/O_{PD}
DVDDL	14	P
HSON	15	AO
HSOP	16	AO
SVDDL	17	AP
HSIP	18	AI
HSIN	19	AI
AVDDH	20	AP
NC	21	-
DVDDIO_2	22	P

Name	Pin No.	Type
GPIO1/ RG2_TXD3 /M2M_TXD3/M2P_RXD3/ G2_TXD7	23	I/O
GPIO2/ RG2_TXD2 /M2M_TXD2/M2P_RXD2/ G2_TXD6	24	I/O
GPIO3/ RG2_TXD1 /M2M_TXD1/M2P_RXD1/ G2_TXD5	25	I/O
GPIO4/ RG2_TXD0 /M2M_TXD0/M2P_RXD0/ G2_TXD4	26	I/O
GPIO5/ RG2_TXCTL/ M2M_TXEN/M2P_RXDV/ G2_TXD3	27	I/O
GPIO6/RG2_TXCLK/ M2M_TXCLK/M2P_RXCLK/ G2_TXD2	28	I/O
GPIO7/RG2_RXCLK/ M2M_RXCLK/M2P_TXCLK/ G2_TXD1	29	I/O
GPIO8/RG2_RXCTL /M2M_RXDV/M2P_TXEN/ G2_TXD0	30	I/O

Name	Pin No.	Type
GPIO9/RG2_RXD0 /M2M_RXD0/M2P_TXD0/ G2_TXEN	31	I/O
GPIO10/RG2_RXD1 /M2M_RXD1/M2P_TXD1/ G2_GTXC	32	I/O
GPIO11/RG2_RXD2/M2M_RXD2/ M2P_TXD2	33	I/O
GPIO12/RG2_RXD3/M2M_RXD3/ M2P_TXD3	34	I/O
DVDDL	35	P
DVDDIO_2	36	P
DVDDIO_1	37	P
GPIO19/RG1_TXD3 /M1M_TXD3/M1P_RXD3	38	I/O
GPIO20/RG1_TXD2/M1M_TXD2/ M1P_RXD2	39	I/O
GPIO21/RG1_TXD1/M1M_TXD1/ M1P_RXD1/G2_RXC	40	I/O
GPIO22/RG1_TXD0/M1M_TXD0/ M1P_RXD0/G2_RXDV	41	I/O
GPIO23/RG1_TXCTL /M1M_TXEN/M1P_RXDV/ G2_RXD0	42	IO
GPIO24/RG1_TXCLK/ M1M_TXCLK/M1P_RXCLK/ G2_RXD1	43	I/O
GPIO28/RG1_RXCLK /M1M_RXCLK/M1P_TXCLK/ G2_RXD2	44	I/O
GPIO29/RG1_RXCTL /M1M_RXDV/M1P_TXEN/ G2_RXD3	45	I/O
GPIO30/RG1_RXD0 /M1M_RXD0/M1P_TXD0/ G2_RXD4	46	I/O
GPIO31/RG1_RXD1 /M1M_RXD1/M1P_TXD1/ G2_RXD5	47	I/O
GPIO32/RG1_RXD2 /M1M_RXD2/M1P_TXD2/ G2_RXD6	48	I/O
GPIO33/RG1_RXD3 /M1M_RXD3/M1P_TXD3/ G2_RXD7	49	I/O

Name	Pin No.	Type
DVDDIO_1	50	P
DVDDIO_0	51	P
DVDDL	52	P
GPO38/DIS_SPIS	53	I/O_{PU}
GPIO41/P3LED1	54	I/O_{PU}
GPO42/P3LED2/EN_PWRLIGHT	55	I/O_{PU}
GPIO43/P3LED0	56	I/O_{PU}
GPIO44	57	I/O_{PU}
GPO45/DISAUTOLOAD	58	I/O_{PU}
GPO47/P1LED2/SMI_SEL_1	59	I/O_{PU}
GPO48/P1LED0/MID29	60	I/O_{PU}
GPIO49/P1LED1	61	I/O_{PU}
GPO50/EN_PHY	62	I/O_{PU}
GPO52/SMI_SEL_0	63	I/O_{PU}
AVDDH	64	AP
XTALO	65	AI/O
XTALI	66	AI
nRESET	67	I_{PU}
GPIO53/SPIS_nCS	68	I/O_{PU}
MDC/SCK/SPIS_CK	69	I/O
MDIO/SDA/SPIS_DI	70	I/O
GPIO56/SPIS_DO	71	I/O
AVDDH	72	AP
P1MDIAP	73	AI/O
P1MDIAN	74	AI/O
P1MDIBP	75	AI/O
P1MDIBN	76	AI/O
AVDDL	77	AP
P1MDICP	78	AI/O
P1MDICN	79	AI/O
P1MDIDP	80	AI/O
P1MDIDN	81	AI/O
PLLVDDL	82	AP
PLLGND	83	AG
AVDDH	84	AP
P3MDIAP	85	AI/O
P3MDIAN	86	AI/O
P3MDIBP	87	AI/O
P3MDIBN	88	AI/O
GND	EPAD	G

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7. Pin Descriptions

7.1. Media Dependent Interface Pins

Table 2. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	73 74 75 76 78 79 80 81	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	85 86 87 88 2 3 4 5	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-TX and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

7.2. High Speed Serial Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
HSOP/N	16 15	AO	10	High Speed Serial Output Pins: 125MHz/1.25GHz/3.125GHz Differential serial interface to transmit data. Keep floating when unused.
HSIP/N	18 19	AI	10	High Speed Serial Input Pins: 125MHz/1.25GHz/3.125GHz Differential serial interface to receive data. Keep floating when unused.

7.3. General Purpose Interfaces

The RTL8364NB-VB supports multi-function General Purpose Interfaces that can be configured as MII/RGMII/GMII mode for extension GMAC interfaces. The RTL8364NB-VB supports two extension interfaces (Extension GMAC1 and Extension GMAC2) for connecting with an external PHY, MAC, or CPU in specific applications. These extension interfaces support GMII, RGMII, (T)MII MAC mode, (T)MII PHY mode or RMII mode via register configuration.

Table 3. General Purpose Interfaces Pins

Pin No.	GPIO	RGMII	GMII	(T)MII MAC Mode	(T)MII PHY Mode	RMII and Other function	Configuration Strapping
13	GPIO57	-	-	-	-	INTERRUPT	-
23	GPIO1	RG2_TXD3	G2_TXD7	M2M_TXD3	M2P_RXD3	-	-

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Pin No.	GPIO	RGMII	GMII	(T)MII MAC Mode	(T)MII PHY Mode	RMII and Other function	Configuration Strapping
24	GPIO2	RG2_TXD2	G2_TXD6	M2M_TXD2	M2P_RXD2	-	-
25	GPIO3	RG2_TXD1	G2_TXD5	M2M_TXD1	M2P_RXD1	RM2M_TXD1	-
26	GPIO4	RG2_TXD0	G2_TXD4	M2M_TXD0	M2P_RXD0	RM2M_TXD0	-
27	GPIO5	RG2_TXCTL	G2_TXD3	M2M_TXEN	M2P_RXDV	RM2M_TXEN	-
28	GPIO6	RG2_TXCLK	G2_TXD2	M2M_TXCLK	M2P_RXCLK	RM2M_CLK	-
29	GPIO7	RG2_RXCLK	G2_TXD1	M2M_RXCLK	M2P_TXCLK	-	-
30	GPIO8	RG2_RXCTL	G2_TXD0	M2M_RXDV	M2P_TXEN	RM2M_CRS_DV	-
31	GPIO9	RG2_RXD0	G2_TXEN	M2M_RXD0	M2P_TXD0	RM2M_RXD0	-
32	GPIO10	RG2_RXD1	G2_GTXC	M2M_RXD1	M2P_TXD1	RM2M_RXD1	-
33	GPIO11	RG2_RXD2	-	M2M_RXD2	M2P_TXD2	-	-
34	GPIO12	RG2_RXD3	-	M2M_RXD3	M2P_TXD3	-	-
38	GPIO19	RG1_TXD3	-	M1M_TXD3	M1P_RXD3	-	-
39	GPIO20	RG1_TXD2	-	M1M_TXD2	M1P_RXD2	-	-
40	GPIO21	RG1_TXD1	G2_RXC	M1M_TXD1	M1P_RXD1	RM1M_TXD1	-
41	GPIO22	RG1_TXD0	G2_RXDV	M1M_TXD0	M1P_RXD0	RM1M_TXD0	-
42	GPIO23	RG1_TXCTL	G2_RXD0	M1M_TXEN	M1P_RXDV	RM1M_TXEN	-
43	GPIO24	RG1_TXCLK	G2_RXD1	M1M_TXCLK	M1P_RXCLK	RM1M_CLK	-
44	GPIO28	RG1_RXCLK	G2_RXD2	M1M_RXCLK	M1P_TXCLK	-	-
45	GPIO29	RG1_RXCTL	G2_RXD3	M1M_RXDV	M1P_TXEN	RM1M_CRS_DV	-
46	GPIO30	RG1_RXD0	G2_RXD4	M1M_RXD0	M1P_TXD0	RM1M_RXD0	-
47	GPIO31	RG1_RXD1	G2_RXD5	M1M_RXD1	M1P_TXD1	RM1M_RXD1	-
48	GPIO32	RG1_RXD2	G2_RXD6	M1M_RXD2	M1P_TXD2	-	-
49	GPIO33	RG1_RXD3	G2_RXD7	M1M_RXD3	M1P_TXD3	-	-
53	GPO38	-	-	-	-	-	DIS_SPIS
54	GPIO41	-	-	-	-	P3LED1	-
55	GPO42	-	-	-	-	P3LED2	EN_PWRLIGHT
56	GPIO43	-	-	-	-	P3LED0	-
57	GPIO44	-	-	-	-	-	-
58	GPO45	-	-	-	-	-	DISAUTOLOAD
59	GPO47	-	-	-	-	P1LED2	SMI_SEL_1
60	GPO48	-	-	-	-	P1LED0	MID29
61	GPIO49	-	-	-	-	P1LED1	-
62	GPO50	-	-	-	-	-	EN_PHY
63	GPO52	-	-	-	-	-	SMI_SEL_0
68	GPIO53	-	-	-	-	SPIS_nCS	-
71	GPIO56	-		-	-	SPIS_DO	-

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7.3.1. RGMII Pins

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB support dual RGMII interfaces to connect with an external MAC or PHY device when register configuration is set to RGMII mode interface.

Table 4. Extension 1 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG1_TXD3 RG1_TXD2 RG1_TXD1 RG1_TXD0	38 39 40 41	O	-	RG1_TXD[3:0] Extension GMAC1 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG1_TXCLK.
RG1_TXCTL	42	O	-	RG1_TXCTL Extension GMAC1 RGMII Transmit Control signal Output. The RG1_TXCTL indicates TX_EN at the rising edge of RG1_TXCLK, and TX_ER at the falling edge of RG1_TXCLK. At the RG1_TXCLK falling edge, RG1_TXCTL= TX_EN (XOR) TX_ER.
RG1_TXCLK	43	O	-	RG1_TXCLK Extension GMAC1 RGMII Transmit Clock Output. RG1_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_TXD[3:0] and RG1_TXCTL synchronization at RG1_TXCLK on both rising and falling edges.
RG1_RXCLK	44	I	-	RG1_RXCLK Extension GMAC1 RGMII Receive Clock Input. RG1_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_RXD[3:0] and RG1_RXCTL synchronization at both RG1_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXCTL	45	I	-	RG1_RXCTL Extension GMAC1 RGMII Receive Control signal input. The RG1_RXCTL indicates RX_DV at the rising of RG1_RXCLK and RX_ER at the falling edge of RG1_RXCLK. At RG1_RXCLK falling edge, RG1_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXD0 RG1_RXD1 RG1_RXD2 RG1_RXD3	46 47 48 49	I	-	RG1_RXD[3:0] Extension GMAC1 RGMII Receive Data Input. Received data is received synchronously by RG1_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

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Table 5. Extension 2 RGMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RG2_TXD3 RG2_TXD2 RG2_TXD1 RG2_TXD0	23 24 25 26	O	-	RG2_TXD[3:0] Extension GMAC2 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG2_TXCLK.
RG2_TXCTL	27	O	-	RG2_TXCTL Extension GMAC2 RGMII Transmit Control signal Output. The RG2_TXCTL indicates TX_EN at the rising edge of RG2_TXCLK, and TX_ER at the falling edge of RG2_TXCLK. At the RG2_TXCLK falling edge, RG2_TXCTL= TX_EN (XOR) TX_ER.
RG2_TXCLK	28	O	-	RG2_TXCLK Extension GMAC2 RGMII Transmit Clock Output. RG2_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG2_TXD[3:0] and RG2_TXCTL synchronization at RG2_TXCLK on both rising and falling edges.
RG2_RXCLK	29	I	-	RG2_RXCLK Extension GMAC2 RGMII Receive Clock Input. RG2_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG2_RXD[3:0] and RG2_RXCTL synchronization at both RG2_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG2_RXCTL	30	I	-	RG2_RXCTL Extension GMAC2 RGMII Receive Control signal input. The RG2_RXCTL indicates RX_DV at the rising of RG2_RXCLK and RX_ER at the falling edge of RG2_RXCLK. At RG2_RXCLK falling edge, RG2_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG2_RXD0 RG2_RXD1 RG2_RXD2 RG2_RXD3	31 32 33 34	I	-	RG2_RXD[3:0] Extension GMAC2 RGMII Receive Data Input. Received data is received synchronously by RG2_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

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7.3.2. GMII Pins

The Extension GMAC2 of the RTL8364NB-VB support GMII interface to connect with an external MAC or PHY device when register configuration is set to GMII mode interface.

Table 6. Extension GMAC2 GMII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
G2_TXD7 G2_TXD6 G2_TXD5 G2_TXD4 G2_TXD3 G2_TXD2 G2_TXD1 G2_TXD0	23 24 25 26 27 28 29 30	O	-	G2_TXD[7:0] Extension GMAC2 GMII Transmit Data Output. Transmitted data is sent synchronously to G2_GTXC.
G2_TXEN	31	O	-	G2_TXEN Extension GMAC2 GMII Transmit Enable signal Output.
G2_GTXC	32	O	-	G2_GTXC Extension GMAC2 GMII Transmit Clock Output (125MHz).
G2_RXC	40	I	-	G2_RXC Extension GMAC2 GMII Receive Clock Input (125MHz). This pin must be pulled low with a 1K ohm resistor when not used.
G2_RXDV	41	I	-	G2_RXDV Extension GMAC2 GMII Receive Valid signal input. This pin must be pulled low with a 1K ohm resistor when not used.
G2_RXD0 G2_RXD1 G2_RXD2 G2_RXD3 G2_RXD4 G2_RXD5 G2_RXD6 G2_RXD7	42 43 44 45 46 47 48 49	I	-	G2_RXD[7:0] Extension GMAC2 GMII Receive Data Input. Received data is received synchronously by G2_RXC.

7.3.3. (T)MII Pins

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB supports (T)MII interface connection to an external MAC or PHY device when register configuration is set to (T)MII mode interface. The (T)MII interface can also be configured as (T)MII MAC mode or (T)MII PHY mode by register.

Table 7. Extension 1 (T)MII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_TXD3/ M1P_RXD3 M1M_TXD2/ M1P_RXD2 M1M_TXD1/ M1P_RXD1 M1M_TXD0/ M1P_RXD0	38 39 40 41	O	-	M1M_TXD[3:0] Extension 1 (T)MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXD[3:0] Extension 1 (T)MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M1P_RXCLK.

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Pin Name	Pin No.	Type	Drive (mA)	Description
M1M_TXEN/ M1P_RXDV	42	O	-	M1M_TXEN Extension 1 (T)MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXDV Extension 1 (T)MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M1P_RXCLK.
M1M_TXCLK/ M1P_RXCLK	43	I/O	-	M1M_TXCLK Extension 1 (T)MII MAC Mode Transmit Clock Input. In MII 100Mbps, M1M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_TXCLK is 2.5MHz Clock Input. In TMII 200Mbps, M1M_TXCLK is 50MHz Clock Input. In TMII 20Mbps, M1M_TXCLK is 5MHz Clock Input. Used to synchronize M1M_TXD[3:0] and M1M_TXEN. M1P_RXCLK Extension 1 (T)MII PHY Mode Receive Clock Output. In MII 100Mbps, M1P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_RXCLK is 2.5MHz Clock Output. In TMII 200Mbps, M1P_RXCLK is 50MHz Clock Output. In TMII 20Mbps, M1P_RXCLK is 5MHz Clock Output. Used to synchronize M1P_RXD[3:0] and M1P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXCLK/ M1P_TXCLK	44	I/O	-	M1M_RXCLK Extension 1 (T)MII MAC Mode Receive Clock Input. In MII 100Mbps, M1M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_RXCLK is 2.5MHz Clock Input. In TMII 200Mbps, M1M_RXCLK is 50MHz Clock Input. In TMII 20Mbps, M1M_RXCLK is 5MHz Clock Input. Used to synchronize M1M_RXD[3:0], M1M_RXDV. M1P_TXCLK Extension 1 (T)MII PHY Mode Transmit Clock Output. In MII 100Mbps, M1P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_TXCLK is 2.5MHz Clock Output. In TMII 200Mbps, M1P_TXCLK is 50MHz Clock Output. In TMII 20Mbps, M1P_TXCLK is 5MHz Clock Output. Used to synchronize M1P_TXD[3:0] and M1P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXDV/ M1P_TXEN	45	I	-	M1M_RXDV Extension 1 (T)MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M1M_RXCLK. M1P_TXEN Extension 1 (T)MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M1P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXD0/ M1P_TXD0 M1M_RXD1/ M1P_TXD1 M1M_RXD2/ M1P_TXD2 M1M_RXD3/ M1P_TXD3	46 47 48 49	I	-	M1M_RXD[3:0] Extension 1 (T)MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M1M_RXCLK. M1P_TXD[3:0] Extension 1 (T)MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M1P_TXCLK.

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Table 8. Extension 2 (T)MII Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
M2M_TXD3/ M2P_RXD3 M2M_TXD2/ M2P_RXD2 M2M_TXD1/ M2P_RXD1 M2M_TXD0/ M2P_RXD0	23 24 25 26	O	-	M2M_TXD[3:0] Extension 2 (T)MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M2M_TXCLK. M2P_RXD[3:0] Extension 2 (T)MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M2P_RXCLK.
M2M_TXEN/ M2P_RXDV	27	O	-	M2M_TXEN Extension 2 (T)MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M2M_TXCLK. M2P_RXDV Extension 2 (T)MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M2P_RXCLK.
M2M_TXCLK/ M2P_RXCLK	28	I/O	-	M2M_TXCLK Extension 2 (T)MII MAC Mode Transmit Clock Input. In MII 100Mbps, M2M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M2M_TXCLK is 2.5MHz Clock Input. In TMII 200Mbps, M2M_TXCLK is 50MHz Clock Input. In TMII 20Mbps, M2M_TXCLK is 5MHz Clock Input. Used to synchronize M2M_TXD[3:0] and M1M_TXEN. M2P_RXCLK Extension 2 (T)MII PHY Mode Receive Clock Output. In MII 100Mbps, M2P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M2P_RXCLK is 2.5MHz Clock Output. In TMII 200Mbps, M2P_RXCLK is 50MHz Clock Output. In TMII 20Mbps, M2P_RXCLK is 5MHz Clock Output. Used to synchronize M2P_RXD[3:0] and M2P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M2M_RXCLK/ M2P_TXCLK	29	I/O	-	M2M_RXCLK Extension 2 (T)MII MAC Mode Receive Clock Input. In MII 100Mbps, M2M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M2M_RXCLK is 2.5MHz Clock Input. In TMII 200Mbps, M2M_RXCLK is 50MHz Clock Input. In TMII 20Mbps, M2M_RXCLK is 5MHz Clock Input. Used to synchronize M2M_RXD[3:0], M2M_RXDV. M2P_TXCLK Extension 2 (T)MII PHY Mode Transmit Clock Output. In MII 100Mbps, M2P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M2P_TXCLK is 2.5MHz Clock Output. In TMII 200Mbps, M2P_TXCLK is 50MHz Clock Output. In TMII 20Mbps, M2P_TXCLK is 5MHz Clock Output. Used to synchronize M2P_TXD[3:0] and M1P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.

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Pin Name	Pin No.	Type	Drive (mA)	Description
M2M_RXDV/ M2P_TXEN	30	I	-	M2M_RXDV Extension 2 (T)MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M2M_RXCLK. M2P_TXEN Extension 2 (T)MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M2P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M2M_RXD0/ M2P_TXD0 M2M_RXD1/ M2P_TXD1 M2M_RXD2/ M2P_TXD2 M2M_RXD3/ M2P_TXD3	31 32 33 34	I	-	M2M_RXD[3:0] Extension 2 (T)MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M2M_RXCLK. M2P_TXD[3:0] Extension 2 (T)MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M2P_TXCLK.

7.3.4. RMII Pins

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB support dual RMII interfaces to connect with an external MAC or PHY device when register configuration is set to RMII mode interface. These two RMII interfaces can be configured as RMII Clock Input mode or RMII Clock Output mode by register.

Table 9. Extension 1 & Extension 2 RMII Pins (RMII Clock Input Mode or RMII Clock Output Mode)

Pin No.	Type	RMII	Description
40	O	RM1M_TXD1	RMII 1 TXD1
41	O	RM1M_TXD0	RMII 1 TXD0
42	O	RM1M_TXEN	RMII 1 TXEN
43	I/O	RM1M_CLK	RMII 1 Reference 50MHz Clock In RMII Clock Input Mode，this pin is Input. In RMII Clock Output Mode, this pin is Output.
45	I	RM1M_CRS_DV	RMII 1 CRS_DV
46	I	RM1M_RXD0	RMII 1 RXD0
47	I	RM1M_RXD1	RMII 1 RXD1
25	O	RM2M_TXD1	RMII 2 TXD1
26	O	RM2M_TXD0	RMII 2 TXD0
27	O	RM2M_TXEN	RMII 2 TXEN
28	I/O	RM2M_CLK	RMII 2 Reference 50MHz Clock In RMII Clock Input Mode，this pin is Input. In RMII Clock Output Mode, this pin is Output.
30	I	RM2M_CRS_DV	RMII 2 CRS_DV
31	I	RM2M_RXD0	RMII 2 RXD0
32	I	RM2M_RXD0	RMII 2 RXD1

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7.4. LED Pins

The RTL8364NB-VB LED Pins can be configured to parallel mode LED or serial mode LED interface via Register configuration. LED0, LED1, and LED2 of Port n indicate information that can be defined via register or EEPROM.

In parallel mode LED interface, when the LED pin is pulled low, the LED output polarity will be high active. When the LED pin is pulled high, the LED output polarity will change from high active to low active. See section 9.17 LED Indicators, page 45 for more details.

Table 10. LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P3LED2/ EN_PWRLIGHT	55	I/O_{PU}	-	Port 3 LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 45 for more details.
P3LED1	54	I/O_{PU}	-	Port 3 LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 45 for more details.
P3LED0	56	I/O_{PU}	-	Port 3 LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 45 for more details.
P1LED2/ SMI_SEL_1	59	I/O_{PU}	-	Port 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 45 for more details.
P1LED1	61	I/O_{PU}	-	Port 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 45 for more details.
P1LED0/ MID29	60	I/O_{PU}	-	Port 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM. See section 9.17 LED Indicators, page 45 for more details.

7.5. Configuration Strapping Pins

Table 11. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
DIS_SPIS	53	I/O_{PU}	SPI Slave Management Interface Selection. Pull Up: Disable SPI Slave Management Interface, and refer [SMI_SEL_1, SMI_SEL_0] Pull Down: Enable SPI Slave Management Interface *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

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Pin Name	Pin No.	Type	Description
EN_PWRLIGHT/ P3LED2	55	I/O_{PU}	Enable Power on Light. Pull Up: Enable Power on Light *Pull Down: Disable Power on Light* *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 9.17 LED Indicators, page 45 for more details.*
DISAUTOLOAD	58	I/O_{PU}	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload Pull Down: Enable EEPROM autoload *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
SMI_SEL_1/ P1LED2	59	I/O_{PU}	External CPU Access Interface Selection. SMI_SEL[1:0]: 00：LSB I^2C mode 01：MSB I^2C mode 10：Slave MII Management MDC/MDIO 11：Realtek I^2C-like mode *Note: These pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section9.17 LED Indicators, page 45 for more details.*
SMI_SEL_0	63	I/O_{PU}	
MID29/ P1LED0	60	I/O_{PU}	Slave SMI (MDC/MDIO) Device Address. Pull Up: MII Management Interface PHY ID is 29 Pull Down: MII Management Interface PHY ID is 0 *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 9.17 LED Indicators, page 45 for more details.*
EN_PHY	62	I/O_{PU}	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

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7.6. Management Interface Pins

Table 12. Management Interface Pins

Pin Name	Pin No.	Type	Description
SPIS_nCS	68	I_{PU}	When DIS_SPIS is Pulled Low, SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Chip Selection Input pin. When DIS_SPIS is Pulled Up, SPI Slave Management Interface is Disabled. This pin is unused.

Pin Name	Pin No.	Type	Description
MDC/ SCK/ SPIS_CK	69	I/O	Slave MII Management Interface Clock Master I2C Interface Clock for EEPROM auto-download. Slave I2C Interface Clock for external CPU to access DUT. SPI slave mode Serial Clock Input pin. (Selected via the hardware strapping DIS_SPIS & SMI_SEL_1 & SMI_SEL_0).
MDIO/ SDA/ SPIS_DI	70	I/O	Slave MII Management Interface Data Master I2C Interface Data for EEPROM auto-download. Slave I2C Interface Data for external CPU to access DUT. SPI slave mode Serial Data Input pin. (Selected via the hardware strapping DIS_SPIS & SMI_SEL_1 & SMI_SEL_0).
SPIS_DO	71	O	When DIS_SPIS is Pulled Low, SPI Slave Management Interface is Enabled. This pin acts as SPI slave mode Serial Data Output pin. When DIS_SPIS is Pulled Up, SPI Slave Management Interface is Disabled. This pin is unused.
INTERRUPT	13	O_{PD}	Interrupt output when Interrupt even occurs. Output can be high or low active by register configuration.

7.7. Miscellaneous Pins

Table 13. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
XTALO	65	AI/O	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output. When using a crystal, connect a loading capacitor from each pad to ground.
XTALI	66	AI	25MHz Crystal Clock Input Pin. 25MHz +/-50ppm tolerance crystal reference input. When using a crystal, connect a loading capacitor from each pad to ground. When either using an oscillator or driving an external 25MHz clock from another device, XTALO should be kept floating.
MDIREF	8	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
NC	21	-	Not Connected.
nRESET	67	I_{PU}	System Reset Input Pin. When low active will reset the RTL8364NB-VB.
GPIO1	23	I/O	General Purpose Input/Output Interface IO01.
GPIO2	24	I/O	General Purpose Input/Output Interface IO02.
GPIO3	25	I/O	General Purpose Input/Output Interface IO03.
GPIO4	26	I/O	General Purpose Input/Output Interface IO04.
GPIO5	27	I/O	General Purpose Input/Output Interface IO05.
GPIO6	28	I/O	General Purpose Input/Output Interface IO06.
GPIO7	29	I/O	General Purpose Input/Output Interface IO07.
GPIO8	30	I/O	General Purpose Input/Output Interface IO08.
GPIO9	31	I/O	General Purpose Input/Output Interface IO09.
GPIO10	32	I/O	General Purpose Input/Output Interface IO10.
GPIO11	33	I/O	General Purpose Input/Output Interface IO11.
GPIO12	34	I/O	General Purpose Input/Output Interface IO12.

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Pin Name	Pin No.	Type	Description
GPIO19	38	I/O	General Purpose Input/Output Interface IO19.
GPIO20	39	I/O	General Purpose Input/Output Interface IO20.
GPIO21	40	I/O	General Purpose Input/Output Interface IO21.
GPIO22	41	I/O	General Purpose Input/Output Interface IO22.
GPIO23	42	I/O	General Purpose Input/Output Interface IO23.
GPIO24	43	I/O	General Purpose Input/Output Interface IO24.
GPIO28	44	I/O	General Purpose Input/Output Interface IO28.
GPIO29	45	I/O	General Purpose Input/Output Interface IO29.
GPIO30	46	I/O	General Purpose Input/Output Interface IO30.
GPIO31	47	I/O	General Purpose Input/Output Interface IO31.
GPIO32	48	I/O	General Purpose Input/Output Interface IO32.
GPIO33	49	I/O	General Purpose Input/Output Interface IO33.
GP O38/ DIS_SPIS	53	I/O_{PU}	General Purpose Output Interface O38.
GPIO41/ P3LED1	54	I/O_{PU}	General Purpose Input/Output Interface IO41.
GP O42/ P3LED2/ EN_PWRLIGHT	55	I/O_{PU}	General Purpose Output Interface O42.
GPIO43/ P3LED0	56	I/O_{PU}	General Purpose Input/Output Interface O43.
GP O44	57	I/O_{PU}	General Purpose Output Interface O44.
GP O45/ DISAUTOLOAD	58	I/O_{PU}	General Purpose Output Interface O45.
GP O47/ P1LED2/ SMI_SEL_1	59	I/O_{PU}	General Purpose Output Interface O47.
GP O48/ P1LED0/ MID29	60	I/O_{PU}	General Purpose Output Interface O48.
GPIO49/ P1LED1	61	I/O_{PU}	General Purpose Input/Output Interface IO49.
GP O50/ EN_PHY	62	I/O_{PU}	General Purpose Output Interface O50.
GP O52/ SMI_SEL_0	63	I/O_{PU}	General Purpose Output Interface O52.
GPIO53/ SPIS_nCS	68	I/O_{PU}	General Purpose Input/Output Interface IO53.
GPIO56/ SPIS_DO	71	I/O	General Purpose Input/Output Interface IO56.
GPIO57/ INTERRUPT	13	I/O_{PD}	General Purpose Input/Output Interface IO57.

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7.8. Test Pins

Table 14. Test Pins

Pin Name	Pin No.	Type	Description
RTT1	10	AO	Reserved for Internal Use. Must be left floating.

7.9. Power and GND Pins

Table 15. Power and GND Pins

Pin Name	Pin No.	Type	Description
DVDDIO_0	51	P	Digital I/O High Voltage Power for LED, Management Interface, nRESET pins.
DVDDIO_1	37, 50	P	Digital I/O High Voltage Power for Extension Port 1 General Purpose Interface.
DVDDIO_2	22, 36	P	Digital I/O High Voltage Power for Extension Port 2 General Purpose Interface.
DVDDIO_3	12	P	Digital I/O High Voltage Power for INTERRUPT pin.
DVDDL	14, 35, 52	P	Digital Low Voltage Power.
AVDDH	6, 11, 20, 64, 72, 84	AP	Analog High Voltage Power.
AVDDL	1, 9, 77	AP	Analog Low Voltage Power.
SVDDL	17	AP	SerDes Analog Low Voltage Power.
PLLVDDL	82	AP	PLL Low Voltage Power.
GND	EPAD	G	GND.
AGND	7	AG	Analog GND.
PLLGND	83	AG	PLL GND.

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8. Physical Layer Functional Overview

8.1. MDI Interface

The RTL8364NB-VB embeds five 10/100/1000M Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-TX, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

8.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

8.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

8.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

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8.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

8.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

8.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

8.8. Auto-Negotiation for UTP

The RTL8364NB-VB obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8364NB-VB advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

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8.9. Crossover Detection and Auto Correction

The RTL8364NB-VB automatically determines whether or not it needs to crossover between pairs (see Table 16) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8364NB-VB automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 16. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

8.10. Polarity Correction

The RTL8364NB-VB automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

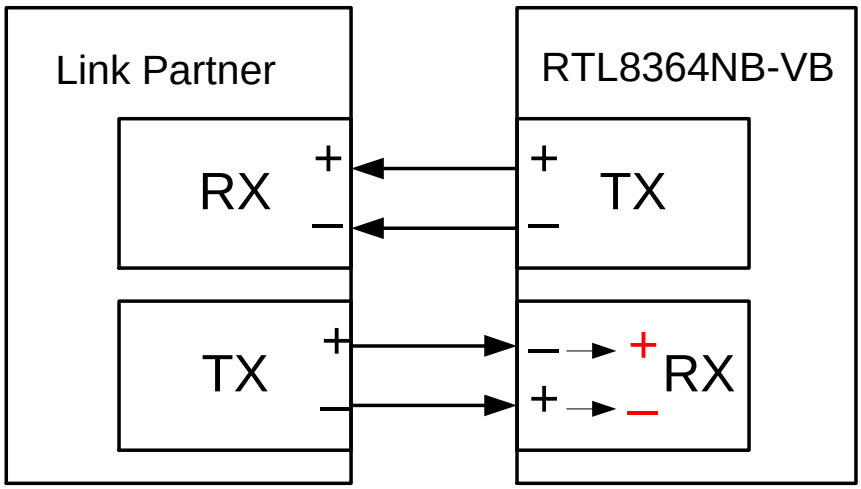


Figure 6. Conceptual Example of Polarity Correction

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9. General Function Description

9.1. Reset

9.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8364NB-VB will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

9.1.2. Software Reset

The RTL8364NB-VB supports two software resets; a chip reset and a soft reset.

9.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

9.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

9.2. IEEE 802.3x Full Duplex Flow Control

The RTL8364NB-VB supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

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9.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "Truncated Binary Exponential Backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8364NB-VB is 9.

The half duplex back-off algorithm in the RTL8364NB-VB does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

9.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8364NB-VB sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. The RTL8364NB-VB supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

9.4. Search and Learning

Search

When a packet is received, the RTL8364NB-VB uses the destination MAC address, Filtering Identifier (FID) and Enhanced Filtering Identifier (EFID) to search the 2048-entry look-up table. The 48-bit MAC address, 4-bit FID and 3-bit EFID use a hash algorithm, to calculate an 11-bit index value. The RTL8364NB-VB uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8364NB-VB uses the source MAC address, FID, and EFID of the incoming packet to hash into a 9-bit index (4-entry). It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8364NB-VB will update the entry with new

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information. If there is no match and the 4 entries are not all occupied by other MAC addresses, the RTL8364NB-VB will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8364NB-VB is between 200 and 400 seconds (typical is 300 seconds).

9.5. SVL and IVL/SVL

The RTL8364NB-VB supports a 16-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

9.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8364NB-VB. The maximum packet length may be set from 1518 bytes to 16K bytes.

9.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8364NB-VB supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 17 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 17. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
Provider Bridge Group Address	01-80-C2-00-00-08

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Assignment	Value
Undefined 802.1 Address	01-80-C2-00-00-04 ~ 01-80-C2-00-00-07 & 01-80-C2-00-00-09 ~ 01-80-C2-00-00-0C & 01-80-C2-00-00-0F
Provider Bridge MVRP Address	01-80-C2-00-00-0D
IEEE Std 802.1AB Link Layer Discovery Protocol Address	01-80-C2-00-00-0E
All LANs Bridge Management Group Address	01-80-C2-00-00-10
Load Server Generic Address	01-80-C2-00-00-11
Loadable Device Generic Address	01-80-C2-00-00-12
Undefined 802.1 Address	01-80-C2-00-00-13 ~ 01-80-C2-00-00-17 & 01-80-C2-00-00-19 & 01-80-C2-00-00-1B ~ 01-80-C2-00-00-1F
Generic Address for All Manager Stations	01-80-C2-00-00-18
Generic Address for All Agent Stations	01-80-C2-00-00-1a
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F
CDP(Cisco Discovery Protocol)	01-00-0C-CC-CC-CC
CSSTP(Cisco Shared Spanning Tree Protocol)	01-00-0C-CC-CC-CD
LLDP	(01:80:c2:00:00:0e or 01:80:c2:00:00:03 or 01:80:c2:00:00:00) && ethertype = 0x88CC

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9.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8364NB-VB enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate (number of Kbps per second or number of packets per second), all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

9.9. Port Security Function

The RTL8364NB-VB supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

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9.10. MIB Counters

The RTL8364NB-VB supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

9.11. Port Mirroring

The RTL8364NB-VB supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets from multiple mirrored port can be mirrored to one monitor port.

9.12. VLAN Function

The RTL8364NB-VB supports 4096 VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to ‘Admit All’, ‘Admit only Untagged’ or

'Admit only Tagged'

- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8364NB-VB will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8364NB-VB also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8364NB-VB supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID.

9.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached Slave I2C-like serial Interface, Slave Media Independent Interface Management (MIIM) Interface, or Salve SPI Interface. The 4096-entry VLAN Table designed into the RTL8364NB-VB provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

9.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8364NB-VB supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8364NB-VB uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8364NB-VB compares the explicit identifier in the VLAN tag with the 4096 VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8364NB-VB performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8364NB-VB performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8364NB-VB. One is the 'VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

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9.12.3. Protocol-Based VLAN

The RTL8364NB-VB supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 7. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be 'Ethernet', and value to be '0x0800'. Each table will index to one of the entries in the 4096-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

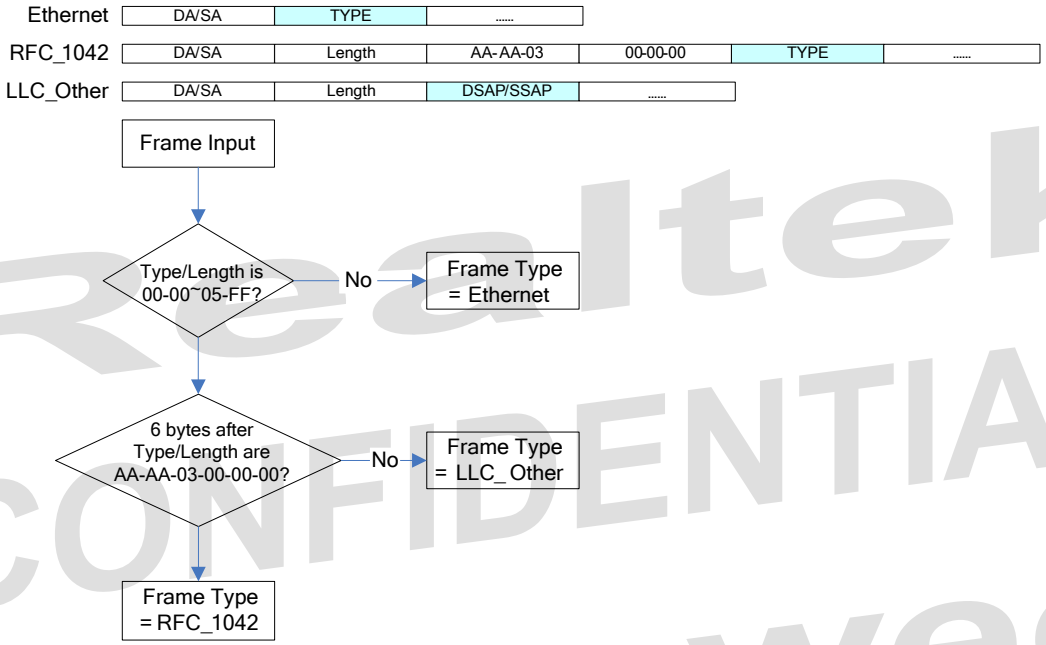


Figure 7. Protocol-Based VLAN Frame Format and Flow Chart

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9.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8364NB-VB supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress.

9.13. QoS Function

The RTL8364NB-VB supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8364NB-VB, the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) or Weighted Round Robin (WRR) for packet scheduling algorithm.

9.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a ‘pause ON’ frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

9.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8364NB-VB can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8364NB-VB identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority
- VLAN-based priority
- MAC-based priority
- SVLAN-based priority

9.13.3. Priority Queue Scheduling

The RTL8364NB-VB supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- Average Packet Rate (APR) leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue
- Weighted Round Robin (WRR)

In addition, each queue of each port can select Strict Priority or WFQ or WRR packet scheduling according to packet scheduling mode.

9.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8364NB-VB supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 8 queues, the packet’s 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. 802.1p/Q priority & IP DSCP value can be remarked based on internal priority or original 802.1p/Q priority & IP DSCP value in packets.

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9.13.5. ACL-Based Priority

The RTL8364NB-VB supports 48-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

If a packet hits an ACL rule and the priority action bit is 'enable', then this packet gets a 3-bit ACL-priority from the ACL module.

9.14. IEEE 802.1x Function

The RTL8364NB-VB supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior

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9.14.1. Port-Based Access Control

Each port of the RTL8364NB-VB can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

9.14.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

9.14.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

9.14.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

9.14.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction should be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

9.14.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

9.15. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8364NB-VB supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8364NB-VB also supports a per-port transmission/reception enable/disable function. Users can control the port state via register

9.16. Realtek Cable Test (RTCT)

The RTL8364NB-VB physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open or impedance mismatch in each differential pair. The RTL8364NB-VB also provides LED support to indicate test status and results.

9.17. LED Indicators

The RTL8364NB-VB supports parallel LEDs for each port. Each port has three LED indicator pins, LED0, LED1, and LED2. Each pin may have different indicator information (defined in Table 18). Refer to section 7.4 LED Pins, page 28 for pin details. Upon reset, the RTL8364NB-VB supports chip diagnostics and LED operation test by blinking all LEDs once.

Table 18. LED Definitions

LED Statuses	Description
LED_Off	LED Pin Output Off.

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LED Statuses	Description
Dup/Col	Duplex/Collision Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

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The LED pin also supports pin strapping configuration functions. The PnLED0, PnLED1, and PnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. When the pin input is pulled high upon reset, the pin output is active low after reset. When the pin input is pulled down upon reset, the pin output is active high after reset (see Figure 8 and Figure 9). Typical values for pull-up/pull-down resistors are 4.7KΩ.

The PnLED1 can be combined with PnLED0 or PnLED2 as a Bi-color LED.

The PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

- P1LED1 should pull up upon reset if P1LED1 is combined with P1LED2 as a Bi-color LED, and P1LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- P1LED1 should be pulled down upon reset if P1LED1 is combined with P1LED2 as a Bi-color LED, and P1LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

Upon reset, the RTL8364NB-VB supports chip diagnostics and LED functions by blinking all LEDs once. This function can be disabled by asserting EN_PWRLIGHT to 0b0 (pull down).

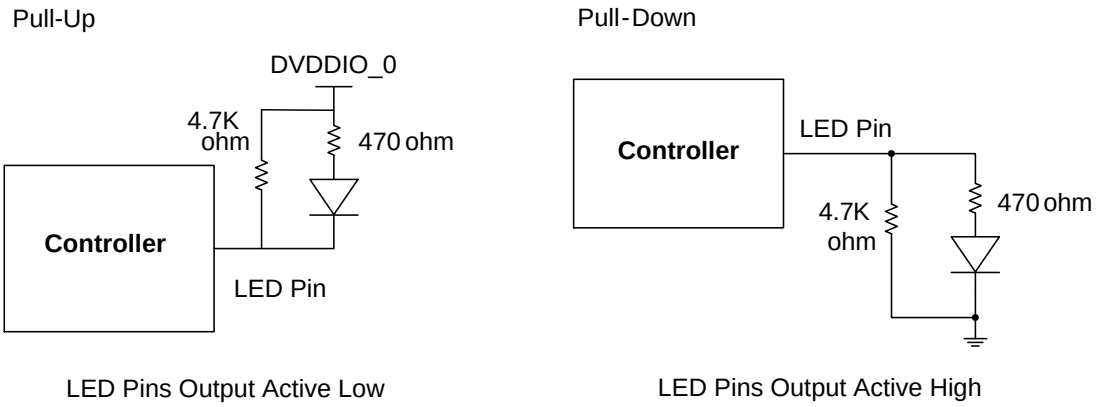


Figure 8. Pull-Up and Pull-Down of LED Pins for Single-Color LED

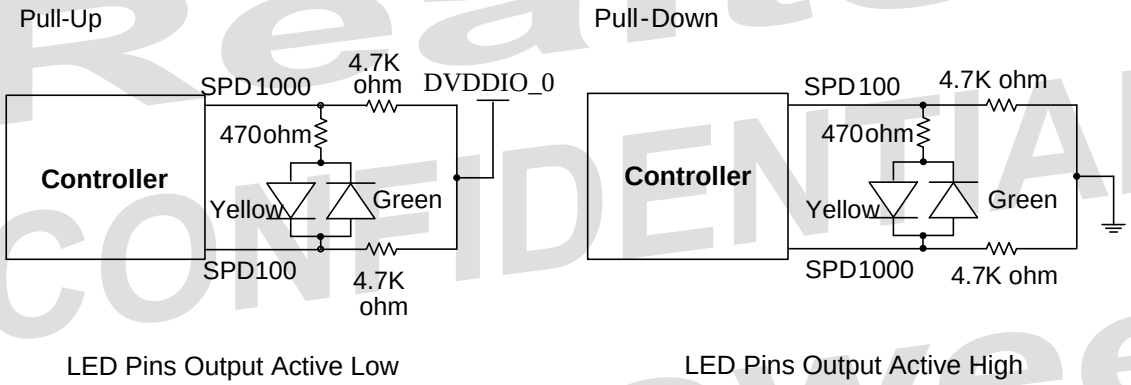


Figure 9. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

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9.18. Green Ethernet

9.18.1. Link-On and Cable Length Power Saving

The RTL8364NB-VB provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

9.18.2. Link-Down Power Saving

The RTL8364NB-VB implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

9.19. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8364NB-VB supports IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T and 100Base-TX in full duplex operation.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access Control (MAC) sub-layer with 100Base-TX and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle

The RTL8364NB-VB MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

9.20. Interrupt Pin for External CPU

The RTL8364NB-VB provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the RTL8364NB-VB will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

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10. Interface Descriptions

10.1. I2C Master for EEPROM Auto-load

The EEPROM interface of the RTL8364NB-VB uses the serial bus I^2C to read the Serial EEPROM. When the RTL8364NB-VB is powered up, it drives SCK and SDA to read the configuration/code data from the EEPROM by strapping configuration.

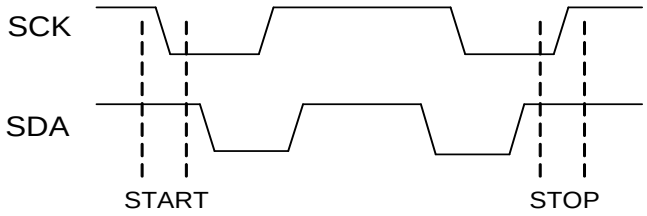


Figure 10. I2C Start and Stop Command

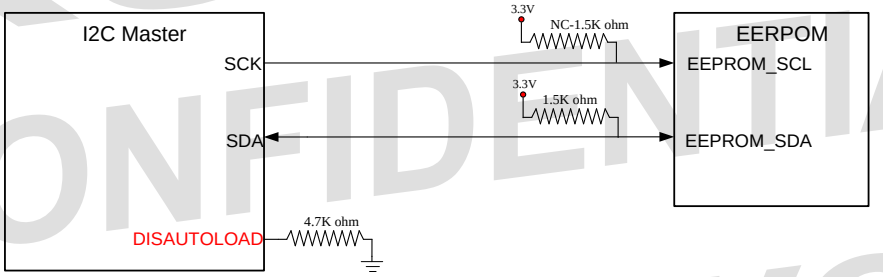


Figure 11. I2C Master for EEPROM Auto-load Interface Connection Example

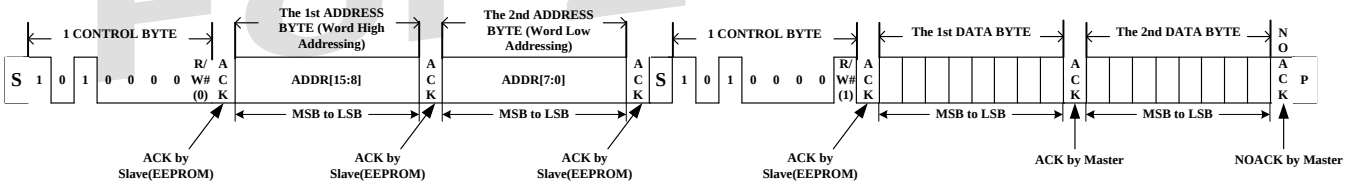


Figure 12. 16-Bit EEPROM Sequential Read

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10.2. Realtek I2C-Like Slave Interface for External CPU to Access RTL8364NB-VB

When EEPROM auto-load is complete, the RTL8364NB-VB registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8364NB-VB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

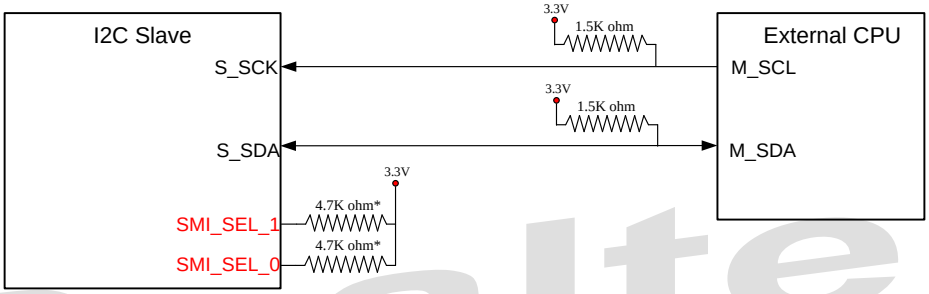


Figure 13. Realtek I2C-Like Slave for External CPU Access Interface Connection Example

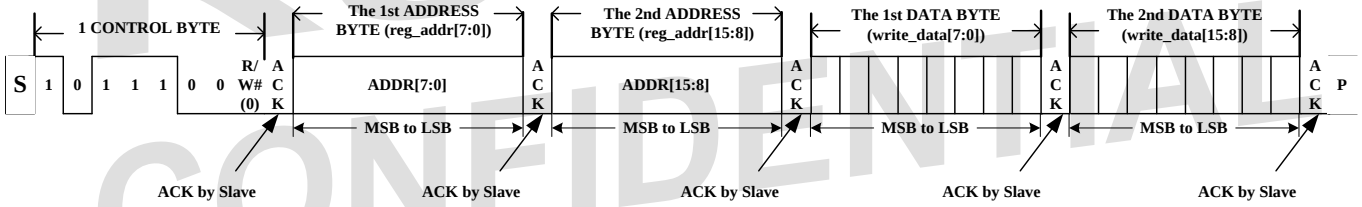


Figure 14. Realtek I2C-Like Slave Interface Write Command

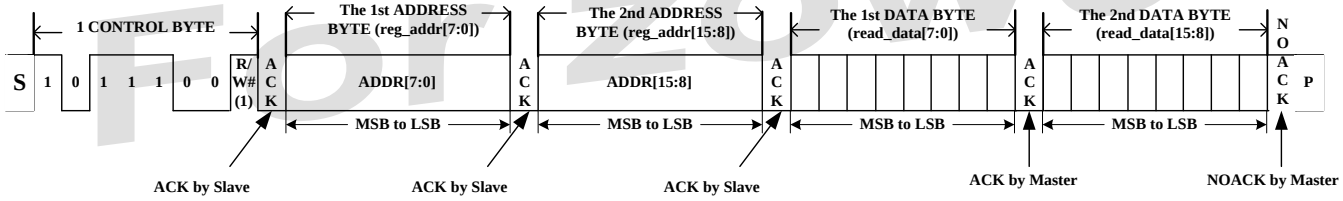


Figure 15. Realtek I2C-Like Slave Interface Read Command

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10.3. LSB I2C Slave Interface for External CPU to Access RTL8364NB-VB

When EEPROM auto-load is complete, the RTL8364NB-VB registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8364NB-VB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

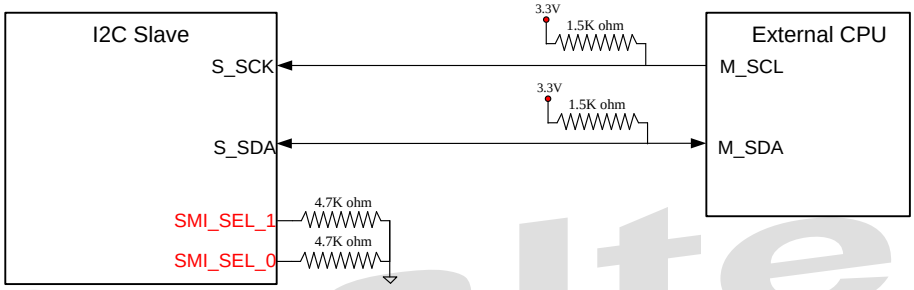


Figure 16. LSB I2C-like Slave for External CPU Access Interface Connection Example

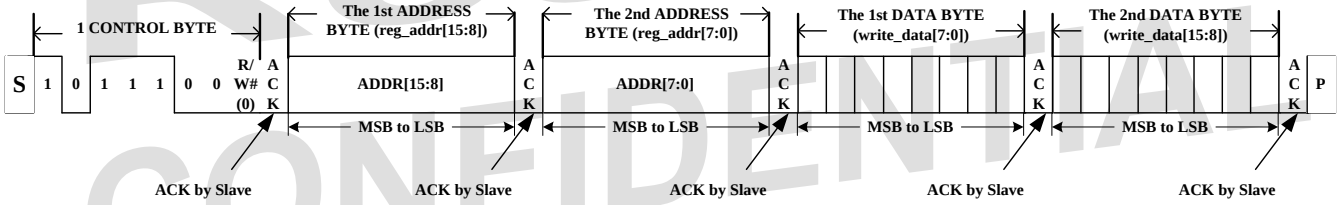


Figure 17. LSB I2C-like Slave Interface Write Command

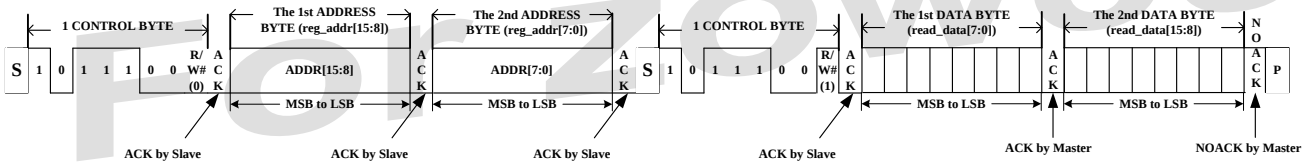


Figure 18. LSB I2C-like Slave Interface Read Command

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10.4. MSB I2C-like Slave Interface for External CPU to Access RTL8364NB-VB

When EEPROM auto-load is complete, the RTL8364NB-VB registers can be accessed through SCK and SDA via an external CPU. The device address of the RTL8364NB-VB is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

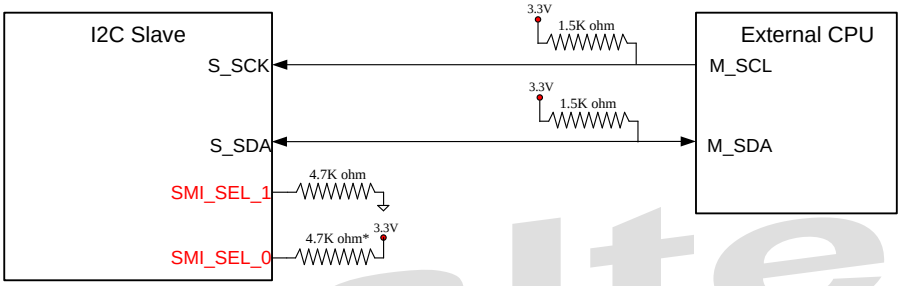


Figure 19. MSB I2C-like Slave for External CPU Access Interface Connection Example

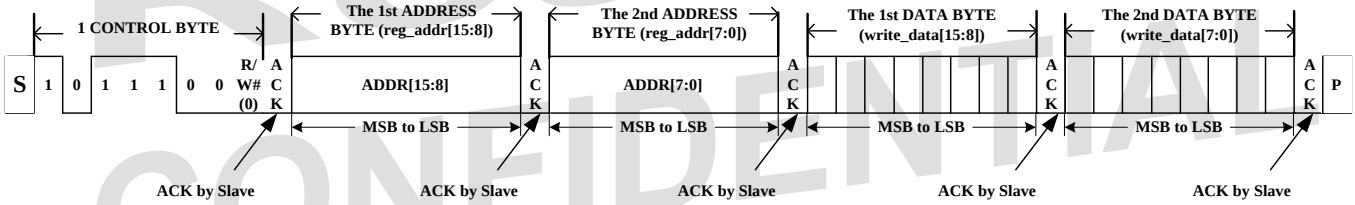


Figure 20. MSB I2C-like Slave Interface Write Command

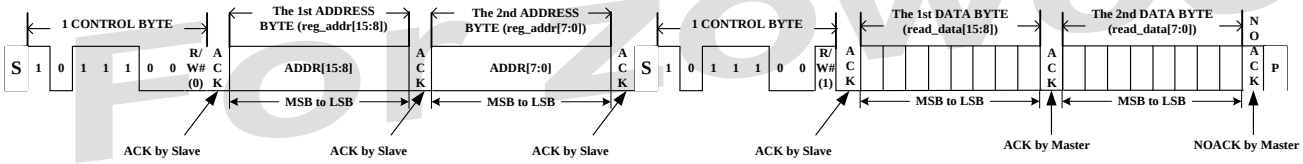


Figure 21. MSB I2C-like Slave Interface Read Command

10.5. *Slave MII Management SMI Interface for External CPU to Access* RTL8364NB-VB

The RTL8364NB-VB registers can be accessed via Slave MDC and MDIO via an external CPU (Decided by Strapping Configuration).

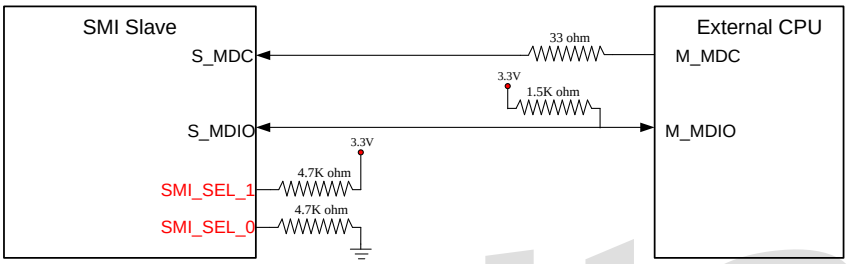


Figure 22. Slave MII Management SMI Interface Connection Example

Table 19. Slave MII Management SMI Access Format

	Management Frame Fields							
	PRE	**ST**	**OP**	**DEVAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note: The Slave needs no less than 32bit Preambles (PRE) for accessing slave by Slave SMI interface default. External CPU can configure the Slave to enable preamble suppression function, and then the Slave doesn't need preamble for accessing slave.

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10.6. SPI Slave for External CPU

The RTL8364NB-VB supports an SPI-Slave Management Interface that can be enabled via Pin configuration (see Table 11, page 28). An External CPU can configure or manage the RTL8364NB-VB internal register through the SPI interface.

When the CPU writes data to the RTL8364NB-VB internal register via the SPI interface, the first 8-bits is OP code, and the write command OP code is 8h'02. The second 8-bits define the address [15:8], the third 8-bits are the Address [7:0], the fourth 8-bits are write data [15:8], and the fifth 8-bits are write data [7:0] (see Figure 23).

When the CPU reads data from the RTL8364NB-VB internal register via the SPI interface, the first 8-bits OP code is 8h'03. The second 8-bits define the address [15:8] and the third 8-bits are the Address [7:0]. The RTL8364NB-VB returns read data [15:8] at the fourth 8-bits, and data [7:0] at the fifth 8-bits (see Figure 24).

10.6.1. SPI-Slave Interface Access Format

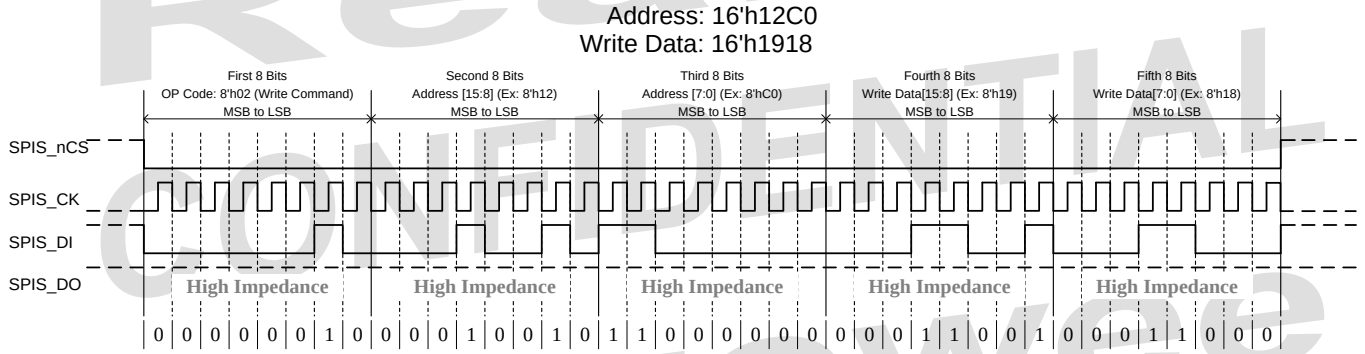


Figure 23. SPI-Slave Write Command Access Format

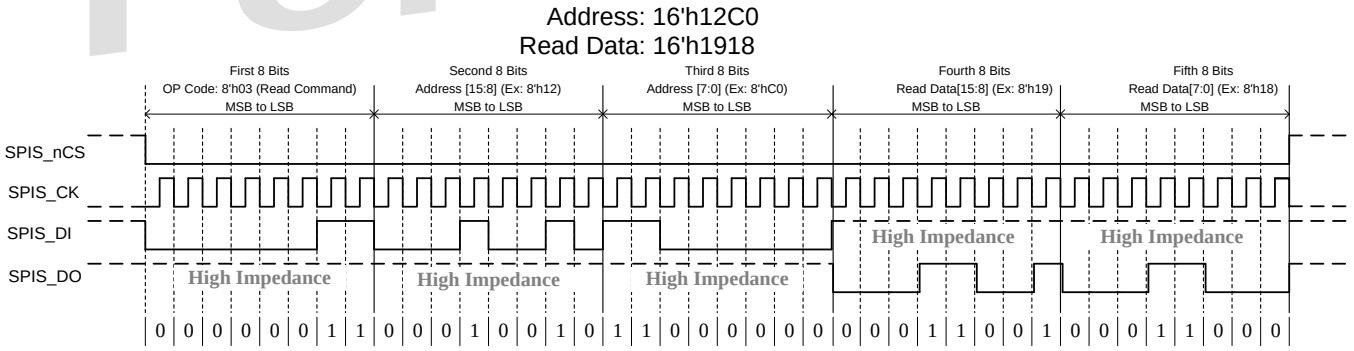


Figure 24. SPI-Slave Read Command Access Format

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10.7. General Purpose Interface

The RTL8364NB-VB supports two extension interfaces. The interface function mux is summarized in Table 20. The Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB support GMII, RGMII, MII MAC mode, or MII PHY mode via register configuration.

Table 20. RTL8364NB-VB Extension Port 1/Port 2 Pin Definitions

Pin No.	GPIO	RGMII	GMII	(T)MII MAC Mode	(T)MII PHY Mode	RMII Mode
23	GPIO1	RG2_TXD3	G2_TXD7	M2M_TXD3	M2P_RXD3	
24	GPIO2	RG2_TXD2	G2_TXD6	M2M_TXD2	M2P_RXD2	
25	GPIO3	RG2_TXD1	G2_TXD5	M2M_TXD1	M2P_RXD1	RM2M_TXD1
26	GPIO4	RG2_TXD0	G2_TXD4	M2M_TXD0	M2P_RXD0	RM2M_TXD0
27	GPIO5	RG2_TXCTL	G2_TXD3	M2M_TXEN	M2P_RXDV	RM2M_TXEN
28	GPIO6	RG2_TXCLK	G2_TXD2	M2M_TXCLK	M2P_RXCLK	RM2M_CLK
29	GPIO7	RG2_RXCLK	G2_TXD1	M2M_RXCLK	M2P_TXCLK	
30	GPIO8	RG2_RXCTL	G2_TXD0	M2M_RXDV	M2P_TXEN	RM2M_CRS_DV
31	GPIO9	RG2_RXD0	G2_TXEN	M2M_RXD0	M2P_TXD0	RM2M_RXD0
32	GPIO10	RG2_RXD1	G2_GTXC	M2M_RXD1	M2P_TXD1	RM2M_RXD1
33	GPIO11	RG2_RXD2	-	M2M_RXD2	M2P_TXD2	
34	GPIO12	RG2_RXD3	-	M2M_RXD3	M2P_TXD3	
38	GPIO19	RG1_TXD3	-	M1M_TXD3	M1P_RXD3	
39	GPIO20	RG1_TXD2	-	M1M_TXD2	M1P_RXD2	
40	GPIO21	RG1_TXD1	G2_RXC	M1M_TXD1	M1P_RXD1	RM1M_TXD1
41	GPIO22	RG1_TXD0	G2_RXDV	M1M_TXD0	M1P_RXD0	RM1M_TXD0
42	GPIO23	RG1_TXCTL	G2_RXD0	M1M_TXEN	M1P_RXDV	RM1M_TXEN
43	GPIO24	RG1_TXCLK	G2_RXD1	M1M_TXCLK	M1P_RXCLK	RM1M_CLK
44	GPIO28	RG1_RXCLK	G2_RXD2	M1M_RXCLK	M1P_TXCLK	
45	GPIO29	RG1_RXCTL	G2_RXD3	M1M_RXDV	M1P_TXEN	RM1M_CRS_DV
46	GPIO30	RG1_RXD0	G2_RXD4	M1M_RXD0	M1P_TXD0	RM1M_RXD0
47	GPIO31	RG1_RXD1	G2_RXD5	M1M_RXD1	M1P_TXD1	RM1M_RXD1
48	GPIO32	RG1_RXD2	G2_RXD6	M1M_RXD2	M1P_TXD2	
49	GPIO33	RG1_RXD3	G2_RXD7	M1M_RXD3	M1P_TXD3	

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10.7.1. Extension Ports GMII Mode (1Gbps)

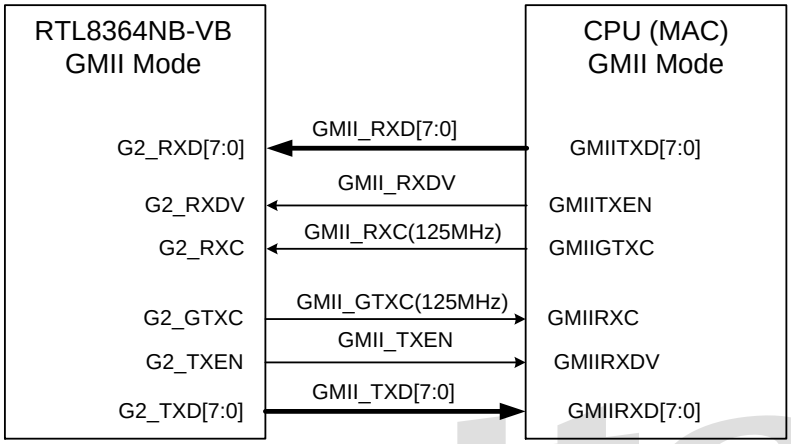


Figure 25. GMII Mode Interface Signal Diagram

Note : The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

10.7.2. Extension Ports RGMII Mode (1Gbps)

The Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB support dual-port RGMII interfaces to an external CPU. The pin numbers and names are shown in Table 21 and Table 22. Figure 26 shows the signal diagram for Extension Port 1 and Extension Port 2 in RGMII interfaces.

Table 21. Extension GMAC1 RGMII Pins

RTL8364NB-VB Pin No.	Type	Extension Port 1 RGMII
38, 39, 40, 41	O	RG1_TXD[3:0]
42	O	RG1_TXCTL
43	O	RG1_TXCLK
44	I	RG1_RXCLK
45	I	RG1_RXCTL
46, 47, 48, 49	I	RG1_RXD[0:3]

Table 22. Extension GMAC2 RGMII Pins

RTL8364NB-VB Pin No.	Type	Extension Port 2 RGMII
23, 24, 25, 26	O	RG2_TXD[3:0]
27	O	RG2_TXCTL
28	O	RG2_TXCLK
29	I	RG2_RXCLK
30	I	RG2_RXCTL
31, 32, 33, 34	I	RG2_RXD[0:3]

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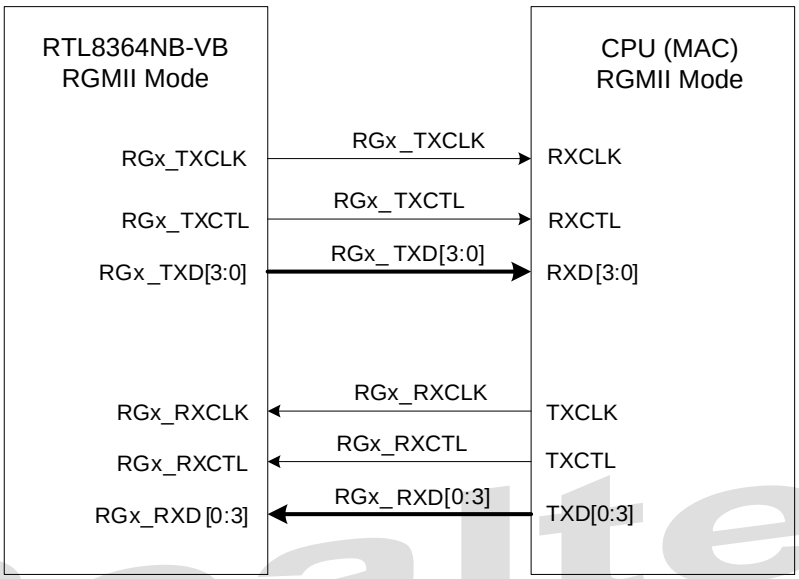


Figure 26. RGMII Mode Interface Signal Diagram

Note : The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

10.7.3. Extension Ports (T)MII MAC/PHY Mode Interface

Both the Extension GMAC1, and Extension GMAC2 of the RTL8364NB-VB support (T)MII MAC/PHY mode interfaces to an external CPU. The pin numbers and names are shown in Table 23, and Table 24.

Figure 27, page 58, shows the signal diagram for the (T)MII PHY mode interface, and Figure 28, page 58, shows the signal diagram for the (T)MAC mode interface.

Table 23. Extension GMAC1 (T)MII Pins

RTL8364NB-VB Pin No.	Type	Extension Port 1 MII MAC Mode	Type	Extension Port 1 MII PHY Mode
38, 39, 40, 41	O	M1M_TXD[3:0]	O	M1P_RXD[3:0]
42	O	M1M_TXEN	O	M1P_RXDV
43	I	M1M_TXCLK	O	M1P_RXCLK
44	I	M1M_RXCLK	O	M1P_TXCLK
45	I	M1M_RXDV	I	M1P_TXEN
46, 47, 48, 49	I	M1M_RXD[0:3]	I	M1P_TXD[0:3]

Table 24. Extension GMAC2 (T)MII Pins

RTL8364NB-VB Pin No.	Type	Extension Port 2 MII MAC Mode	Type	Extension Port 2 MII PHY Mode
23, 24, 25, 26	O	M2M_TXD[3:0]	O	M2P_RXD[3:0]
27	O	M2M_TXEN	O	M2P_RXDV
28	I	M2M_TXCLK	O	M2P_RXCLK
29	I	M2M_RXCLK	O	M2P_TXCLK
30	I	M2M_RXDV	I	M2P_TXEN
31, 32, 33, 34	I	M2M_RXD[0:3]	I	M2P_TXD[0:3]

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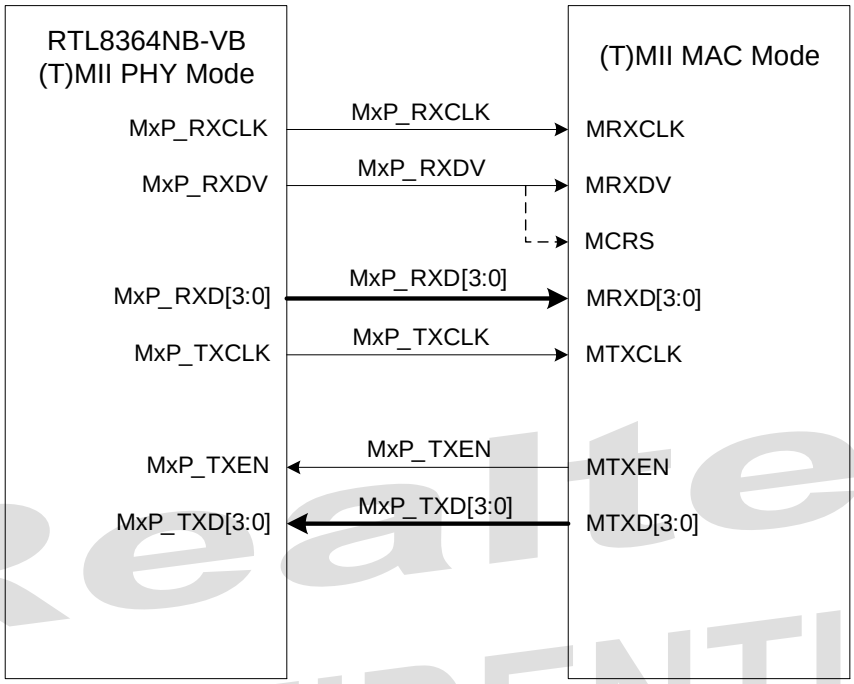


Figure 27. Signal Diagram of (T)MII PHY Mode Interface (100Mbps)

Note : The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

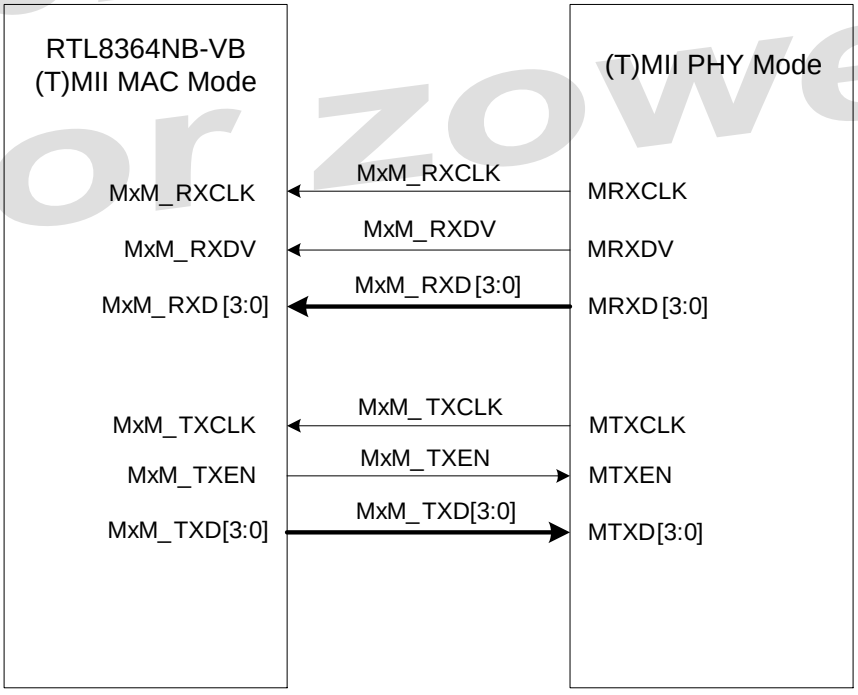


Figure 28. Signal Diagram of (T)MII MAC Mode Interface (100Mbps)

Note : The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

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10.7.4. Extension Ports RMII Clock Input/Output Mode Interface (10/100Mbps)

Both the Extension GMAC1 and Extension GMAC2 of the RTL8364NB-VB support RMII Clock Input/Output mode interfaces to an external CPU.

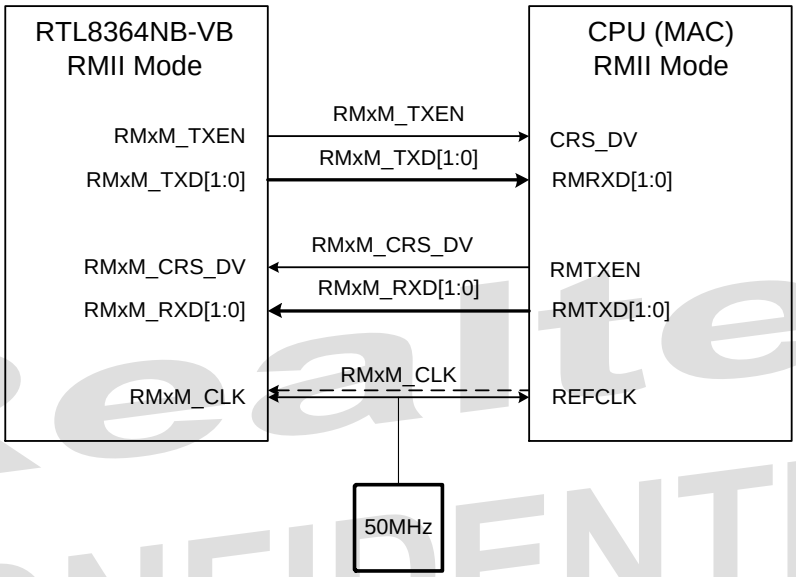


Figure 29. Signal Diagram of RMII Mode (Clock Input Mode)

Note : The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

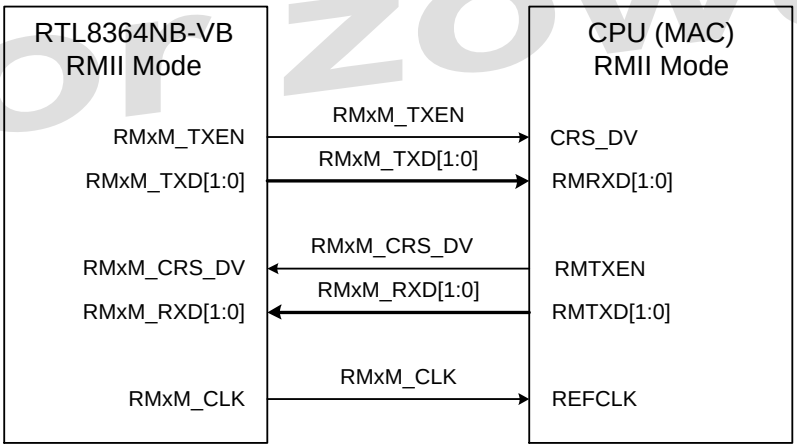


Figure 30. Signal Diagram of RMII Mode (Clock Output Mode)

Note : The termination network on the transmitter (for example, a serial termination resistor) may be used for better signal integrity.

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11. Electrical Characteristics

11.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 25. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO_0, DVDDIO_1, DVDDIO_2, DVDDIO_3 AVDDH, Supply Referenced to GND and AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, SVDDL, PLLVDDL, Supply Referenced to GND, AGND, and PLLGND.	GND-0.3	+1.21	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

11.2. Recommended Operating Range

Table 26. Recommended Operating Range

Parameter		Min	Typical	Max	Units
Ambient Operating Temperature (Ta)		0	-	70	°C
AVDDH Supply Voltage Range		3.135	3.3	3.465	V
DVDDIO_0, DVDDIO_3 Supply Voltage Range	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
	1.8V	1.710	1,8	1.890	
DVDDIO_2 Supply Voltage Range (DVDDIO_2: Extension Port 2 Supports 2.5V or 3.3V)	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
DVDDIO_1 Supply Voltage Range (DVDDIO_1: Extension Port 1 Supports 1.8V, 2.5V, or 3.3V)	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
	1.8V	1.710	1,8	1.890	V
DVDDL, AVDDL, SVDDL, PLLVDDL Supply Voltage Range		1.045	1.1	1.155	V

Note: When DVDDIO_0 is in 1.8V mode, the parallel LED pin of the RTL8364NB-VB maybe cannot able to drive the parallel LED directly.

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11.3. Thermal Characteristics

11.3.1. Assembly Description

Table 27. Assembly Description

Package	Type	QFN88
	Dimension (L ×W)	10 ×10mm
	Thickness	0.65mm
PCB	PCB Dimension (L ×W)	70x87 mm
	PCB Thickness	1.6mm
	Number of Cu Layer-PCB	2-Layer: - Top layer (1oz): 20% coverage of Cu - Bottom layer (1oz): 75% coverage of Cu 4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

11.3.2. Material Properties

Table 28. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.88
PCB		Cu	400
		FR4	0.2

11.3.3. Simulation Conditions

Table 29. Simulation Conditions

Input Power	1W
Test Board (PCB)	2L (2S)/4L (2S2P)
Control Condition	Air Flow = 0 m/s

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11.3.4. Thermal Performance of QFN-88 on PCB Under Still Air Convection

Table 30. Thermal Performance of QN-88 on PCB Under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}
4L PCB	23.7	6.29	8.9	0.23
2L PCB	27.8	7.81	9.5	0.27

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB}: Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JT}: Junction-to-top-center thermal characterization parameter

11.4. DC Characteristics

Table 31. DC Characteristics

Parameter	SYM	Min	Typical	Max	Unit	Note
Power Supply Current for RGMII1 DVDDIO_1 (2.5V) (For General Purpose Interface) (1000M Active)	I_{DVDDIO_1}	-	28	-	mA	
Power Supply Current for RGMII1 DVDDIO_2 (2.5V) (For General Purpose Interface) (1000M Active)	I_{DVDDIO_2}	-	25	-	mA	
Power Supply Current for RGMII1 DVDDIO_1 (3.3V) (For General Purpose Interface) (1000M Active)	I_{DVDDIO_1}	-	43	-	mA	
Power Supply Current for RGMII1 DVDDIO_2 (3.3V) (For General Purpose Interface) (1000M Active)	I_{DVDDIO_2}	-	35	-	mA	
Power Supply Current for RGMII1 DVDDIO_1 (1.8V) (For General Purpose Interface) (1000M Active)	I_{DVDDIO_1}	-	18	-	mA	
System Idle (All UTP Port Link Down, without LEDs)						
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	17	-	mA	
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	59	-	mA	
1000M Active (All UTP Ports Link/Active, and 2 Extension Port Configured as RGMII, without LEDs)						
Power Supply Current for VDDH	I_{DVDDIO_0}, I_{DVDDIO_3}, I_{AVDDH}	-	128	-	mA	1
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	245	-	mA	
1000M Active (All UTP Ports Link/Active, and 2 Extension Port Configured as RGMII+HSGMII, without LEDs)						
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	131	-	mA	2
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, I_{SVDDL}, $I_{PLLVDDL}$	-	330	-	mA	
VDDIO=3.3V						
TTL Input High Voltage	V_{ih}	2.0	-	-	V	
TTL Input Low Voltage	V_{il}	-	-	0.7	V	
Output High Voltage	V_{oh}	2.7	-	-	V	
Output Low Voltage	V_{ol}	-	-	0.6	V	
VDDIO=2.5V						
TTL Input High Voltage	V_{ih}	1.7	-	-	V	

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TTL Input Low Voltage	V_{il}	-	-	0.6	V	V
Output High Voltage	V_{oh}	2.25	-	-	V	V
Output Low Voltage	V_{ol}	-	-	0.4	V	V
VDDIO=1.8V						
TTL Input High Voltage	V_{ih}	1.2	-	-	V	V
TTL Input Low Voltage	V_{il}	-	-	0.6	V	V
Output High Voltage	V_{oh}	1.45	-	-	V	V
Output Low Voltage	V_{ol}	-	-	0.4	V	V

Note 1: Both I_{DVDDIO_1} & I_{DVDDIO_2} should be added to the total current consumption when the dual extension ports of the RTL8364NB-VB are configured to RGMII mode.

Note 2: I_{DVDDIO_1} or I_{DVDDIO_2} should be added to the total current consumption when the extension ports of the RTL8364NB-VB are configured to RGMII+HSGMII mode.

11.5. AC Characteristics

11.5.1. I²C Master for EEPROM Auto-load Interface Timing Characteristics

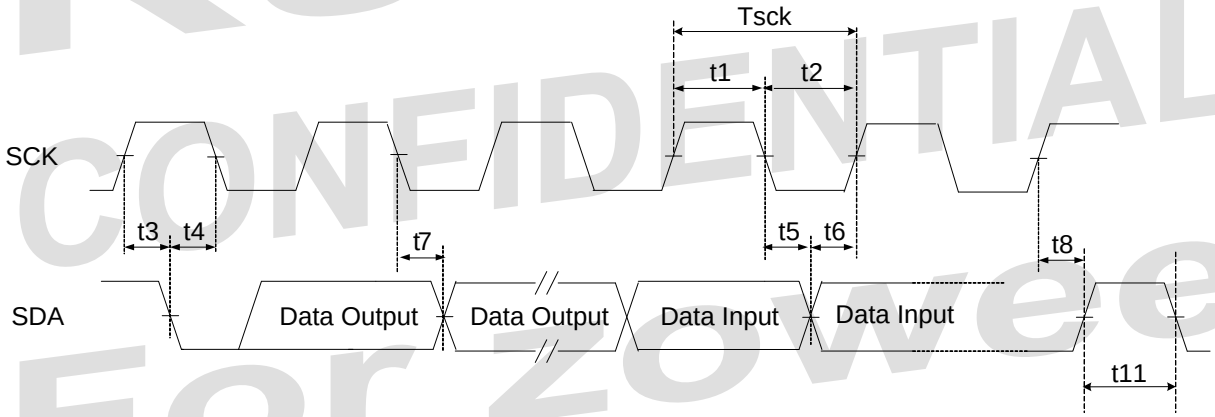


Figure 31. Master I2C for EEPROM Auto-load Timing Characteristics

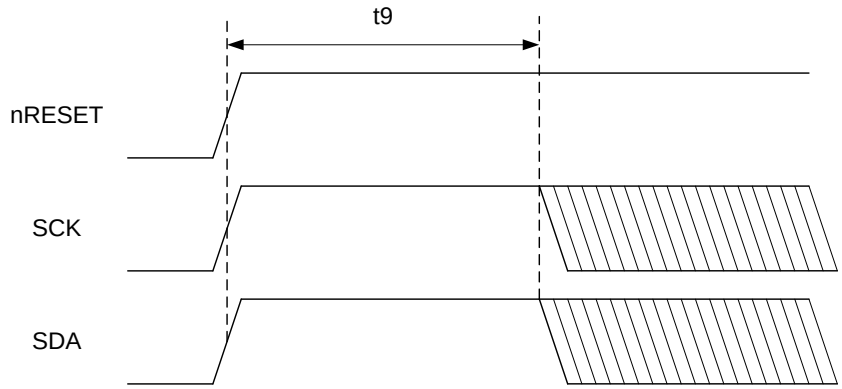


Figure 32. SCK/SDA Power on Timing

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Table 32. Master I2C for EEPROM Auto-load Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
Tsck	SCK Clock Period	O	-	9	-	µs
t1	SCK High Time	O	4.05	4.5	-	µs
t2	SCK Low Time	O	4.05	4.5	-	µs
t3	START Condition Setup Time	O	2	-	-	µs
t4	START Condition Hold Time	O	2	-	-	µs
t5	Data Input Hold Time	O	0	-	-	µs
t6	Data Input Setup Time	O	10	-	-	µs
t7	Data output delay	O	2.15	-	2.35	µs
t8	STOP Condition Setup Time	O	2	-	-	µs
t9	SCK/SDA Active from Reset Ready	O	-	76.8	-	ms
t11	Time the bus free before new START	O	10	-	-	µs
-	SCK Rise Time (10% to 90%)	O	-	-	100	ns
-	SCK Fall Time (90% to 10%)	O	-	-	100	ns
-	Duty Cycle	O	40	50	60	%

11.5.2. Realtek/LSB/MSB I²C-like Slave Mode Timing Characteristics

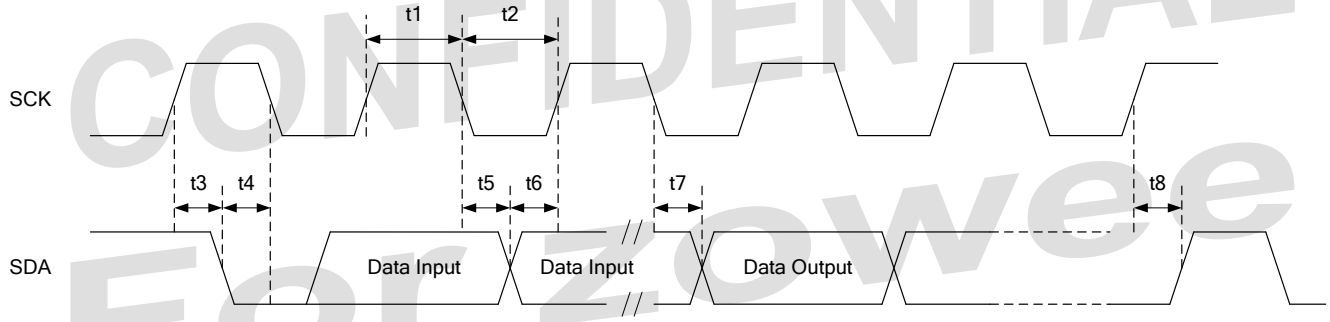


Figure 33. Realtek/LSB/MSB I2C-like Slave Mode Timing Characteristics

Table 33. Realtek/LSB/MSB I2C-like Slave Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	250	-	-	ns
t2	SCK Low Time	I	250	-	-	ns
t3	START Condition Setup Time	I	150	-	-	ns
t4	START Condition Hold Time	I	150	-	-	ns
t5	Data Hold Time	I	150	-	-	ns
t6	Data Setup Time	I	150	-	-	ns
t7	Clock to Data Output Delay	O	10	-	100	ns
t8	STOP Condition Setup Time	I	150	-	-	ns

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11.5.3. Slave MII Management SMI for External CPU Access Interface Timing Characteristics

The RTL8364NB-VB supports MDIO slave mode. The Master (CPU) can access the Slave (RTL8364NB-VB) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the master sources the MDIO signal. In a read command, the slave sources the MDIO signal.

- The timing characteristics t1, t2, and t3 (Table 34) of the Master (the RTL8364NB-VB link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics t4 (Table 34) of the Slave (RTL8364NB-VB) are provided by the RTL8364NB-VB when the RTL8364NB-VB sources the MDIO signal (Read command)

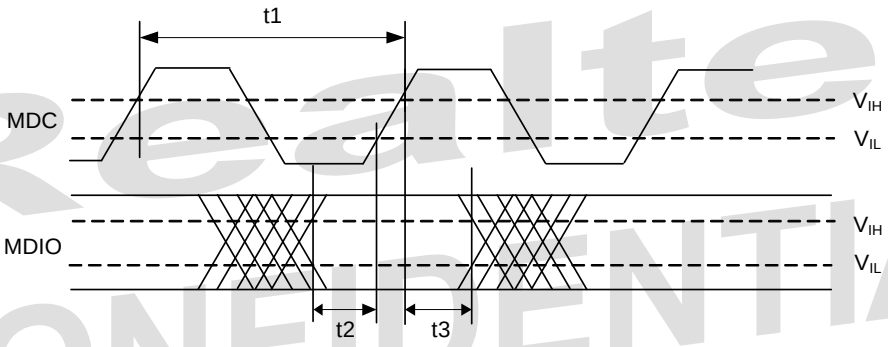


Figure 34. MDIO Sourced by the Master

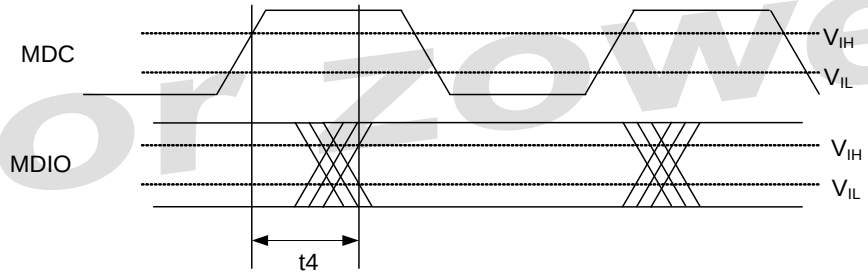


Figure 35. MDIO Sourced by the RTL8364NB-VB (Slave)

Table 34. MDIO Timing Characteristics and Requirement

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	8	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	8	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Rising Edge) to Data Delay Time	O	0	-	80	ns

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11.5.4. (T)MII MAC Mode Timing

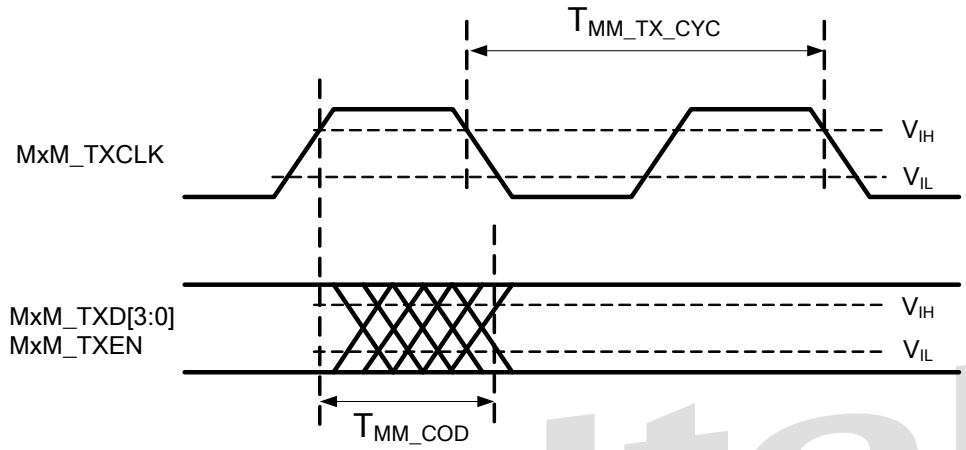


Figure 36. (T)MII MAC Mode Clock to Data Output Delay Timing

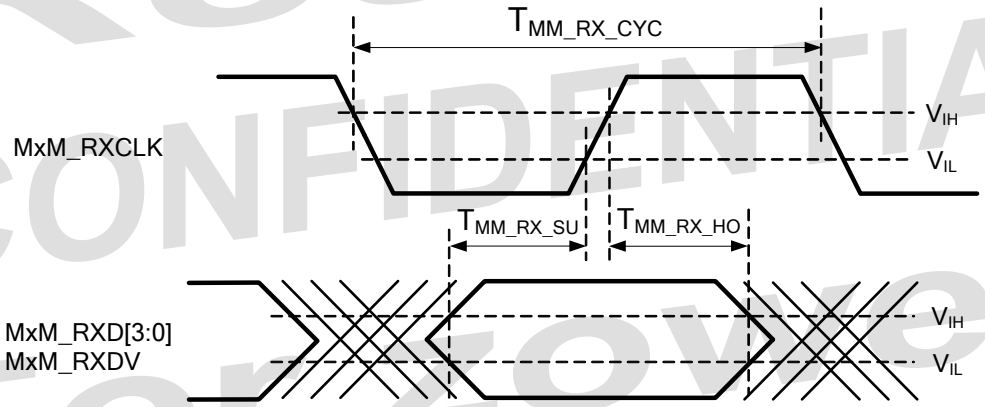


Figure 37. (T)MII MAC Mode Input Timing

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Table 35. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-TX MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM_TX_CYC}$ $T_{MM_RX_CYC}$	25MHz Clock Input.	I	-	40	-	ns
10Base-T MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM_TX_CYC}$ $T_{MM_RX_CYC}$	2.5MHz Clock Input.	I	-	400	-	ns
MxM_TXCLK to MxM_TXD[3:0] and MxM_TXEN Output Delay Time	T_{MM_COD}	-	O	2	-	8	ns
MxM_RXD[3:0], MxM_RXDV, and MxM_CRS Input Setup Time	$T_{MM_RX_SU}$	-	I	10	-	-	ns
MxM_RXD[3:0] and MxM_RXDV Input Hold Time	$T_{MM_RX_HO}$	-	I	10	-	-	ns

Table 36. TMII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-TX MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM_TX_CYC}$ $T_{MM_RX_CYC}$	25MHz Clock Input.	I	-	20	-	ns
10Base-T MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM_TX_CYC}$ $T_{MM_RX_CYC}$	2.5MHz Clock Input.	I	-	200	-	ns
MxM_TXCLK to MxM_TXD[3:0] and MxM_TXEN Output Delay Time	T_{MM_COD}	-	O	2	-	8	ns
MxM_RXD[3:0], MxM_RXDV, and MxM_CRS Input Setup Time	$T_{MM_RX_SU}$	-	I	5	-	-	ns

11.5.5. (T)MII PHY Mode Timing

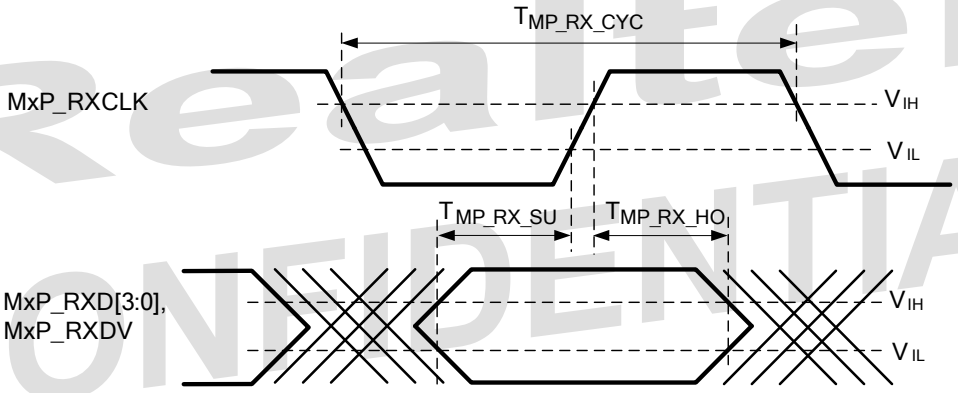


Figure 38. (T)MII PHY Mode Output Timing

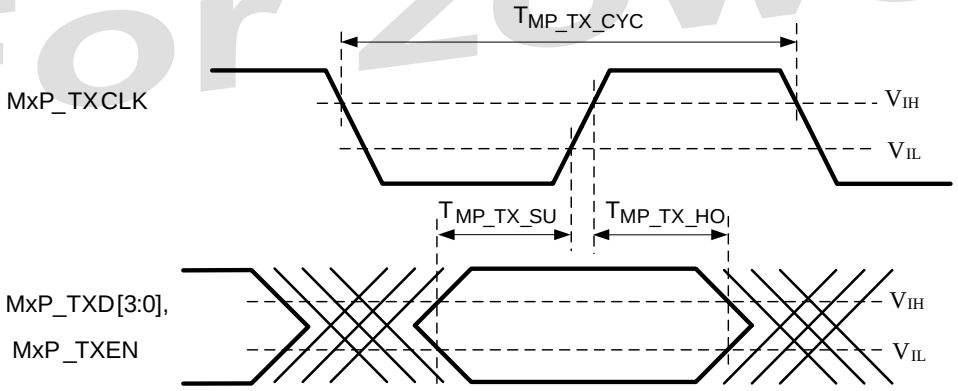


Figure 39. (T)MII PHY Mode Input Timing

Table 37. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP_RX_CYC}$ $T_{MP_TX_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP_RX_CYC}$ $T_{MP_TX_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns

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Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Setup Time	$T_{MP_RX_SU}$	-	O	14	-	-	ns
100M MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Hold Time	$T_{MP_RX_HO}$	-	O	16	-	-	ns
M1P_TXD[3:0], M1P_TXEN to M1P_TXC Input Setup Time	$T_{MP_TX_SU}$	-	I	6	-	-	ns
M1P_TXD[3:0], M1P_TXEN to M1P_TXC Input Hold Time	$T_{MP_TX_HO}$	-	I	0	-	-	ns

Table 38. TMII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP_RX_CYC}$ $T_{MP_TX_CYC}$	25MHz Clock Output.	O	-	20	-	ns
MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP_RX_CYC}$ $T_{MP_TX_CYC}$	2.5MHz Clock Output.	O	-	200	-	ns
MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Setup Time	$T_{MP_RX_SU}$	-	O	7	-	-	ns
MxP_RXD[3:0] and MxP_RXDV to MxP_RXCLK Output Hold Time	$T_{MP_RX_HO}$	-	O	8	-	-	ns
MxP_TXD[3:0], MxP_TXEN to MxP_TXC Input Setup Time	$T_{MP_TX_SU}$	-	I	6	-	-	ns
MxP_TXD[3:0], MxP_TXEN to MxP_TXC Input Hold Time	$T_{MP_TX_HO}$	-	I	0	-	-	ns

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11.5.6. RMII Clock Input Mode Timing

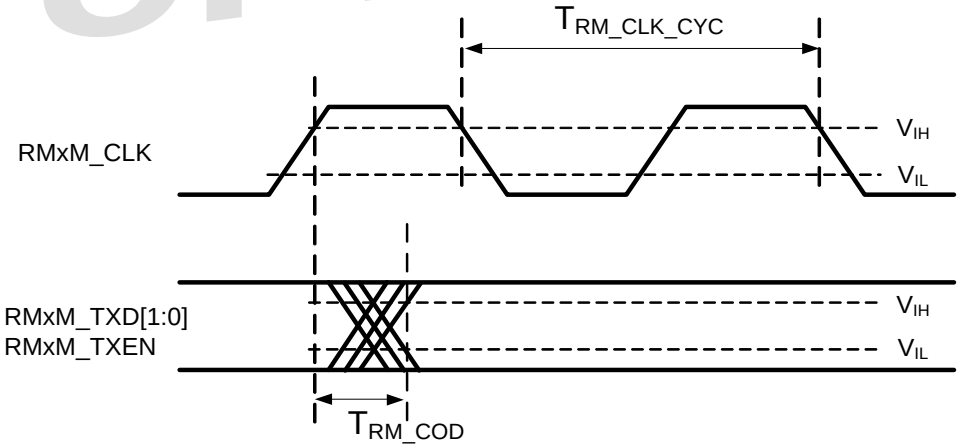


Figure 40. RMII Clock Input Mode Clock to Data Output Delay Timing

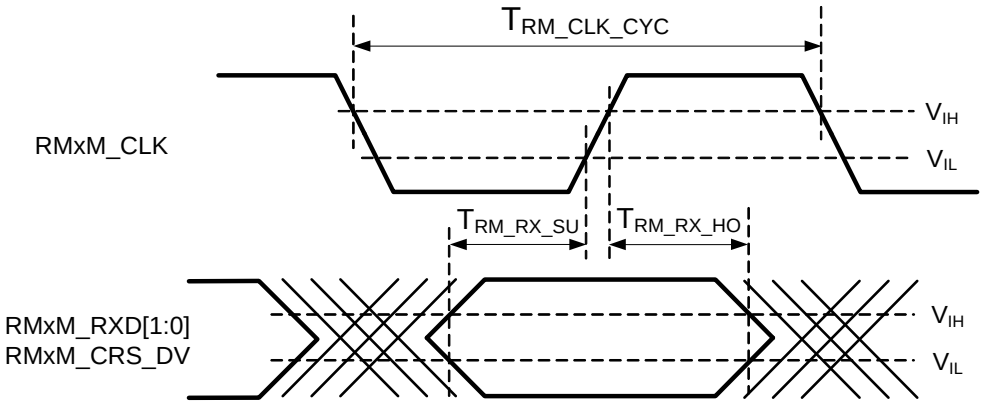


Figure 41. RMII Clock Input Mode Input Timing

Table 39. RMII Clock Input Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
RMxM_CLK Input Cycle Time	$T_{RM_CLK_CYC}$	50MHz Clock Input.	I	-	20	-	ns
RMxM_CLK Input to RMxM_TXD[1:0], MxM_TXEN Output Delay Time	T_{RM_COD}	-	O	2	-	10.5	ns
RMxM_RXD[1:0], RMxM_CRS_DV Input Setup Time	$T_{RM_RX_SU}$	-	I	4	-	-	ns
RMxM_RXD[1:0], RMxM_CRS_DV Input Hold Time	$T_{RM_RX_HO}$	-	I	3	-	-	ns

11.5.7. RMII Clock Output Mode Timing

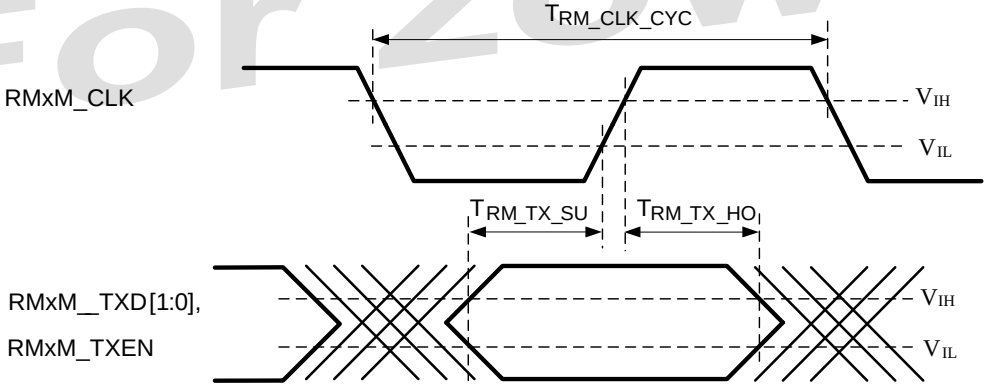


Figure 42. RMII Clock Output Mode Output Timing

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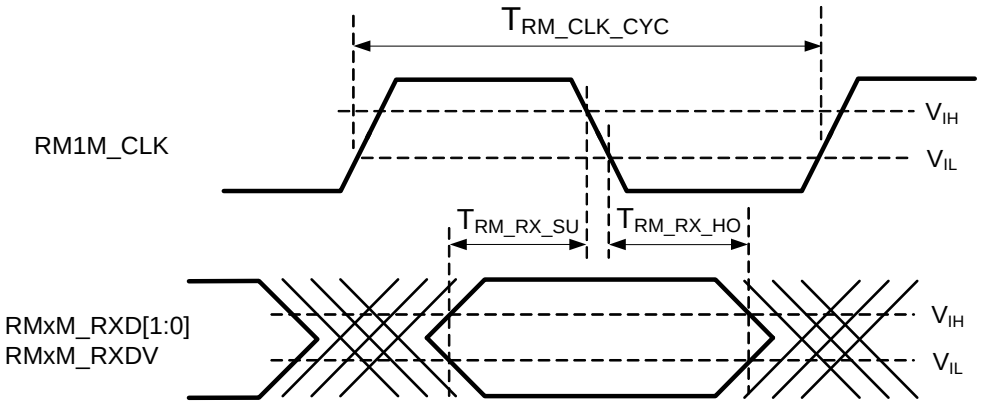


Figure 43. RMII Clock Output Mode Input Timing

Table 40. RMII Clock Output Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
RMxM_CLK Output Cycle Time	$T_{RM_CLK_CYC}$	50MHz Clock Output.	O	-	20	-	ns
RMxM_CLK Duty cycle	-	-	O	45	50	55	%
RMxM_RXD[3:0], and RMxM_ CRS_DV to RMxM_CLK Output Setup Time	$T_{RM_TX_SU}$	-	O	5	-	-	ns
RMxM_TXD[1:0], and RMxM_TXEN to RMxM_CLK Output Hold Time	$T_{RM_TX_HO}$	-	O	8	-	-	ns
RMxM_RXD[1:0], RMxM_CRS_DV Input Setup Time	$T_{RM_RX_SU}$	-	I	4	-	-	ns
RMxM_RXD[1:0], RMxM_CRS_DV Input Hold Time	$T_{RM_RX_HO}$	-	I	0	-	-	ns

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11.5.8. RGMII Timing Characteristics

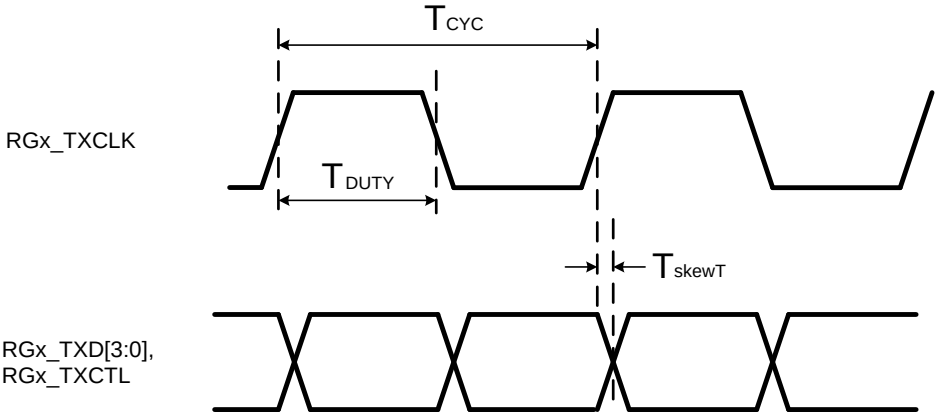


Figure 44. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=0)

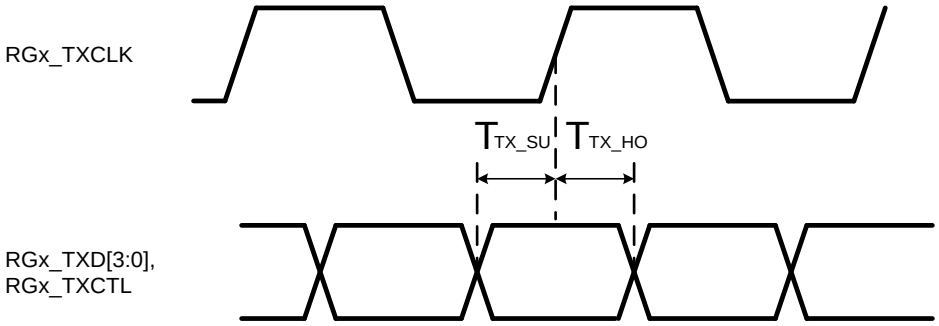


Figure 45. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=2ns)

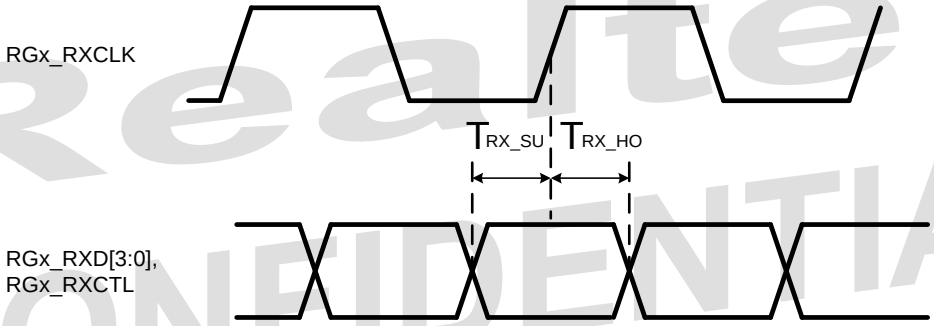


Figure 46. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=0)

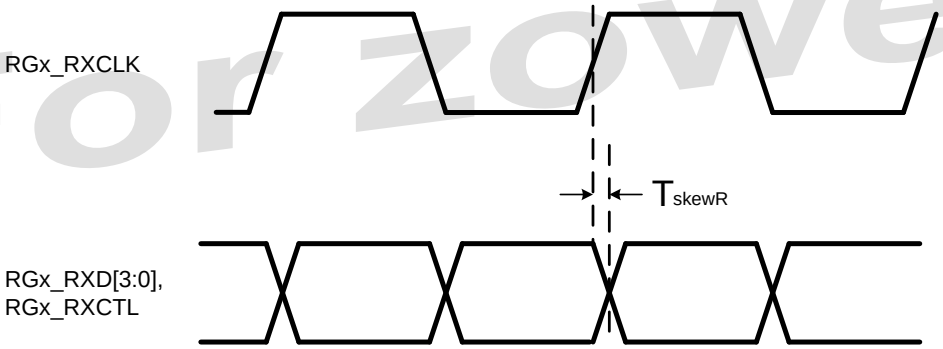


Figure 47. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=2ns)

Table 41. RGMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000M RGx_TXCLKc Output Cycle Time	T_{TX_CYC}	125MHz Clock Output. Refer to Figure 44, page 70.	O	7.6	8	8.6	ns
100M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	25MHz Clock Output. Refer to Figure 44, page 70.	O	38	40	42	ns
10M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	2.5MHz Clock Output. Refer to Figure 44, page 70.	O	380	400	420	ns

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Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Skew	T_{skewT}	Disable Output Clock Delay. (RGx_TXCLK_DELAY=0). Refer to Figure 44, page 70.	O	-500		500	ps
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Setup Time	T_{TX_SU}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 45, page 71.	O	1.2		-	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Hold Time	T_{TX_HO}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 45, page 71.	O	1.2		-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Setup Time	T_{RX_SU}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 46, page 71.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Hold Time	T_{RX_HO}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 46, page 71.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Skew	T_{skewR}	Enable Input Clock Delay. (RGx_RXCLK_DELAY=1). Refer to Figure 47, page 71.	I	-600	-	600	ps

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11.5.9. GMII Timing Characteristics

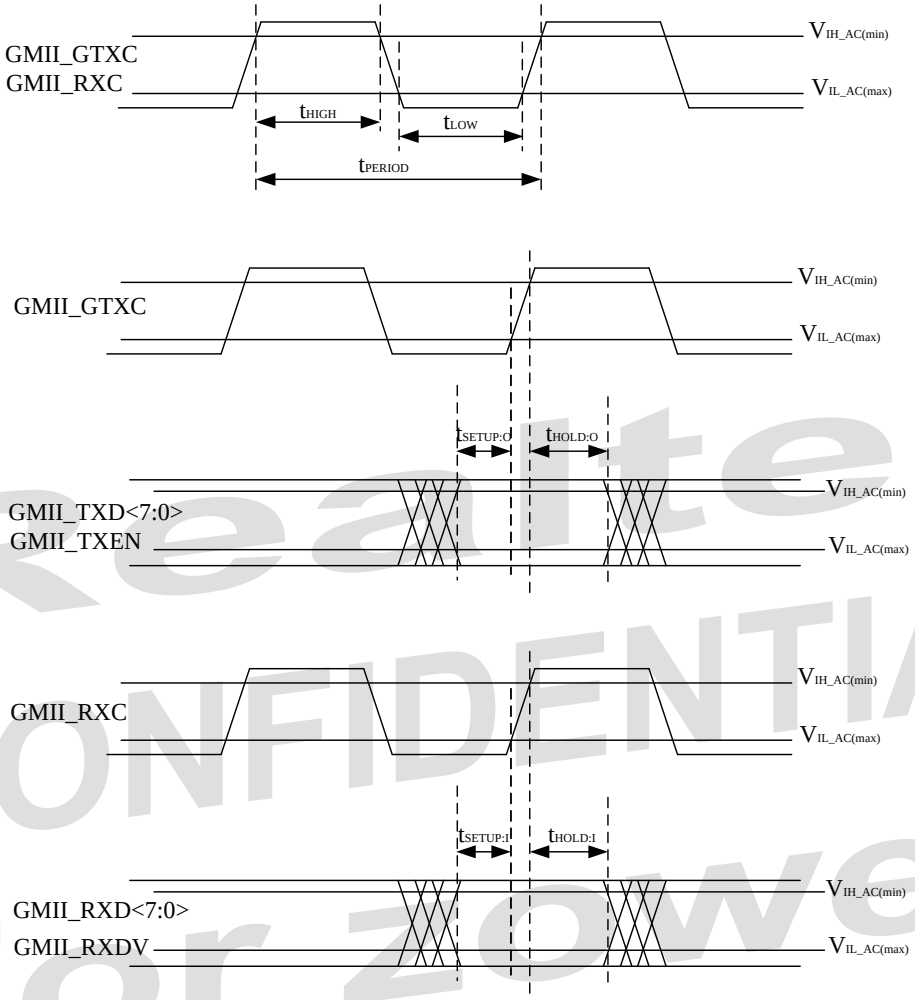


Figure 48. GMII Mode Timing Characteristics

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Table 42. GMII I/O DC characteristics

Parameter	SYM	MIN	TYPICAL	MAX	UNITS
Input High Voltage	V_{ih}	1.7	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.9	V

Note: I/O power DVDDIO_1 & DVDDIO_2=3.3V

Table 43. GMII Mode Timing characteristics

SYM	Parameter	I/O	Min	Typ	Max	Units
t_{txcyc}	1000M GMII Mode GMII_GTXC	O	7.5	8.0	8.5	ns
t_{rxcyc}	1000M GMII Mode GMII_RXC	I	7.5	-	-	ns
t_{HIGH}	GMII_GTXC, GMII_RXC Time High	-	2.5	-	-	ns
t_{LOW}	GMII_GTXC, GMII_RXC Time Low	-	2.5	-	-	ns
t_R	GMII_GTXC, GMII_RXC Rise Time	-	-	-	1.0	ns
t_F	GMII_GTXC, GMII_RXC Fall Time	-	-	-	1.0	ns
$t_{SETUP}O$	GMII_TXD[7:0], GMII_TXEN, Setup Time	O	2.5	-	-	ns

SYM	Parameter	I/O	Min	Typ	Max	Units
$t_{HOLD}O$	GMII_TXD[7:0], GMII_TXEN Hold Time	O	0.5	-	-	ns
$t_{SETUP}I_{(RCVR)}$	GMII_RXD[7:0], GMII_RXDV Setup Time	I	2.0	-	-	ns
$t_{HOLD}I_{(RCVR)}$	GMII_RXD[7:0], GMII_RXDV Hold Time	I	0.0	-	-	ns

11.5.10. HSGMII Characteristics

Table 44. HSGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	319.904	320	320.096	ps	320ps ±300ppm
T_X1	Eye Mask	-	-	0.175	UI	-
T_X2	Eye Mask	-	-	0.39	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	500	700	1000	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.65	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.35	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

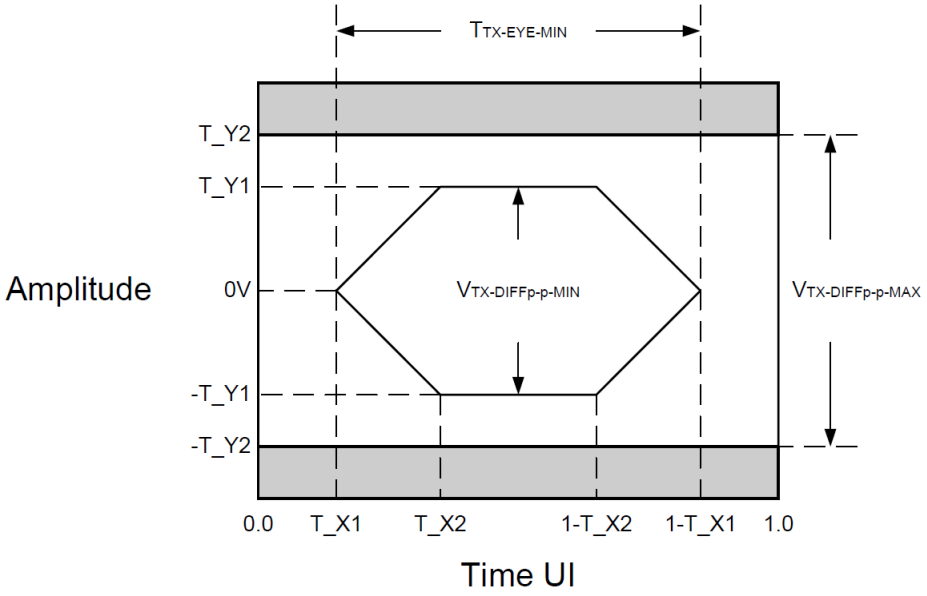


Figure 49. HSGMII Differential Transmitter Eye Diagram

Table 45. HSGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	319.904	320	320.096	ps	320ps ±300ppm
R_X1	Eye Mask	-	-	0.25	UI	-

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Symbol	Parameter	Min	Typical	Max	Units	Notes
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.5	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.5	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

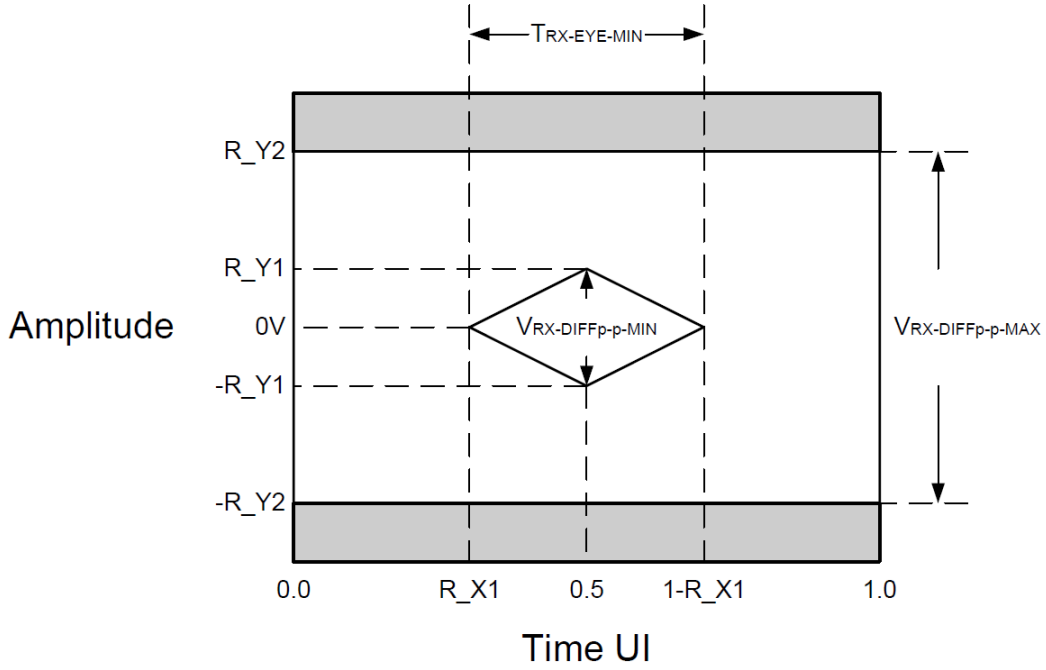


Figure 50. HSGMII Differential Receiver Eye Diagram

11.5.11. SGMII Characteristics

Table 46. SGMII Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ±300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	500	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	700	900	mV	
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-

Symbol	Parameter	Min	Typical	Max	Units	Notes
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

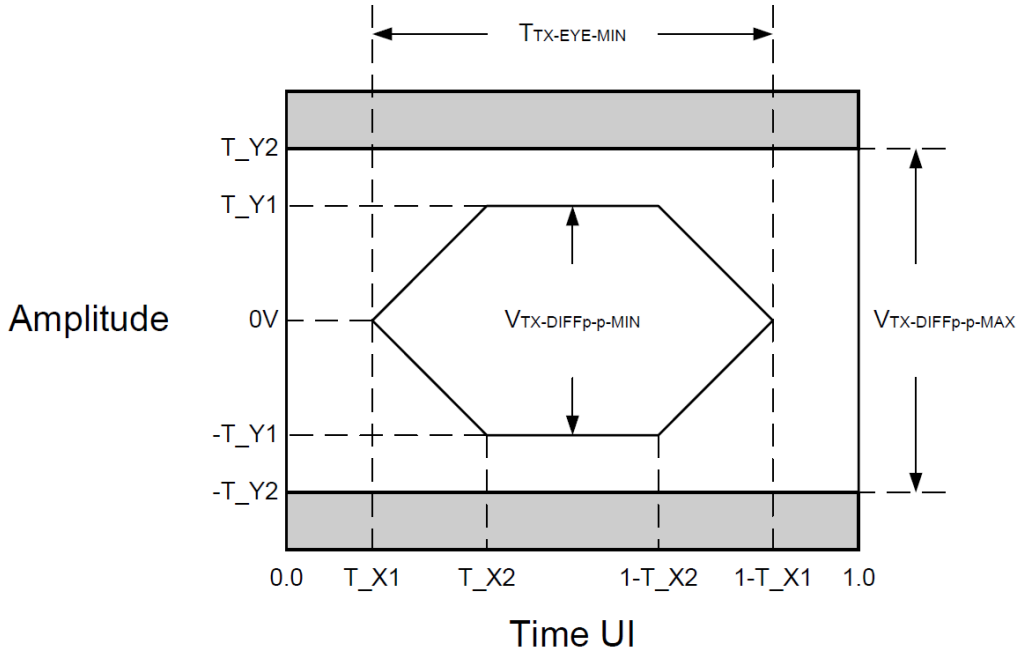


Figure 51. SGMII Differential Transmitter Eye Diagram

Table 47. SGMII Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval	799.76	800	800.24	ps	800ps ±300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	50	-	-	mV	-
R_Y2	Eye Mask	-	-	600	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	100	-	1200	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

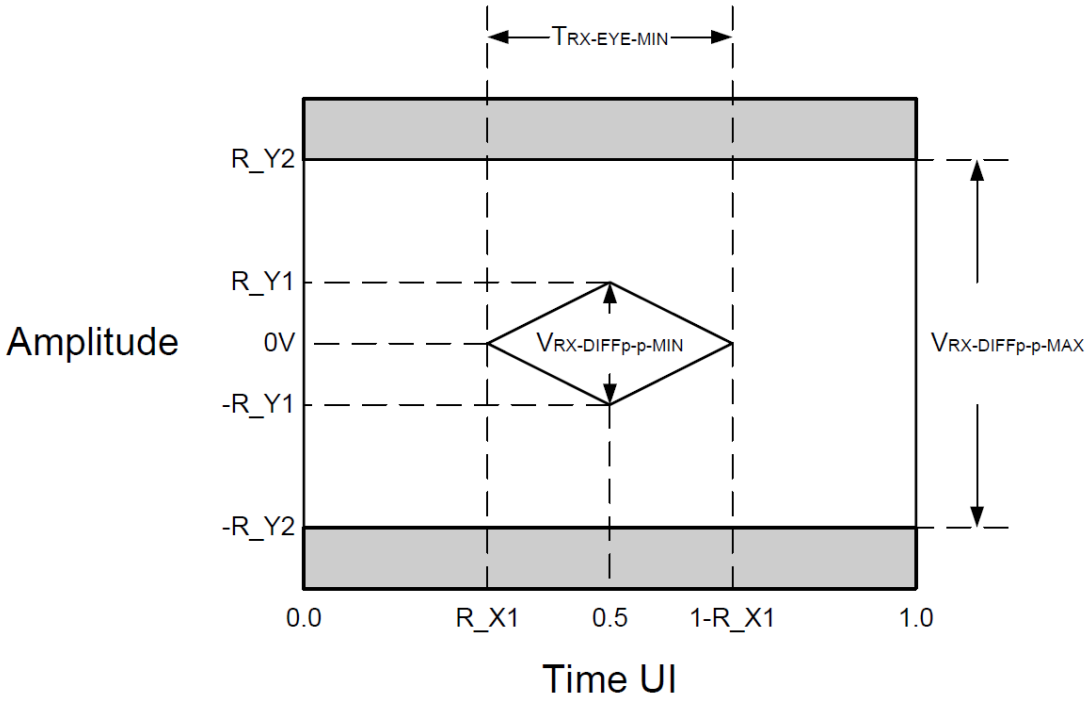


Figure 52. 1000Base-X/SGMII Differential Receiver Eye Diagram

11.5.12. 1000Base-X/100Base-FX Differential Transmitter Characteristics

Table 48. 1000Base-X/100Base-FX Differential Transmitter Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval (1000Base-X)	799.76	800	800.24	ps	800ps ±300ppm
	Unit Interval (100Base-FX)	7.9976	8.0	8.0024	ns	8ns ±300ppm
T_X1	Eye Mask	-	-	0.1875	UI	-
T_X2	Eye Mask	-	-	0.4	UI	-
T_Y1	Eye Mask	200	-	-	mV	-
T_Y2	Eye Mask	-	-	650	mV	-
$V_{TX-DIFFp-p}$	Output Differential Voltage	400	800	1300	mV	-
T_{TX-EYE}	Minimum TX Eye Width	0.625	-	-	UI	-
$T_{TX-JITTER}$	Output Jitter	-	-	0.375	UI	-
R_{TX}	Differential Resistance	80	100	120	ohm	-
C_{TX}	AC Coupling capacitor	75	100	200	nF	-
L_{TX}	Transmit Length in PCB	-	-	10	inch	-

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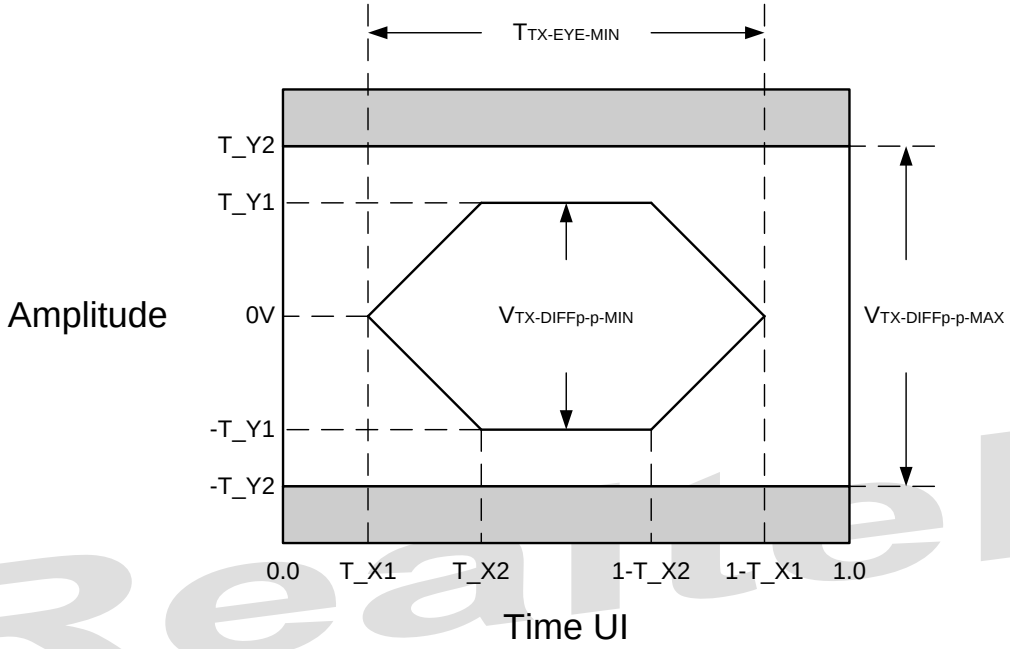


Figure 53. 1000Base-X/100Base-FX Differential Transmitter Eye Diagram

11.5.13. 1000Base-X/100Base-FX Differential Receiver Characteristics

Table 49. 1000Base-X/100Base-FX Differential Receiver Characteristics

Symbol	Parameter	Min	Typical	Max	Units	Notes
UI	Unit Interval (1000Base-X)	799.76	800	800.24	ps	800ps ±300ppm
	Unit Interval (100Base-FX)	7.9976	8.0	8.0024	ns	8ns ±300ppm
R_X1	Eye Mask	-	-	0.3125	UI	-
R_Y1	Eye Mask	100	-	-	mV	-
R_Y2	Eye Mask	-	-	1000	mV	-
$V_{RX-DIFFp-p}$	Input Differential Voltage	200	-	2000	mV	-
T_{RX-EYE}	Minimum RX Eye Width	0.375	-	-	UI	-
$T_{RX-JITTER}$	Input Jitter Tolerance	-	-	0.625	UI	-
R_{RX}	Differential Resistance	80	100	120	ohm	-

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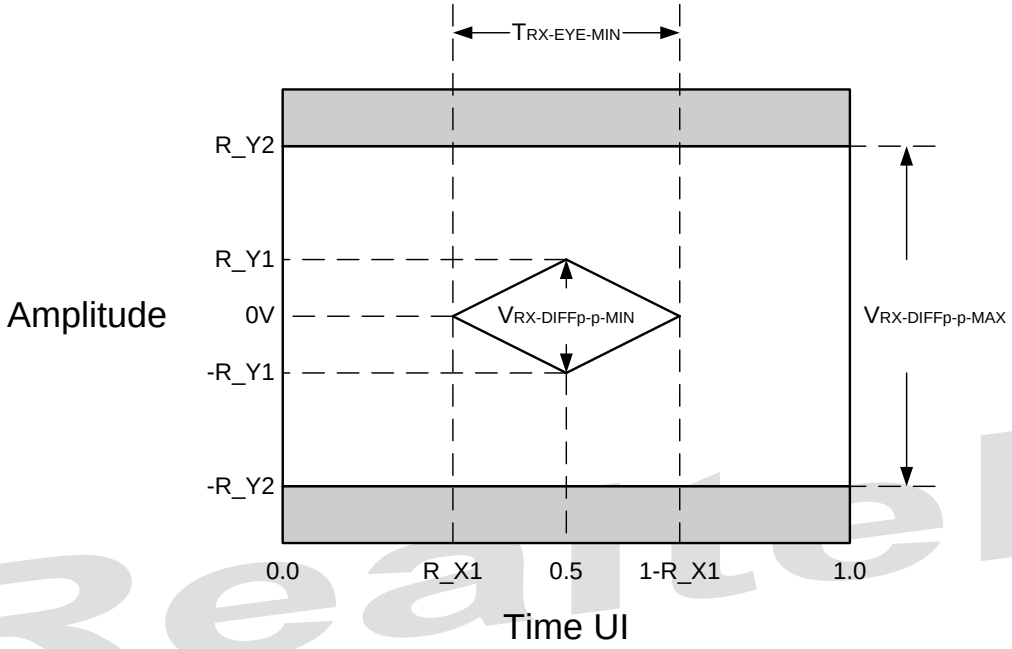


Figure 54. 1000Base-X/100Base-FX Differential Receiver Eye Diagram

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11.6. Power and Reset Characteristics

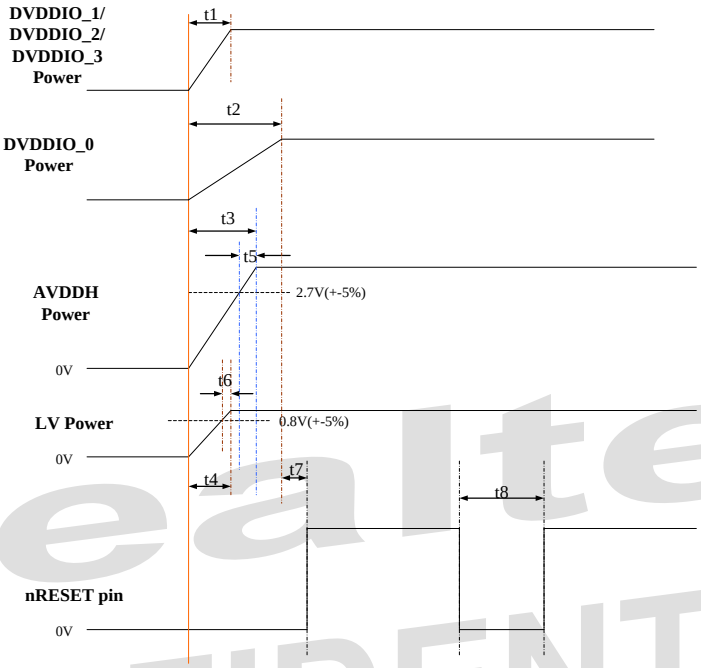


Figure 55. Power and Reset Characteristics

Table 50. Power and Reset Characteristics

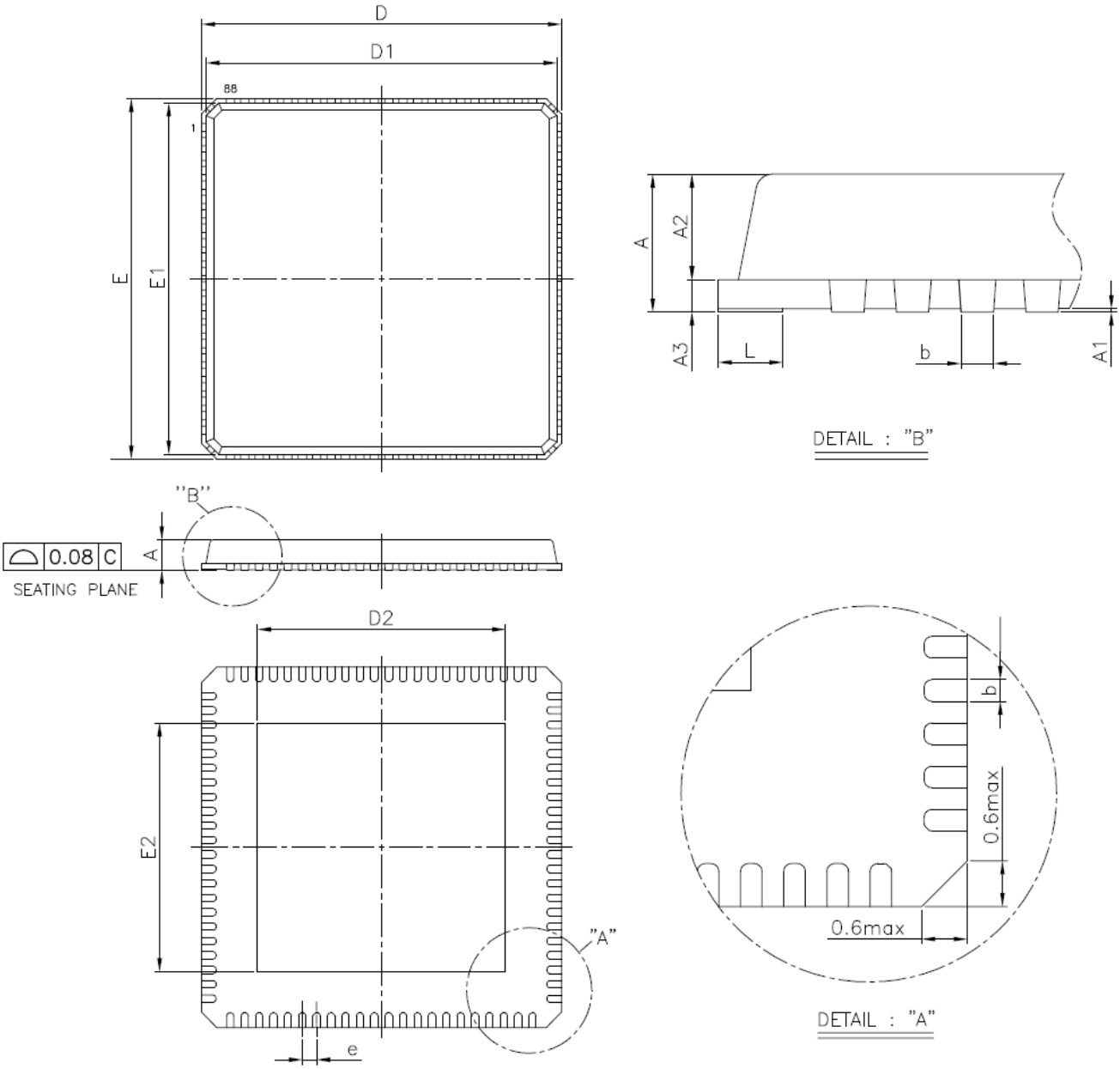
Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
DVDDIO_1/DVDDIO_2/ DVDDIO_3 Rising Time	t1	DVDDIO_1/DVDDIO_2/DVDDIO_3 power rise settling time	I	0.5	-	-	ms
DVDDIO_0 Rising Time	t2	DVDDIO power rise settling time	I	0.5	-	-	ms
HV Power Rising Time	t3	AVDDH power rise settling time	I	0.5	-	-	ms
LV Power Rising Time	t4	DVDDL and AVDDL power rise settling time	I	0.5	-	-	ms
HV Power Ready Time after more than HV POR threshold	t5	The duration from HV power more than HV POR threshold to HV power ready	I	-	-	10	ms
LV Power Ready Time after more than LV POR threshold	t6	The duration from LV power more than LV POR threshold to LV power ready	I	-	-	10	ms
Reset Delay Time	t7	The duration from 'all power steady' to the reset signal released to high	I	10	-	-	ms
Reset Low Time	t8	The duration of reset signal remaining low time before issuing a reset to RTL8364NB-VB	I	10	-	-	ms

Note: If the powers supply voltage of the RTL8364NB-VB lower than normal operation condition happened, the Power On Reset (POR) or Pin Reset be needed for normal operation of the RTL8364NB-VB.

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12. Mechanical Dimensions

Thermally Enhanced Quad Flat Package (QFN) 88 Leads 10×10mm Outline.



12.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		10.00BSC			0.394BSC	
D_1/E_1		9.75BSC			0.384BSC	
D_2/E_2	6.65	6.90	7.15	0.262	0.272	0.282
e		0.40BSC			0.016BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

CONTROLLING DIMENSION: MILLIMETER (mm).
REFERENCE DOCUMENT: JEDEC MO-220.

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13. Ordering Information

Table 51. Ordering Information

Part Number	Package	Status
RTL8364NB-VB-CG	QFN 88-Pin 'Green' Package	Mass Production

Note: See page 16 for package identification.

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