

## -40V P-Channel Enhancement Mode MOSFET

### Description

The AP40P04DF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = -40V$   $I_D = -40A$

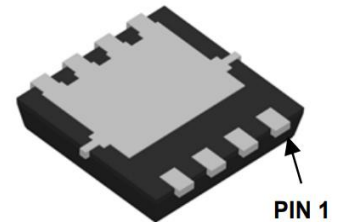
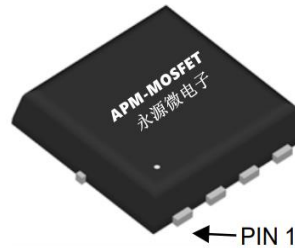
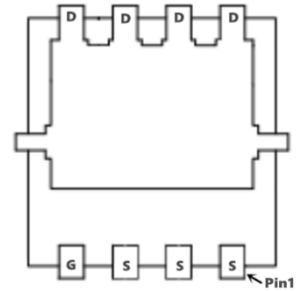
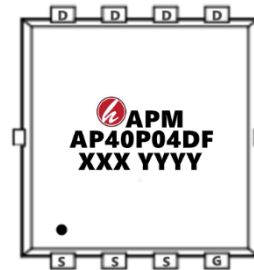
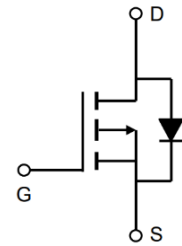
$R_{DS(ON)} < 18m\Omega$  @  $V_{GS} = -10V$  (Type:  $15m\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40P04DF	PDFN3*3-8L	AP40P04DF XXX YYYY	5000

### Absolute Maximum Ratings (TC=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V <sup>1</sup>	-40	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V <sup>1</sup>	-23	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-120	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	125	mJ
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	25	W
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	16	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	5	°C/W

## -40V P-Channel Enhancement Mode MOSFET

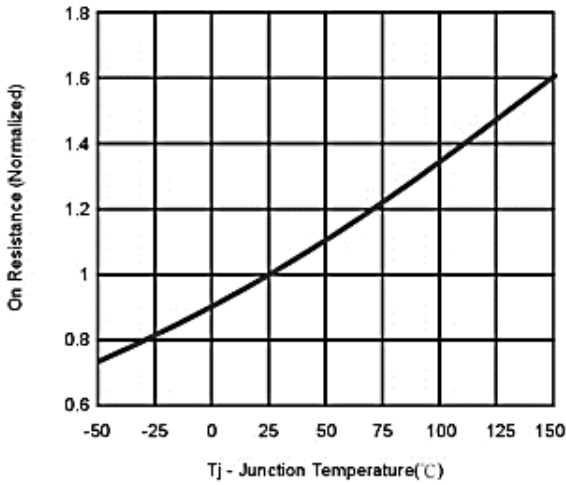
### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-40	-44	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.023	---	V/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-30A	---	15	18	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A	---	18	25	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.0	-1.6	-2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	4.74	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-12A	---	25	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	11	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	9.5	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, R <sub>L</sub> =15Ω I <sub>D</sub> =-1A, V <sub>GEN</sub> =-10V, R <sub>G</sub> =6Ω	---	48	---	ns
T <sub>r</sub>	Rise Time		---	24	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	88	---	
T <sub>f</sub>	Fall Time		---	9.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, f=1MHz	---	2760	---	pF
C <sub>oss</sub>	Output Capacitance		---	260	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	85	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-40	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	-90	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>s</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.3	V

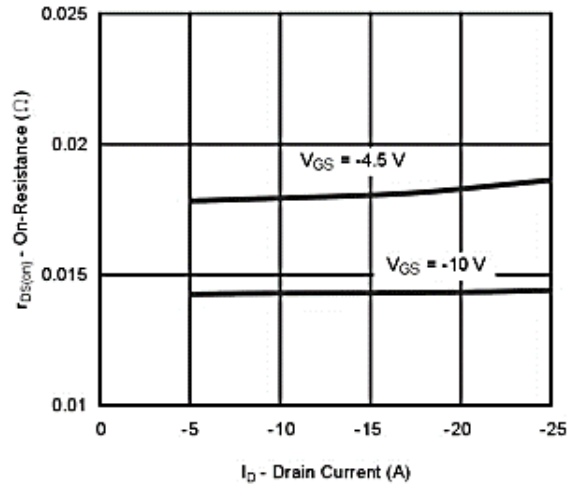
#### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-32V,V<sub>GS</sub>=-10V,L=0.1mH,I<sub>AS</sub>=-30A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

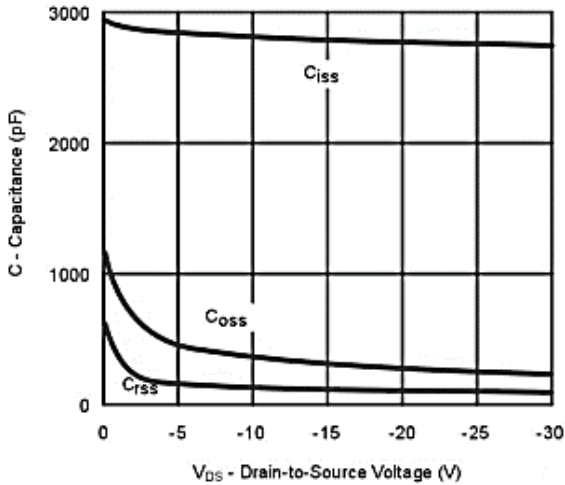
**Typical Characteristics**



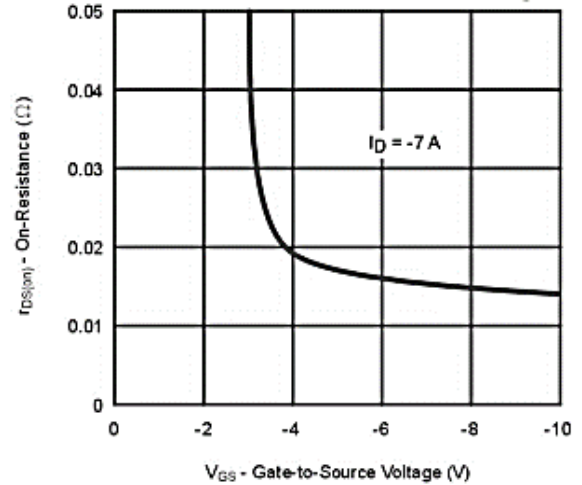
**Fig.1 On Resistance Vs Junction Temperature**



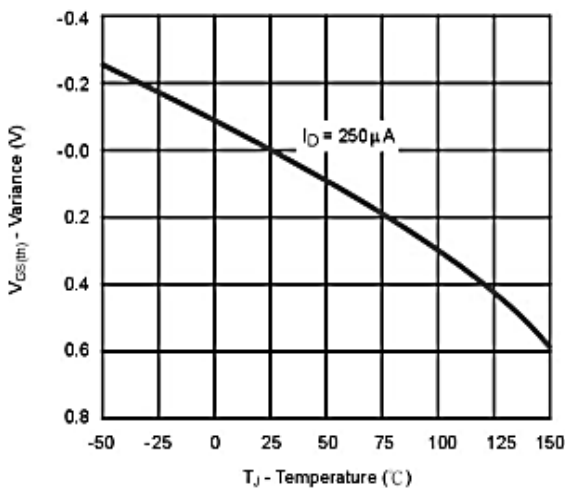
**Fig.2 On-Resistance Vs. Drain Current**



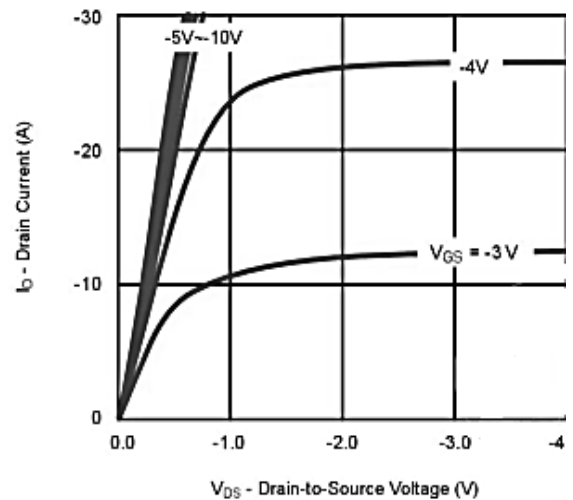
**Fig.3 Capacitance**



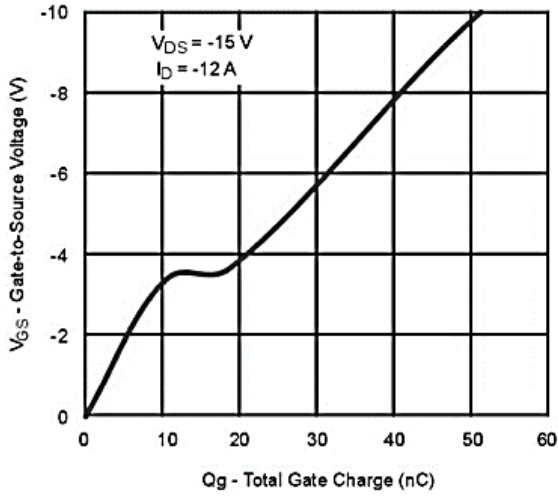
**Fig.4 On-Resistance Vs. Gate-to-Source Voltage**



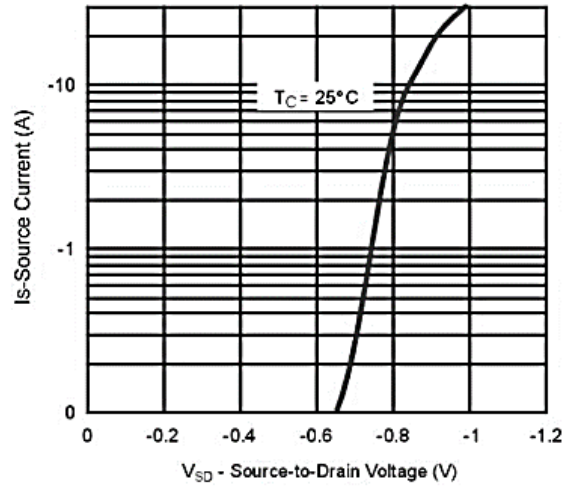
**Fig.5 Threshold Voltage**



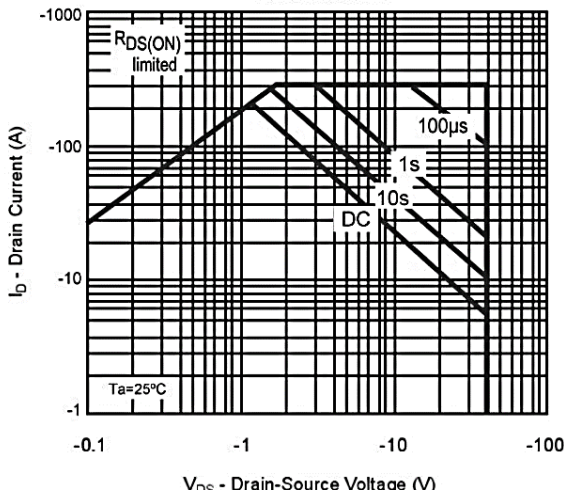
**Fig.6 On-Region Characteristics**



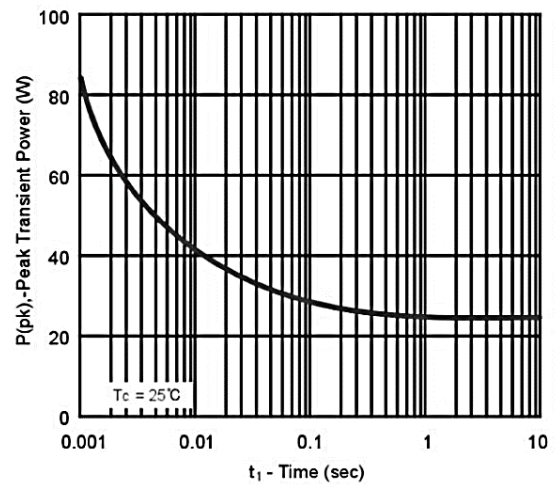
**Fig.7 Gate Charge**



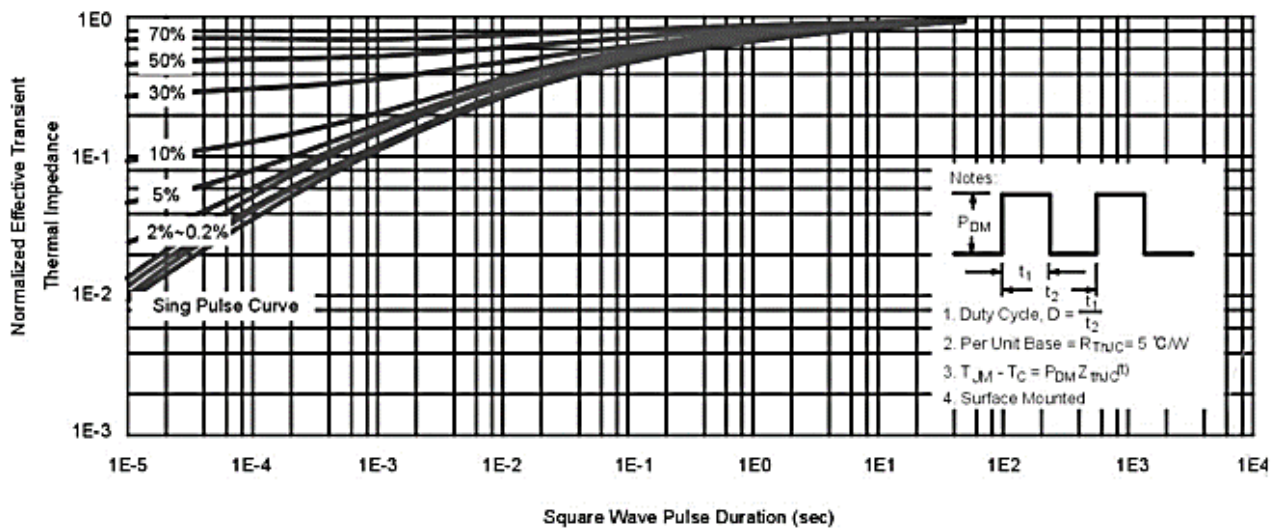
**Fig.8 Body-diode Characteristic**



**Fig.9 Safe Operating Area**



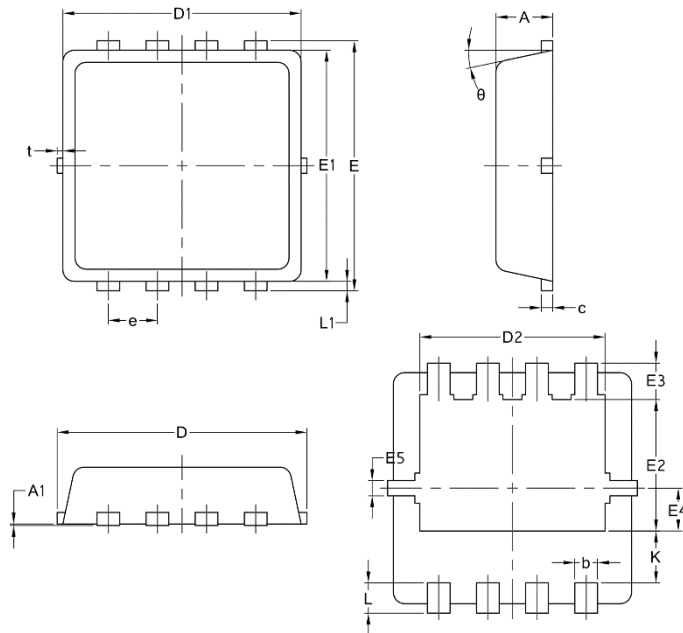
**Fig.10 Single Pulse Maximum Power Dissipation**



**Fig.11 Normalized Maximum Transient Thermal Impedance**



### Package Mechanical Data-DFN3\*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

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Edition	Date	Change
Rve1.0	2021/8/8	Initial release

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