2.4MHz 3A Step-Down Converter with I²C Interface

General Description

The RT5738 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I²C interface capable of operating up to 3.4MHz.

Using a proprietary architecture with synchronous rectification, the RT5738 is capable of delivering 3A continuous at over 80% efficiency, maintaining that efficiency at load currents as low as 10mA. The regulator operates at a nominal fixed frequency of 2.4MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power-Save Mode with a typical quiescent current of 40µA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 2.4MHz. In Shutdown Mode, the supply current is typically 0.1µA, excellent in reducing power consumption. PFM Mode can be disabled if fixed frequency is desired. The RT5738 is available in a small WL-CSP-15B 1.31x2.02 (BSC)

Features

- **0.3V to 1.85V Programmable Slew Rate for Voltage Transitions**
- **Steady 2.4MHz Switching Frequency**
- **Best-in-Class Load Transient**
- **Continuous Output Current Capability : 3A**
- **2.5V to 5.5V Input Voltage Range**
- **Digitally Programmable Output Voltage**
- **I²C-Compatible Interface Up to 3.4Mbps**
- **PFM Mode for High Efficiency in Light Load**
- **Quiescent Current in PFM Mode : 45µA (Typical)**
- **Input Under-Voltage Lockout (UVLO)**
- **Thermal Shutdown and Overload Protection**
- **15-Ball WL-CSP Package**

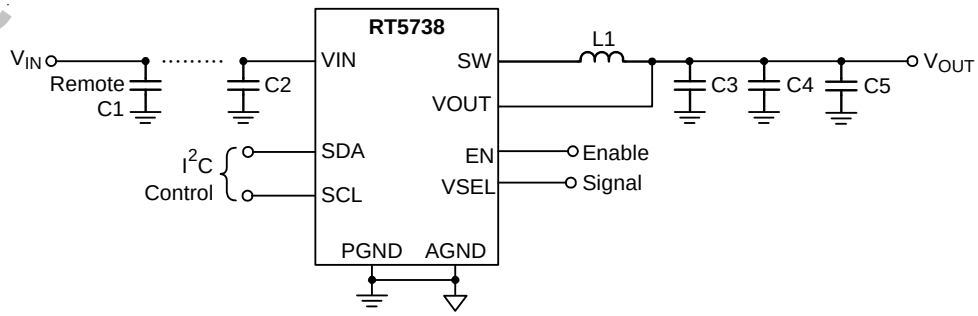
Applications

- Application, Graphic, and DSP Processors
  - ARM™, Tegra™, OMAP™, NovaThor™, ARMADA™, Krait™, etc.
- Hard Disk Drives, LPDDR3, LPDDR4
- Tablets, Netbooks, Ultra-Mobile PCs
- Smart Phones
- Gaming Devices

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Simplified Application Circuit



Ordering Information

RT5738 □□

Package Type
WSC : WL-CSP-15B 1.31x2.02 (BSC)

Power-Up Defaults (VSEL0/VSEL1)
A : 0.4V/0.6V
B : 1.125V/1.125V
C : 0.65V/0.7V

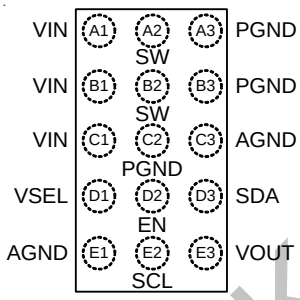
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)

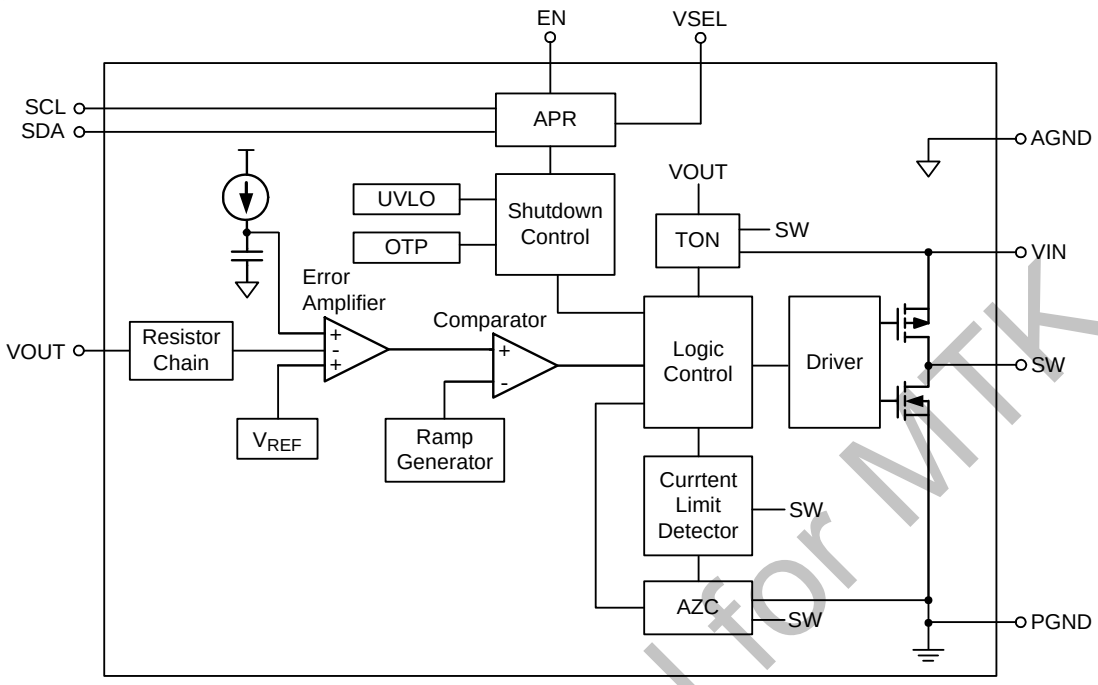


WL-CSP-15B 1.31x 2.02 (BSC)

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1, B1, C1	VIN	Power input voltage. Connect to the input power source. Connect to C_{IN} with minimal path.
A2, B2	SW	Switching node. Connect to the inductor.
A3, B3, C2	PGND	Power ground. The low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
C3, E1	AGND	Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
D1	VSEL	Voltage select. When this pin is LOW, VOUT is set by the VSEL0 register. When this pin is HIGH, VOUT is set by the VSEL1 register. Polarity of pin in conjunction with the MODE bits in the Control register 02h, will select Forced PWM or Auto PFM/PWM mode of operation. VSEL0 = Auto PFM, and VSEL1 = Forced PWM.
D2	EN	Enable. The device is in Shutdown Mode when this pin is LOW. Device keeps register content when EN pin is LOW.
D3	SDA	I^2C serial data.
E2	SCL	I^2C serial clock.
E3	VOUT	VOUT. Output voltage sense through this pin. Connect to output capacitor.

Functional Block Diagram



Operation

The RT5738 is a low voltage synchronous step-down converter that can support input voltage ranging from 2.5V to 5.5V and the output current can be up to 3A. The RT5738 uses ACOT™ mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

PWM Frequency and Adaptive on Time Control

The on-time can be roughly estimated by the equation :

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where f_{SW} is nominal 2.4MHz

Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low side MOSFET decrease to the zero current threshold. The low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can adjust for different condition to get better efficiency.

Under-voltage Protection (UVLO)

The UVLO continuously monitors the voltage of VIN to make sure the device works properly. When the VCC is high enough to reach the high threshold voltage of UVLO. The step down converter softly start or pre-bias to its regulated output voltage. When the VIN decreases to its low threshold (350mV hysteresis), the device will shut down.

Power GOOD

When the output voltage is higher than PGOOD rising threshold, the PGOOD flag is High.

Over-Current Protection (OCP)

The RT5738 senses the current signal when low side MOSFET turns on and uses a valley current limiting circuit. As a result, the OCP set point is the OCP DC

limit minus half of the ripple current. The OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit. If the OCP keeps and the load current is larger than the current provided by the converter over 16 consecutive times, the output voltage drops and the converter latches off before entering Hiccup mode. Latch off time is 1.7ms or 50ms by factory configuration.

Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft start time can be programming by I^2C.

Over-Temperature Protection (OTP)

The RT5738 has over temperature protection. When the device triggers the OTP, the device shuts down.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 7V
- Other I/O Pin Voltages ---------- –0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-15B 1.31x2.02 (BSC) ---------- 2W
- Package Thermal Resistance (Note 3)
  WL-CSP-15B 1.31x2.02 (BSC), θ_{JA} ---------- 49.8°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 4)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 5)

- Supply Input Voltage, V_{IN} ---------- 2.5V to 5.5V
- Output Current, I_{OUT} ---------- 0A to 3A
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = –40°C to 85°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating quiescent current PWM		I_{Q_PWM}	I_{LOAD} = 0, MODE Bit = 1 (Forced PWM)	--	15	--	mA
Operating quiescent current PFM		I_{Q_PFM}	I_{LOAD} = 0	--	45	--	μA
H/W Shutdown Supply Current		$I_{SHDN\_H/W}$	EN = GND	--	0.1	3	μA
S/W Shutdown Supply Current		$I_{SHDN\_S/W}$	EN = VIN, BUCK_ENx = 0, 2.5V ≤ VIN ≤ 5.5V	--	2	12	μA
Under-Voltage Lockout Threshold		V_{UVLO}	VIN Rising	--	2.32	2.45	V
Under-Voltage Lockout Hysteresis		ΔV_{UVLO}		--	350	--	mV
$R_{DS(ON)}$ of P-MOSFET		$R_{DS(ON)\_P}$	V_{IN} = 5V	--	30	--	mΩ
$R_{DS(ON)}$ of N-MOSFET		$R_{DS(ON)\_L}$	V_{IN} = 5V		17	--	mΩ
Input Voltage	Logic-High	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.1	--	--	V
	Logic-Low	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V	--		0.4	
Input Bias Current		I_{IN}	Input Tied to GND or VIN	--	0.01	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VOUT DC Accuracy		2.5 V ≤ V_{IN} ≤ 5.5 V, VOUT from Minimum to Maximum, V_{OUT} = 0.4V, Auto PFM/PWM (Note 5)	–3	--	3	%
		2.5V ≤ V_{IN} ≤ 5.5V, VOUT from Minimum to Maximum, V_{OUT} = 0.4V, Forced PWM (Note 5)	–1.5	--	1.5	%
Load Regulation	ΔV_{LOAD}	$I_{OUT(DC)}$ = 1 to 3A	--	0.1	--	%/A
Line Regulation	ΔV_{LINE}	2.5V ≤ VIN ≤ 5.5V, $I_{OUT(DC)}$ = 1.5A	--	0.2	--	%/V
Transient load Response	AC_{LOAD}	I_{LOAD} Step 0.01 A to 1.5 A, tr = tf = 500ns, V_{OUT} = 1.125 V (Note 5)	--	±45	--	mV
Line Transient	V_{LINE}	V_{IN} = 3V to 3.6V, tr = tf = 10μs, I_{OUT} = 100mA, Forced PWM mode (Note 5)	--	±40	--	mV
P-MOSFET Peak Current Limit	I_{LIM_P}		5	5.5	6	A
Valley Current Limit			3.5	4	4.5	A
Thermal Shutdown	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	30	--	°C
Input OVP Shutdown	V_{SDHD_OVPrth}	Rising Threshold	--	6.15	--	V
Input OVP Shutdown	V_{SDHD_OVPfth}	Falling Threshold	5.5	5.73	--	V
Switching Frequency	f_{SW}	V_{OUT} = 1.2V (Note 5)	2100	2400	2700	kHz
Minimum Off-Time			--	170	--	ns
Resolution			--	8	--	bits
Differential Nonlinearity			--	--	0.5	LSB

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

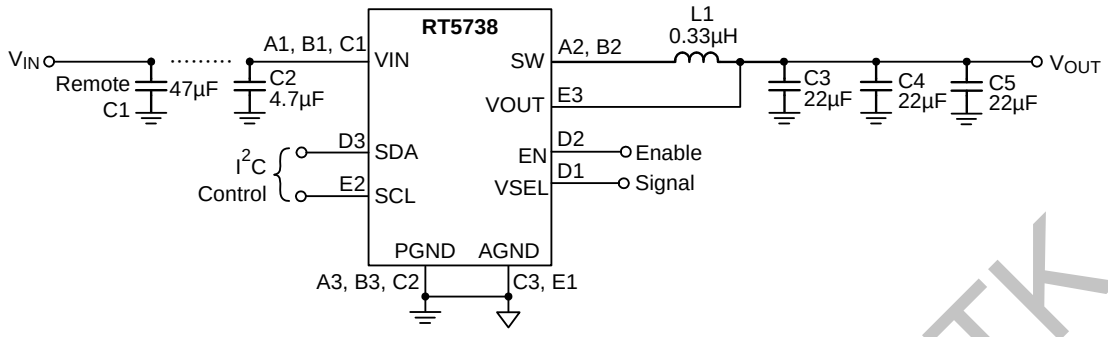
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Typical Application Circuit



Application Information

I²C Interface

The RT5738A I²C slave address = 7'b1010000 for 0.4V/0.6V setting

The RT5738B I²C slave address = 7'b1010111 for 1.125V/1.125V setting

The RT5738C I²C slave address = 7'b1010010 for 0.65V/0.7V setting

I²C Register Map

Address Name	Register Address		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
NSEL0	0x00	Meaning	VSEL0							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
NSEL1	0x01	Meaning	VSEL1							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CONTROL1	0x02	Meaning	DISCHG	UP_SR[2:0]			Reserved	SW_RESET	MODE_VSEL1	MODE_VSEL0
		Default	0	0	0	1	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
ID1	0x03	Meaning	VENDOR_ID			Reserved	DIE_ID			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
ID2	0x04	Meaning	Reserved				DIE_REV			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
MONITOR	0x05	Meaning	PGOOD	UVLO	OVP	POS	NEG	RESET_STAT	OT	BUCK_STATUS
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R
CONTROL2	0x06	Meaning	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_VSEL1	EN_VSEL0
		Default	0	0	1	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
CONTROL3	0x07	Meaning	Reserved		EN_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W
CONTROL4	0x08	Meaning	Reserved		DIS_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
NSEL0	0x00	Meaning	VSEL0							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VSEL0			VID Table satisfy : SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 11001000 : V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V 5mV step for 0.3 to 1.3, 10mV step for 1.3 to1.85							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
NSEL1	0x01	Meaning	VSEL1							
		Default	0	0	0	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VSEL1			VID Table satisfy : SEL[7:0] = 11111111 : V_{OUT} = 1.85V … SEL[7:0] = 1100100 0: V_{OUT} = 1.3V … SEL[7:0] = 0000000 : 0.3V 5mV step for 0.3 to 1.3, 10mV step for 1.3 to 1.85							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL1	0x02	Meaning	DISCHG	UP_SR[2:0]			Reserved	SW_ RESET	MODE_ VSEL1	MODE_ VSEL0
		Default	0	0	0	1	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DISCHG			0 : Discharge path disabled							
			1 : Discharge path enabled							
UP_SR[2:0]			DVS Speed for UP DVS 000 = 24mV step/μs 001 = 12mV step/μs 010 = 6mV step/μs 011 = 3mV step/μs 100 = 1.5mV step/μs 101 = 0.75mV step/μs 110 = 0.375mV step/μs 111 = 0.1875mV step/μs							
Reserved			Reserved							
SW_RESET			write 1 to reset, always read 0							
MODE_VSEL1			0 : Auto							
			1 : Continuous mode							
MODE_VSEL0			0 : Auto							
			1 : Continuous mode							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
ID1	0x03	Meaning	VENDOR_ID[2:0]			Reserved	DIE_ID[3:0]			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
VENDOR_ID[2:0]			Vendor_ID							
DIE_ID[3:0]			DIE_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
ID2	0x04	Meaning	Reserved				DIE_REV[3:0]			
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R	R	R	R	R	R
DIE_REV[3:0]			Revision_ID							

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
MONITOR	0x05	Meaning	PGOOD	UVLO	OVP	POS	NEG	RESET_ STAT	OT	BUCK_ STATUS
		Default	0	0	0	0	0	0	0	1
		Read/Write	R	R	R	R	R	R	R	R

PGOOD	1 : Buck is enabled and soft-start is completed.
UVLO	1 : Signifies the VIN is less than the UVLO threshold.
OVP	1 : Signifies the VIN is greater than the OVP threshold.
POS	1 : Signifies a positive voltage transition is in progress
NEG	1 : Signifies a negative voltage transition is in progress
RESET_STAT	1 : Indicates that a register reset was performed.
OT	1 : Signifies the thermal shutdown is active.
BUCK_STATUS	1 : Buck enabled; 0 : buck disabled.

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL2	0x06	Meaning	DN_SR[2:0]			Reserved	SS_SR[1:0]		EN_ VSEL1	EN_ VSEL0
		Default	0	1	1	0	0	0	0	0
		Read/Write	R/W	R/W	R/W	R	R/W	R/W	--	--

DN_SR[2:0]	DVS Speed for DN DVS 000 = 24mV step/μs 001 = 12mV step/μs 010 = 6mV step/μs 011 = 3mV step/μs 100 = 1.5mV step/μs 101 = 0.75mV step/μs 110 = 0.375mV step/μs 111 = 0.1875mV step/μs
SS_SR[1:0]	DVS Speed for SOFT START DVS 00=10mV step/μs 01=5mV step/μs 10=2.5mV step/μs 11=1.25mV step/μs
EN_VSEL1	0 : DISABLE 1 : ENABLE
EN_VSEL0	0 : DISABLE 1 : ENABLE

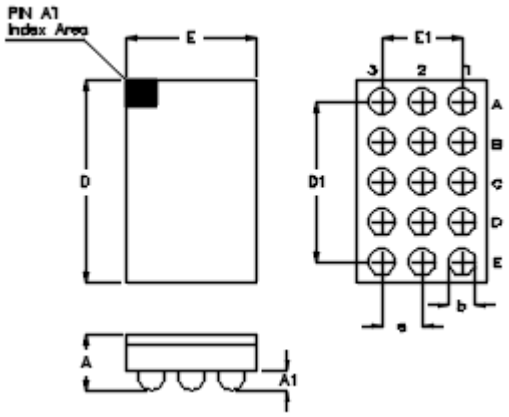
Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL3	0x07	Meaning	Reserved		EN_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Reserved	Reserved bits
EN_DLY[5:0]	Delay applied upon enabling (ms) 000000b = 0ms – 111111b = 63ms (steps of 1ms)

Register Name	Register Address		b[7] (MSB)	b[6]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0] (LSB)
CONTROL4	0x08	Meaning	Reserved		DIS_DLY[5:0]					
		Default	0	0	0	0	0	0	0	0
		Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Reserved	Reserved bits
DIS_DLY[5:0]	Delay applied upon disable (ms) 000000b = 0ms – 111111b = 63ms (steps of 1ms)

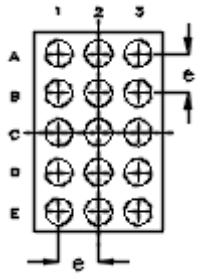
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.980	2.060	0.078	0.081
D1	1.600		0.063	
E	1.270	1.350	0.050	0.053
E1	0.800		0.031	
e	0.400		0.016	

15B WL-CSP 1.31x2.02 Package (BSC)

Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.31*2.02-15(BSC)	15	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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Datasheet Revision History

P00	2016/5/3			First Edition
P01	2016/6/8		I^2C Interface	Modify
P02	2016/8/4		Features Ordering Information Electrical Characteristics Note 2 I^2C Interface	Modify