Application Note: SY6355

Sink and Source DDR Termination Regulator

General Description

The SY6355 is a sink and source double data rate (DDR) regulator designed for use in low input voltage, low-cost, low-noise systems where space is a key consideration. It maintains a fast transient response and requires a minimum output capacitance of only 20μF and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT BUS termination. Additionally, it provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3(suspend to RAM) for DDR application

The SY6355 is available in the DFN3×3-10 thermal pad package, and it's rated both Green and Pb-free. It's specified from -40℃ to 85℃.

Ordering Information

SY6355□(□,□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6355DBC	DFN3×3-10	----

Features

- Input Voltage: Supports 2.5V Rail and 3.3V Rail
- VLDOIN Voltage Range: 1.1V to 3.5V
- Sink and Source Termination Regulator Includes Droop Compensation.
- Requires Minimum Output Capacitance of 20μF(Typically 3×10μF MLCCs) for Memory.
- PGOOD to Monitor Output Regulation
- Enable Function Option
- REFIN Input Allows for Flexible Input Tracking either Directly or Through Resistor Divider
- Remote Sensing(VOSNS)
- ±10mA Buffered Reference(REFOUT)
- Built-in Soft-start, UVLO, and OCL
- Thermal Shutdown Protection
- Supports DDR, DDR2, DDR3, DDR3L, Low Power DDR3, DDR4 VTT Applications
- Compacted Package: DFN3×3-10 with Thermal Pad

Application

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Base Stations

Typical Applications

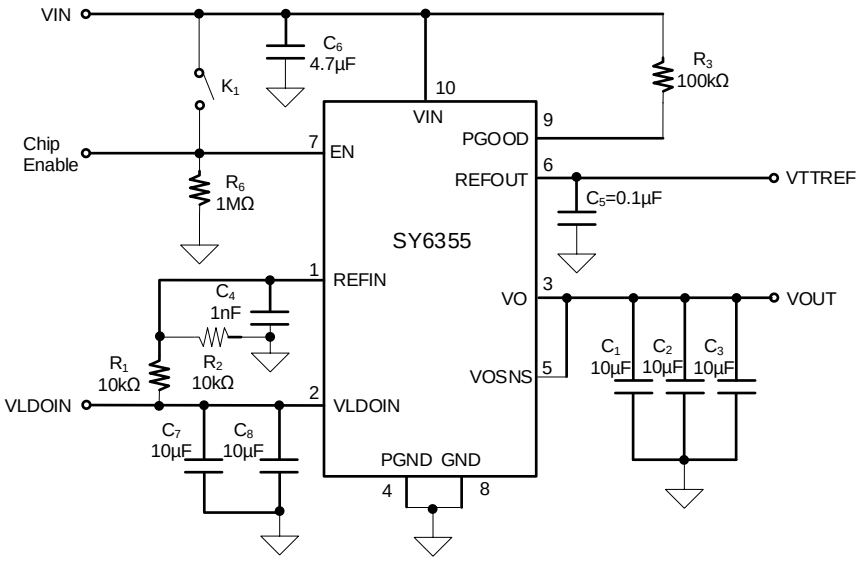

Figure 1. Schematic Diagram

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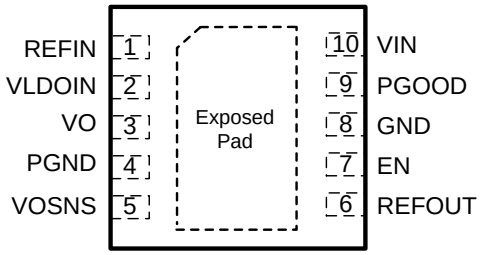
Pinout (Top View)



(DFN3×3-10)

Top Mark: **B9*xyz*** for SY6355DBC **(**Device code: B9; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Name	Pin Description
REFIN	1	Reference Input. Connect to GND through a 0.1μF ceramic capacitor.
VLDOIN	2	Supply voltage for the LDO. Use a 10μF (or greater) ceramic capacitor to supply this transient charge.
VO	3	Power output pin for the LDO. For stable operation, the total capacitance of the VO output pin must be greater than 20μF. Attach three, 10μF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL).
PGND	4	Power ground pin for the LDO.
VOSNS	5	Voltage sense input for the LDO. Connect to positive terminal of the output capacitor or load.
REFOUT	6	Reference output. Connect to GND Through a 0.1uF ceramic capacitor.
EN	7	Enable input. Driving this pin high turns on the regulator. Driving this pin low shuts off the regulator. For DDR VTT application, connect EN to SLP_S3. Do not leave it floating.
GND	8	Signal ground pin
PGOOD	9	Open drain power-good indicator, it's pulled high when VO output is within ±20% of REFOUT.
VIN	10	Input supply pin. A large bulk capacitance should be placed close to this pin to ensure that the input supply does not sag below the minimum VIN. A ceramic decoupling capacitor with a value between 1uF and 4.7uF is required.
Exposed Pad	/	The exposed pad should be connected to ground plane for the better thermal performance.

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Block Diagram

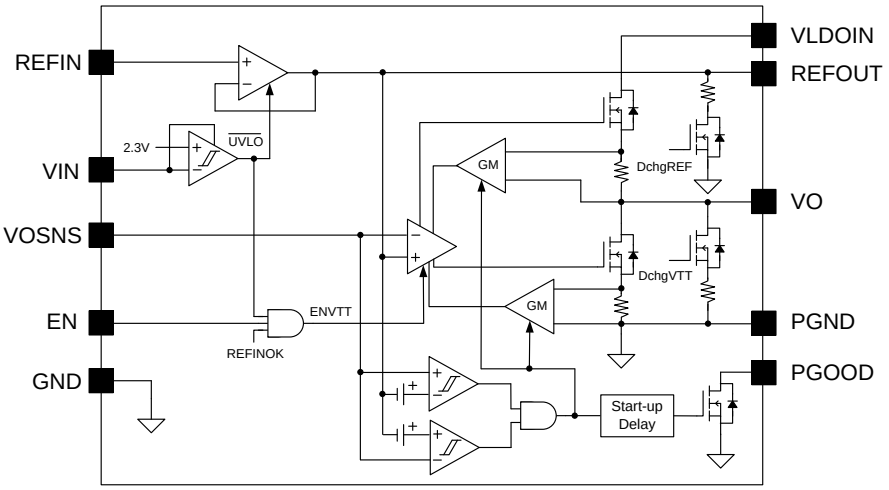

Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

REFIN, REFOUT, VIN, VO, VLDOIN, VOSNS ---------- -0.3 to 3.6V
EN, PGOOD ---------- -0.3 to 6.5V
PGND ---------- -0.3 to 0.3V
Power Dissipation, P_D @ T_A = 25℃ ---------- 1.8W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 54.7℃/W
θ_{JC} ---------- 45.5℃/W
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

VIN ---------- 2.375 to 3.5V
EN, VLDOIN, VOSNS ---------- -0.1 to 3.5V
REFIN ---------- 0.5 to 1.8V
PGOOD, VO ---------- -0.1 to 3.5V
REFOUT ---------- -0.1 to 1.8V
PGND ---------- -0.1 to 0.1V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

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Electrical Characteristics

(V_{VIN}=3.3V, V_{VLDOIN}=1.8V, V_{REFIN}=0.9V, V_{VOSNS}=0.9V, V_{EN}=V_{VIN}, C_{OUT}=3×10μF, T_J=-40℃ to 125℃, typical values are T_J=25℃, unless otherwise specified. The values are guaranteed by test, design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{IN}	V_{EN} = 3.3V, No Load		0.7	1	mA
Shutdown Current	$I_{IN(SDN)}$	V_{EN} = 0V, V_{REFIN} = 0V, No Load		65	80	μA
		V_{EN} = 0V, V_{REFIN} > 0.4V, No Load		200	400	
Supply Current of VLDOIN	I_{LDOIN}	V_{EN} = 3.3V, No Load		1	50	μA
Shutdown Current of VLDOIN	$I_{LDOIN(SDN)}$	V_{EN} = 0V, No Load		0.1	50	μA
Input Current of REFIN	I_{REFIN}	V_{EN} = 3.3V			1	μA
Output DC Voltage of VO	V_{VOSNS}	V_{REFOUT} = 1.25V(DDR1), I_O = 0A		1.25		V
			-15		15	mV
		V_{REFOUT} = 0.9V(DDR2), I_O = 0A		0.9		V
			-15		15	mV
		V_{REFOUT} = 0.75V(DDR3), I_O = 0A		0.75		V
			-15		15	mV
		V_{REFOUT} = 0.675V(DDR3L), I_O = 0A		0.675		V
			-15		15	mV
		V_{REFOUT} = 0.6V(DDR4), I_O = 0A		0.6		V
			-15		15	mV
Output Voltage Tolerance to REFOUT	V_{VOTOL}	-2 A< I_{VO} < 2 A	-25		25	mV
VO Source Current Limit	I_{VOSRCL}	V_{OSNS} = 0.9 ×V_{REFOUT}	3		4.5	A
VO Sink Current Limit	I_{VOSNCL}	V_{OSNS} = 1.1 ×V_{REFOUT}	3.5		5.5	A
OUT Shutdown Discharge Resistance	R_{DSCHRG}	V_{REFIN} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V		18	25	Ω
VO PGOOD Threshold	$V_{TH(PG)}$	PGOOD window lower threshold with respect to REFOUT	-23.5%	-20%	-17.5%	
		PGOOD window upper threshold with respect to REFOUT	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
PGOOD Start-up Delay	$T_{PGSTUPDLY}$	Start-up rising edge, VOSNS within 15% of REFOUT		2		ms
PGOOD Output Low Voltage	$V_{PGOODLOW}$	I_{SINK} = 4 mA			0.4	V
PGOOD Bad Delay	$T_{PBADDLY}$	VOSNS is outside of the ±20% PGOOD window		10		μs
Leakage Current	$I_{PGOODLK}$	V_{OSNS} = V_{REFIN}(PGOOD high impedance), V_{PGOOD} =V_{VIN} + 0.2V			1	μA
REFIN Voltage Range	V_{REFIN}		0.5		1.8	V
REFIN Under Voltage Lockout	$V_{REFINUVLO}$	REFIN rising	360	390	420	mV
REFIN Under Voltage Lock Out Hysteresis	$V_{REFIN-UVHYS}$			20		mV
REFOUT Voltage	V_{REFOUT}			REFIN		V

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REFOUT Voltage Tolerance to V_{REFIN}	$V_{REFOUTTOL}$	-1 mA< I_{REFOUT} < 1 mA, V_{REFIN} = 1.25 V	-12		12	mV
		-1 mA< I_{REFOUT} < 1 mA, V_{REFIN} = 0.9 V	-12		12	
		-1 mA< I_{REFOUT} < 1 mA, V_{REFIN} = 0.75 V	-12		12	
		-1 mA< I_{REFOUT} < 1 mA, V_{REFIN} = 0.675 V	-12		12	
		-1 mA< I_{REFOUT} < 1 mA, V_{REFIN} = 0.6 V	-12		12	
REFOUT Source Current Limit	$V_{REFOUT-SRCL}$	V_{REFOUT} = 0 V	10	40		mA
REFOUT Sink Current Limit	$I_{REFOUT-SNCL}$	V_{REFOUT} = 0 V	10	40		mA
UVLO Threshold	$V_{VINUVVIN}$	Wake up	2.2	2.3	2.375	V
		Hysteresis		50		mV
High-level Input Voltage	V_{ENIH}	Enable	1.2			V
Low-level Input Voltage	V_{ENIL}	Enable			0.3	
Hysteresis Voltage	V_{ENYST}	Enable		0.1		
Logic Input Leakage Current	I_{ENLEAK}	Enable	-1		1	μA
Thermal Shutdown Threshold	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25 ℃ on a Silergy EVB test board.

Note 3: The device is not guaranteed to function outside its operating conditions.

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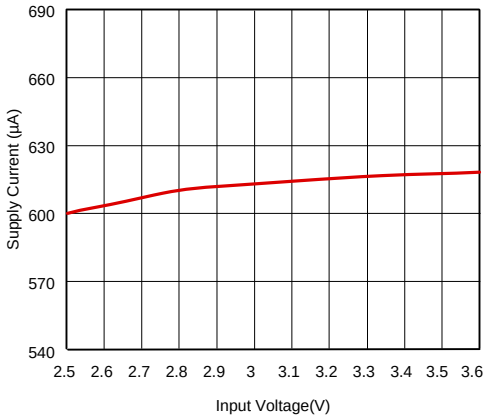
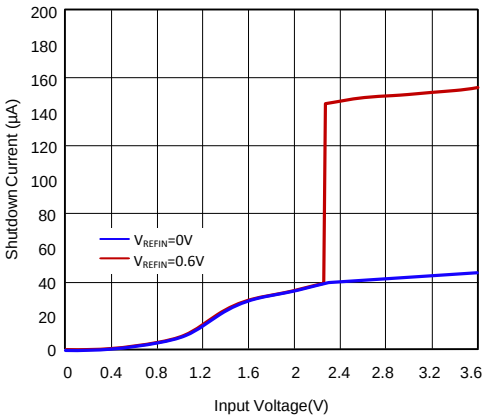
Typical Operating Characteristics

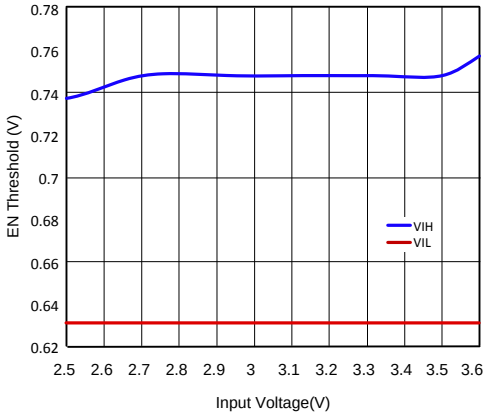
Supply Current vs. Input Voltage
(V_{LDOIN}=1.2V, V_{REFIN}=0.6V, EN ON, Null load)



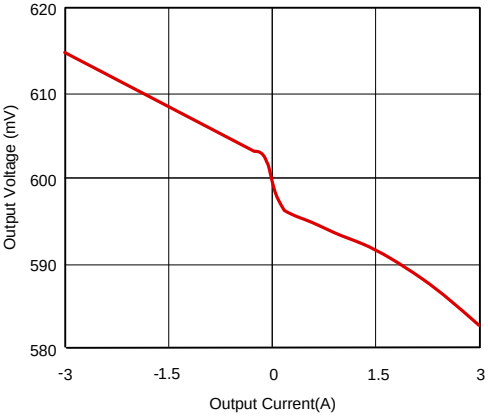
Shutdown Current vs. Input Voltage
(V_{EN}=0V, Null load)



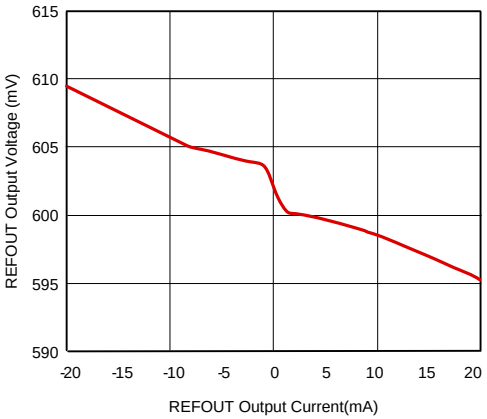
EN Threshold vs. Input Voltage
(V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Null load)



OUT Load Regulation
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V)



REFOUT Load Regulation
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V)



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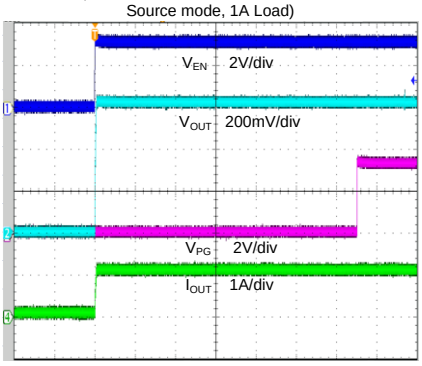
Startup From Enable

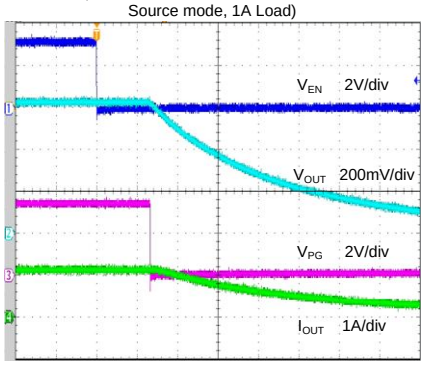
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Source mode, 1A Load)



Time(400μs/div)

Shutdown From Enable

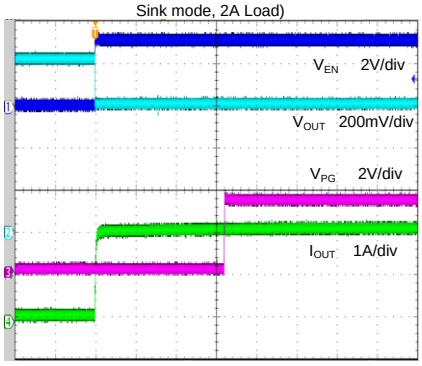
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Source mode, 1A Load)



Time(4μs/div)

Startup From Enable

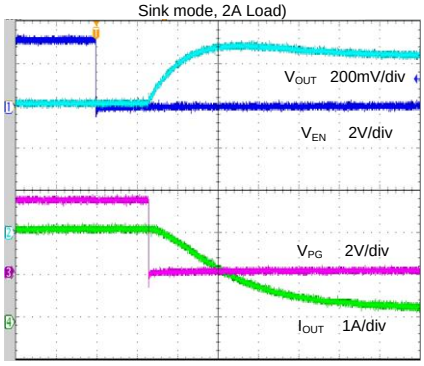
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Sink mode, 2A Load)



Time(800μs/div)

Shutdown From Enable

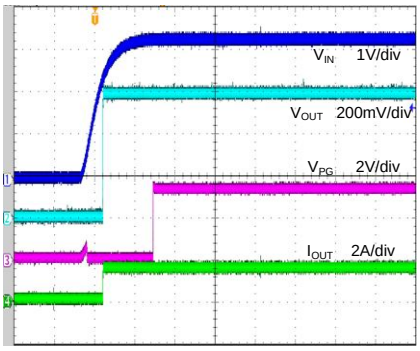
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, Sink mode, 2A Load)



Time(4μs/div)

Startup From VIN

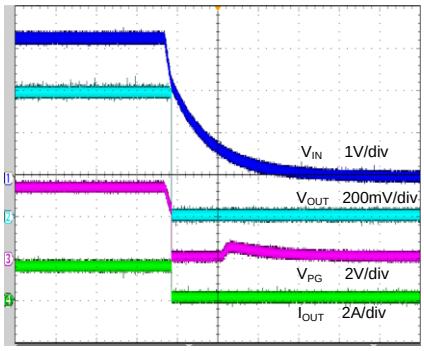
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, 2A Load)



Time(2ms/div)

Shutdown From VIN

(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, 2A Load)



Time(4μs/div)

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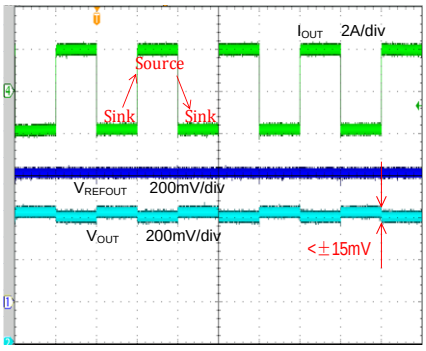
Load Transient

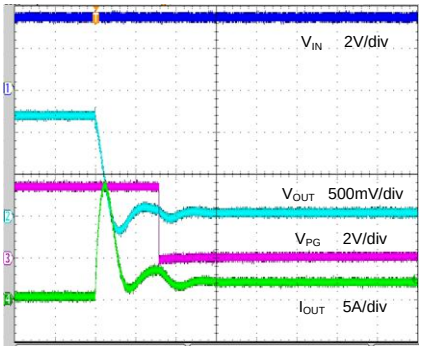
(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V, ±2A Load transient)



Time(10ms/div)

Short Circuit Response

(V_{IN}=3.3V, V_{LDOIN}=1.2V, V_{REFIN}=0.6V)



Time(10μs/div)

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Operation

The SY6355DBC is a sink and source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The device integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, connect a remote sensing terminal, VOSNS, to the positive terminal of each output capacitor as a separate trace from the high current path from VO.

Reference Output Function

When it is configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 10mA. REFOUT becomes active when REFIN voltage rises to 0.390 V and V_{IN} is above the UVLO threshold. When REFOUT is less than 0.375 V, it is disabled and subsequently discharges to GND through an internal 10-kΩ MOSFET. REFOUT is independent of the EN pin state.

En Control Function

When EN is driven high, the VO regulator begins normal operation. When the device drives EN low, VO discharges to GND through an internal 18-Ω MOSFET. REFOUT remains on when the device drives EN low. Ensure that the EN pin voltage remains lower than or equal to VVIN at all times.

Power Good Function

The SY6355DBC device provides an open-drain PGOOD output that goes high when the VO output is within ±20% of REFOUT. PGOOD de-asserts within 10 µs after the output exceeds the size of the power good window. During initial VO start-up, PGOOD asserts high 2 ms (typ) after the VO enters power good window. Because PGOOD is an open-drain output, a pull-up resistor with a value between 1 kΩ and 100 kΩ, placed between PGOOD and a stable active supply voltage rail is required.

Current Limit Protection

The LDO has a constant over current limit (OCL). The OCL level reduces by one-half when the output voltage is not within the power good window. This reduction is a non-latch protection.

UVLO Protection

For VIN under voltage lockout (UVLO) protection, the SY6355DBC monitors VIN voltage. When the VIN voltage is lower than the UVLO threshold voltage, both the VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

Thermal Shutdown Protection

The SY6355DBC monitors junction temperature. If the device junction temperature exceeds the threshold value, (typically 150℃), the VO and REFOUT regulators both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

Supply Filter Capacitor

Add a ceramic capacitor, with a value between 1µF and 4.7µF, placed close to the VIN pin, to stabilize the bias supply (2.5-V rail or 3.3-V rail) from any parasitic impedance from the supply.

VLDOIN Input Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10µF (or greater) ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at the VO pin. In general, use one-half of the COUT value for input.

Output Filter Capacitor

For stable operation, the total capacitance of the VO output pin must be greater than 20 µF. Attach three, 10-µF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2 mΩ, insert an RC filter between the output and the VOSNS input to achieve loop stability. The RC filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

PCB Layout Guide

For best performance of the SY6355DBC, the following guidelines must be strictly followed:

1. Place the input capacitors as close to VDLOIN pin as possible with short and wide connection
2. Place the output capacitor as close to VO pin as possible with short and wide connection. Place a ceramic capacitor with a value of at least 10-µF as close to VO pin if the rest of output capacitors need to be placed on the load side.

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3. Connect the VOSNS pin to the positive node of output capacitors as a separate trace. In DDR VTT application, connect the VO sense trace to DIMM side to ensure the VTT voltage at DIMM side is well regulated.
4. Consider adding low-pass filter at VOSNS if the VO sense trace is very long.
5. Connect the GND pin and PGND pin to the thermal pad directly.
6. SY6355DBC uses its thermal pad to dissipate heat. In order to effectively remove heat from SY6355DBC package, place numerous ground vias on the thermal pad. Use large ground copper plane, especially the copper plane on surface layer, to pour over those vias on thermal pad.

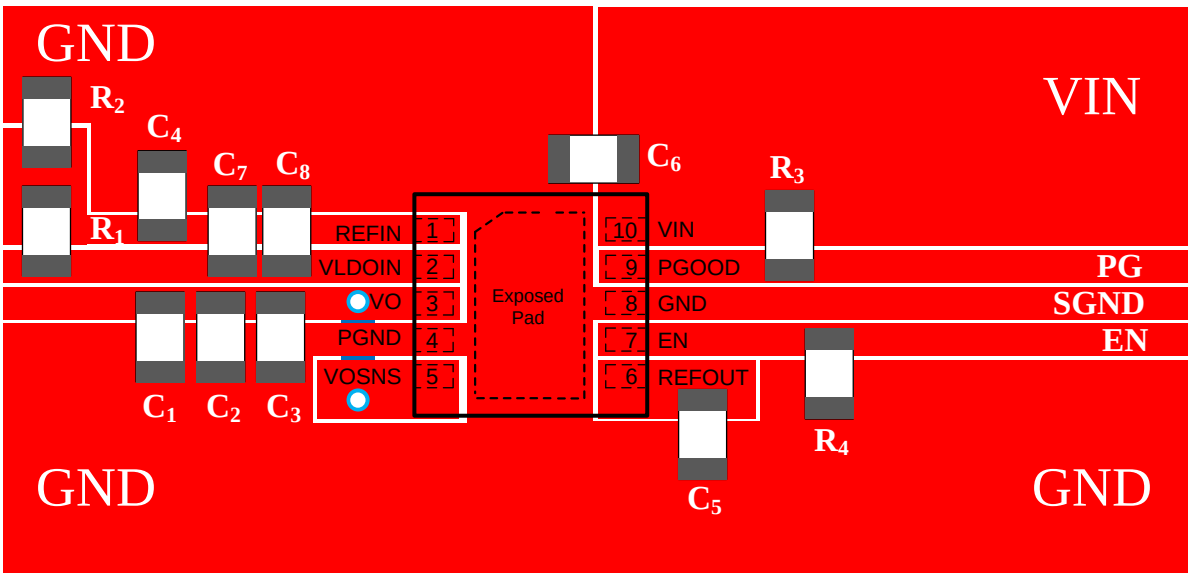

Figure 3. SY6355DBC PCB Layout Suggestion

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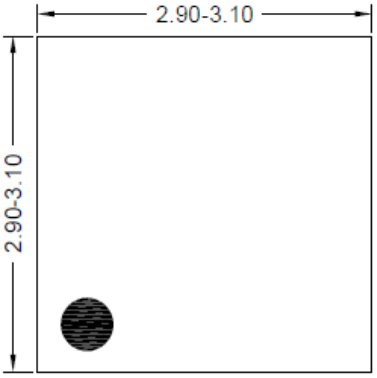
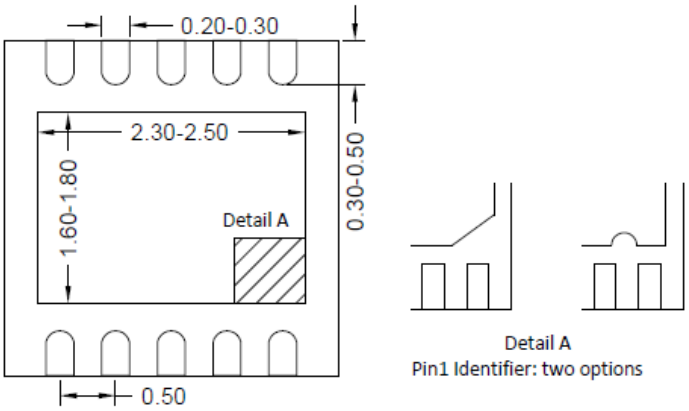
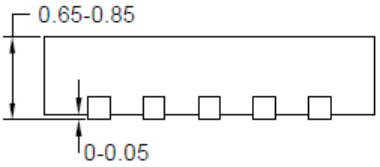
DFN3×3-10 Package Outline



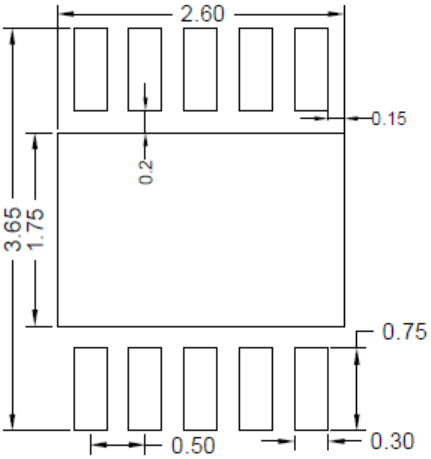
Top View



Bottom View



Side View



PCB layout (recommended)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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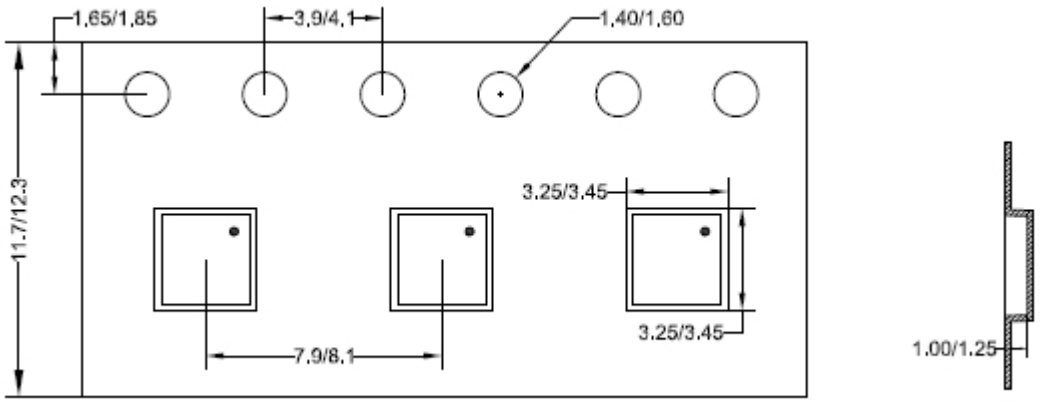
Taping & Reel Specification

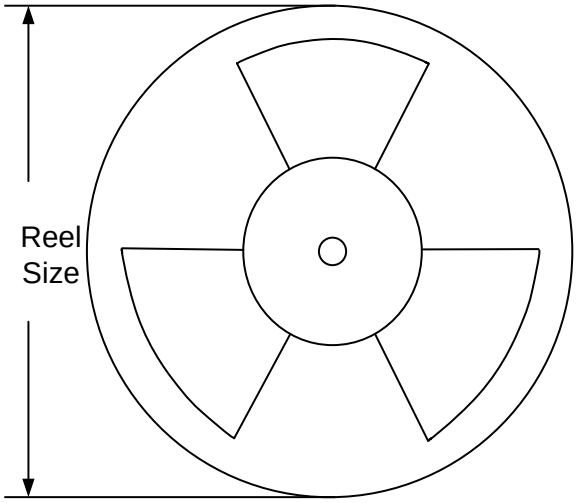
1. Taping orientation

DFN3×3-10



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	12	8	13"	400	400	5000

3. Others: NA

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