

N-channel Enhancement Mode Mosfet

3426B

DESCRIPTION

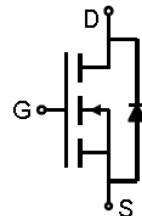
The 3426 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications.

GENERAL FEATURES

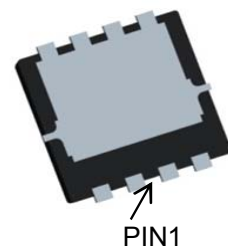
- $R_{DS(ON)} < 13m\Omega$ @ $V_{GS}=4.5V$
 $R_{DS(ON)} < 10m\Omega$ @ $V_{GS}=10V$
- High Power and current handling capability
- Lead free product is acquired
- Surface Mount Package

Application

- PWM applications
- Load switch
- Power management



Schematic diagram



DFN3*3

■ Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^{\circ}C$	I_D	30	A
	$T_C=100^{\circ}C$		21	
Pulsed Drain Current ^A		I_{DM}	100	A
Total Power Dissipation	$T_C=25^{\circ}C$	P_D	25	W
	$T_C=100^{\circ}C$		10	W
Single Pulse Avalanche Energy ^B		E_{AS}	128	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	7.5	$^{\circ}C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+175	$^{\circ}C$



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ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA		30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	T _J =25℃			1	μA
			T _J =55℃			5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V				±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA		1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =15A			8.0	10	mΩ
		V _{GS} = 4.5V, I _D =15A			10	13	
Diode Forward Voltage	V _{SD}	I _S =15A, V _{GS} =0V			0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S					30	A
Dynamic Parameters							
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ			1020		pF
Output Capacitance	C _{oss}				225		
Reverse Transfer Capacitance	C _{rss}				126		
Switching Parameters							
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =30A			28		nC
Gate-Source Charge	Q _{gs}				7		
Gate-Drain Charge	Q _{gd}				5		
Reverse Recovery Chrage	Q _{rr}	I _F =15A, di/dt=100A/us			25		ns
Reverse Recovery Time	t _{rr}				26		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _L =1Ω R _{GEN} =3Ω			8		
Turn-on Rise Time	t _r				15		
Turn-off Delay Time	t _{D(off)}				27		
Turn-off fall Time	t _f				7		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T_J=25°C, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25 Ω

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

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■ Typical Performance Characteristics

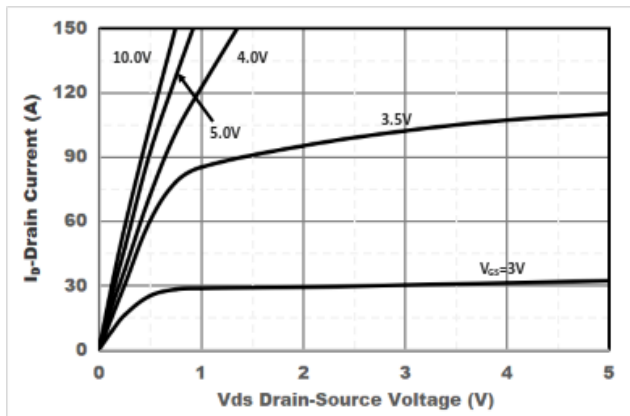


Figure1. Output Characteristics

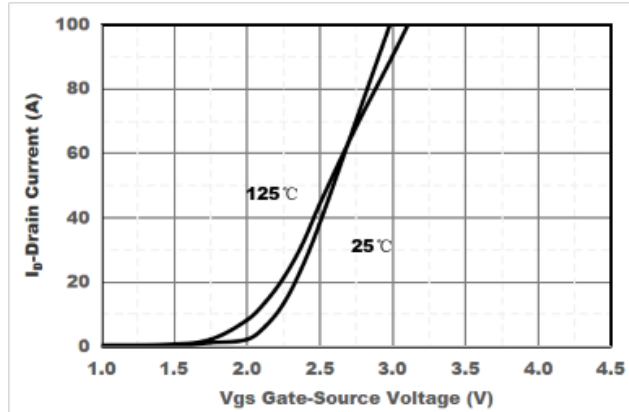


Figure2. Transfer Characteristics

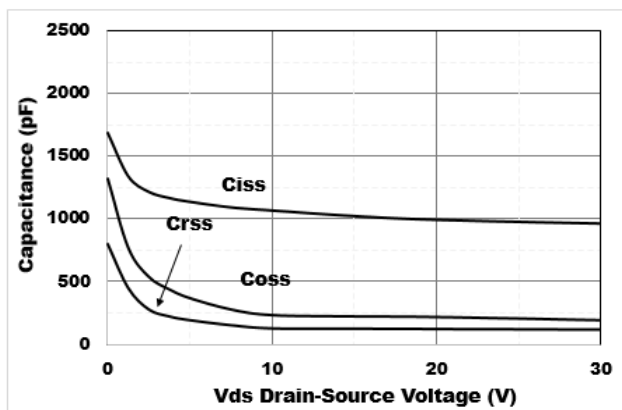


Figure3. Capacitance Characteristics

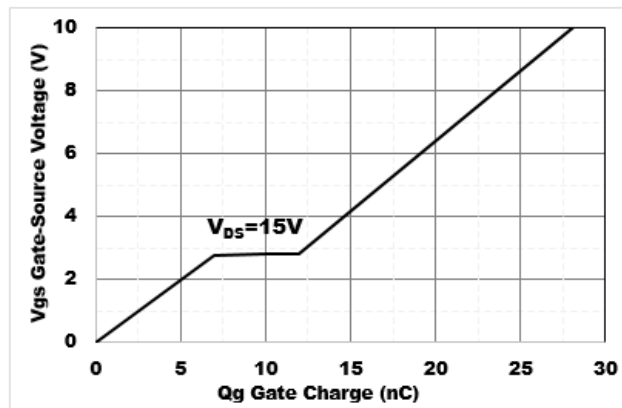


Figure4. Gate Charge

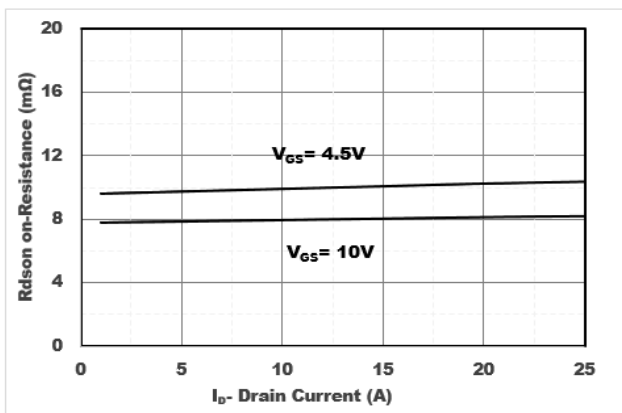


Figure5. Drain-Source on Resistance

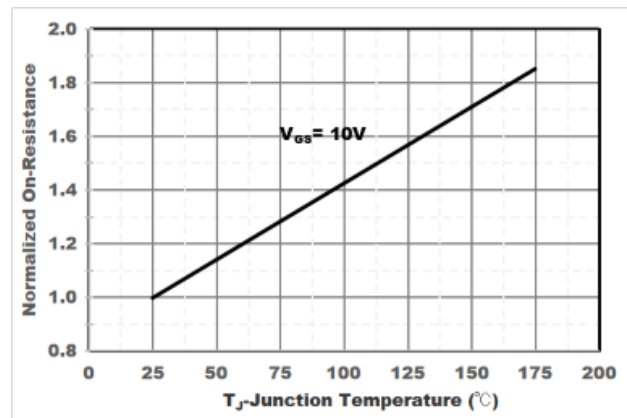


Figure6. Drain-Source on Resistance

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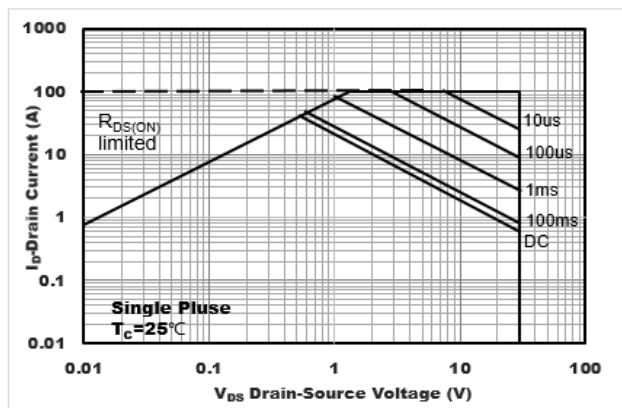


Figure7. Safe Operation Area

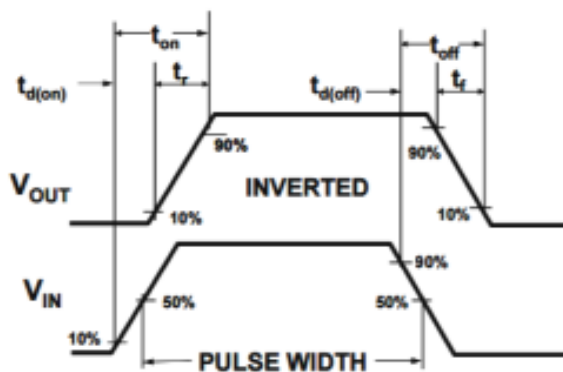
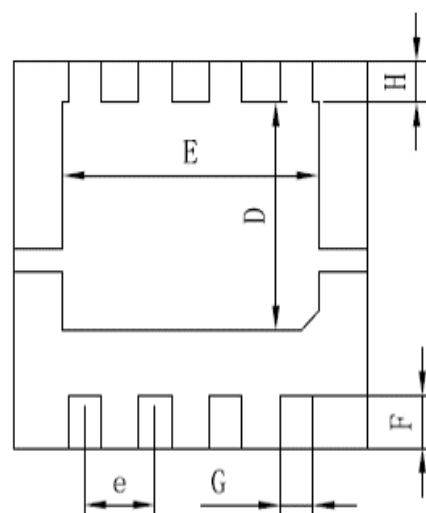
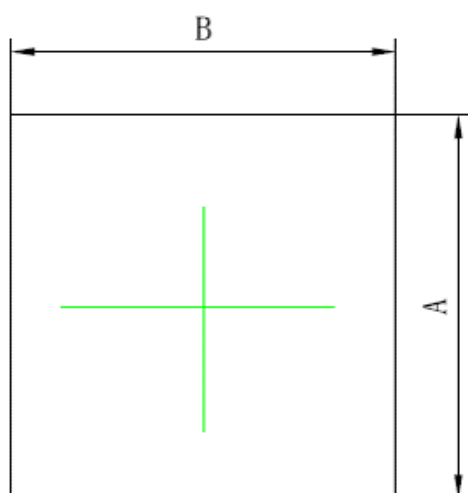


Figure8. Switching wave



Package Information

■ DFN3.3X3.3 Package information



A	B	C	C1
3.25±0.05	3.25±0.05	0.8±0.05	0.2±0.02
C2	D	E	F
0.05Max	1.9±0.1	2.35±0.15	0.45±0.05
G	H	e	
0.3±0.05	0.35±0.05	0.65±0.05	
单位: mm			

