

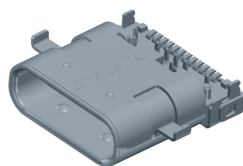
Operation:D+S1.25mm 沉板式 & 3.1Type-C 连接器(24PIN)



LTEM NO.:MC-313C-125 (Consumer Electronics)

(L10.0×W10.0×H 3.15 & DUL SMT LOW PCB TYPE)

3.1 Type-C CONNECTORS



Technical parameter

外焊沉板 DIP+SMT

PROJECT		LEVEL		A[better product]		B[average product]	
Electrical Properties	Contact Rating	5A, 24V DC					
	Initial Contact Resistance	30mΩ max.		50mΩ max.			
	Insulation Resistance	100MΩ min.500V DC		Skey/PD:		100MΩ min.300V DC	
	Withstand Voltage	500V AC for 1 minute		350 V AC for 1 minut			
Durable Performance	There No Load	6,500 Cycles		5,500 Cycles			
	Rated Load	5,500 Cycles		4,500 Cycles			
Storage temp.		-35℃~+75℃(Operating Temp:)					

側向導入 LATERAL

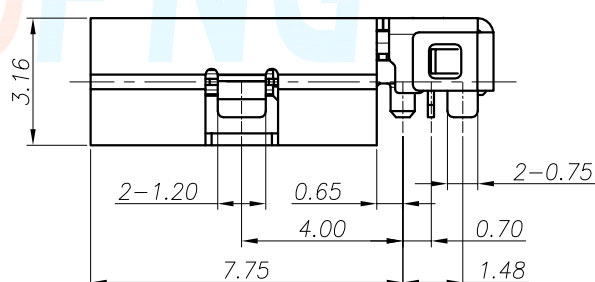
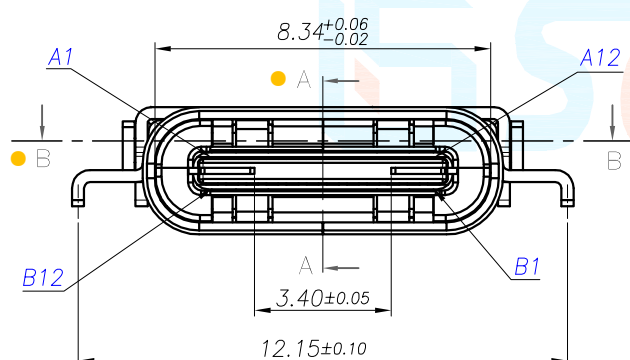
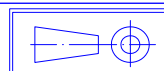
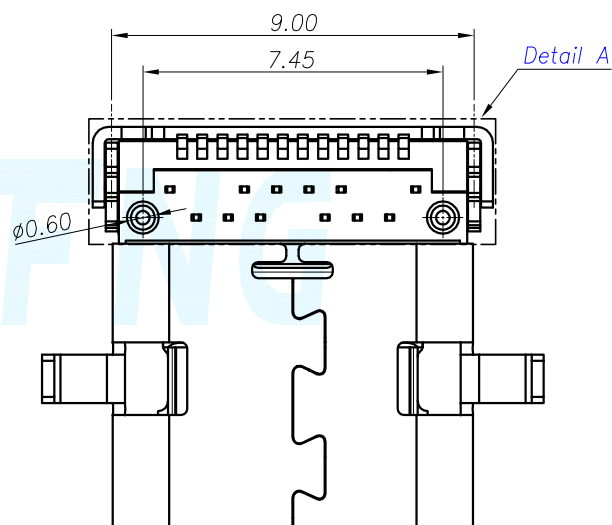
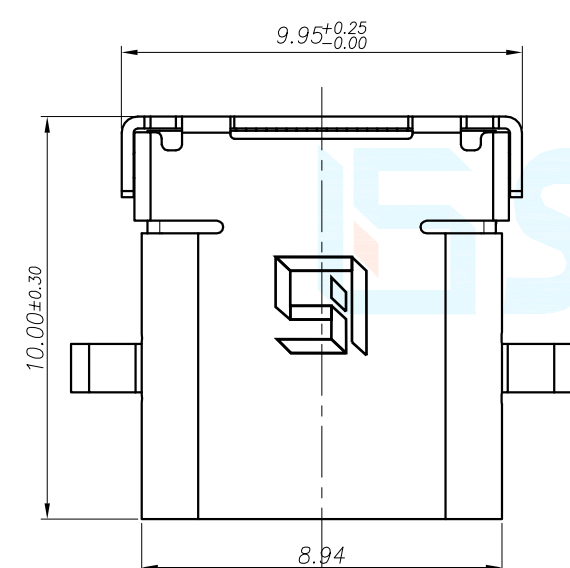
精密部品 NICETY

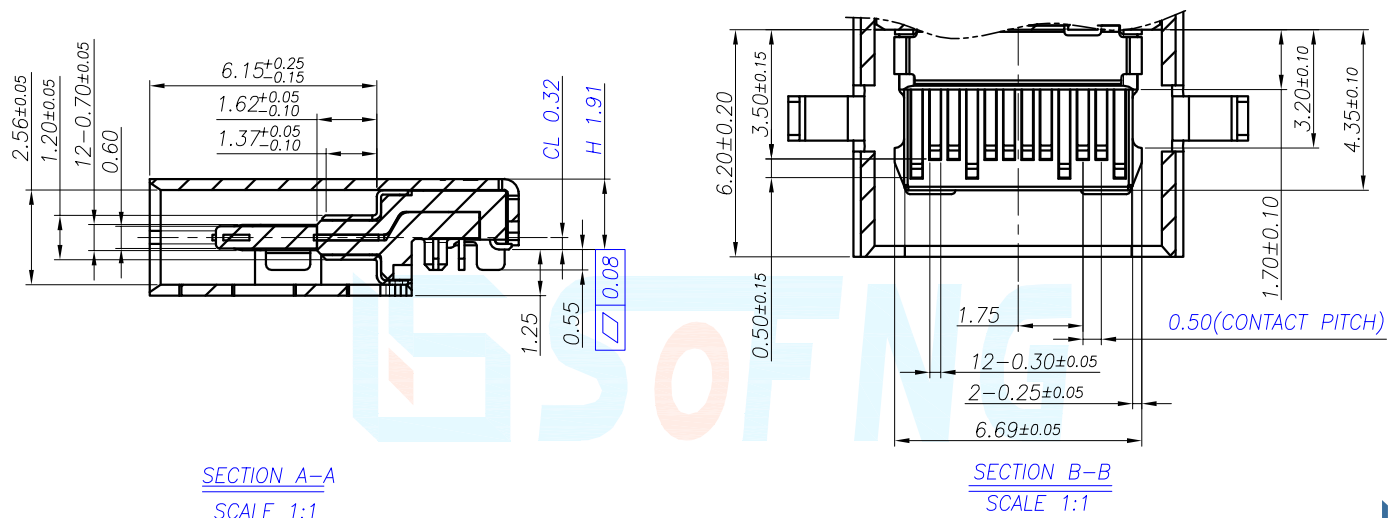
可靠 STABILIZE

環保材質 RoHS

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Unit:mm





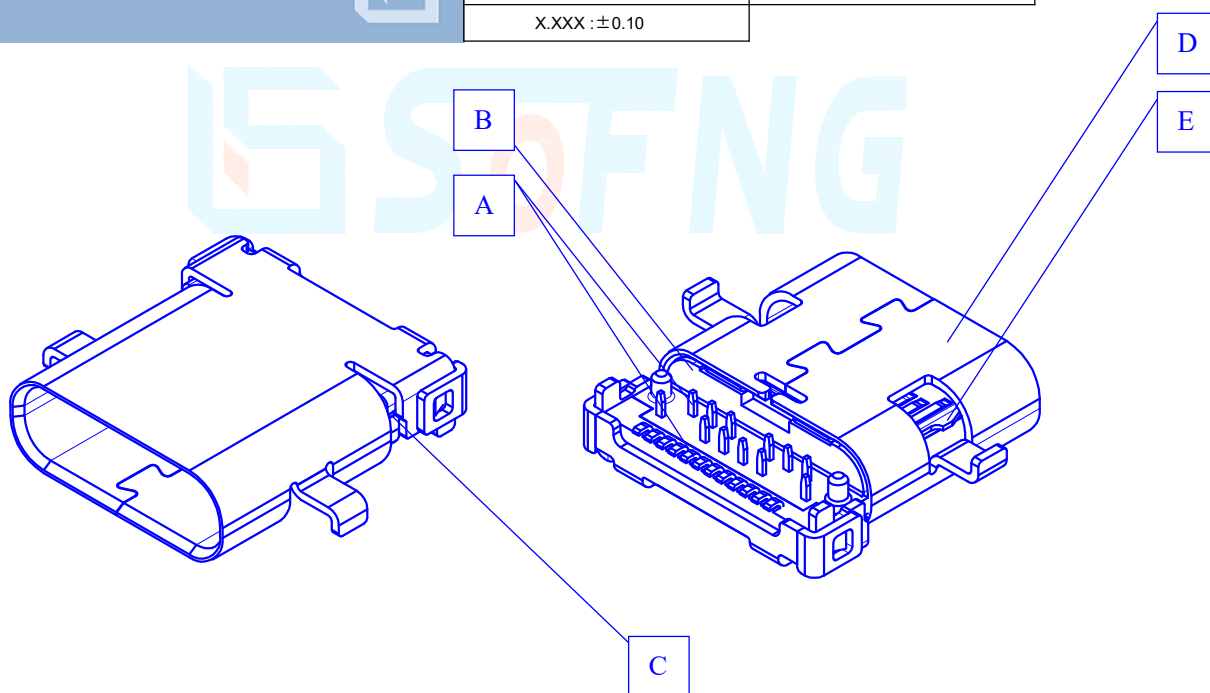
SPECIFIED TOLERANCES

UNLESS OTHERWISE

DECIMALS

X.X : ± 0.25 X.XX : ± 0.15 X.XXX : ± 0.10

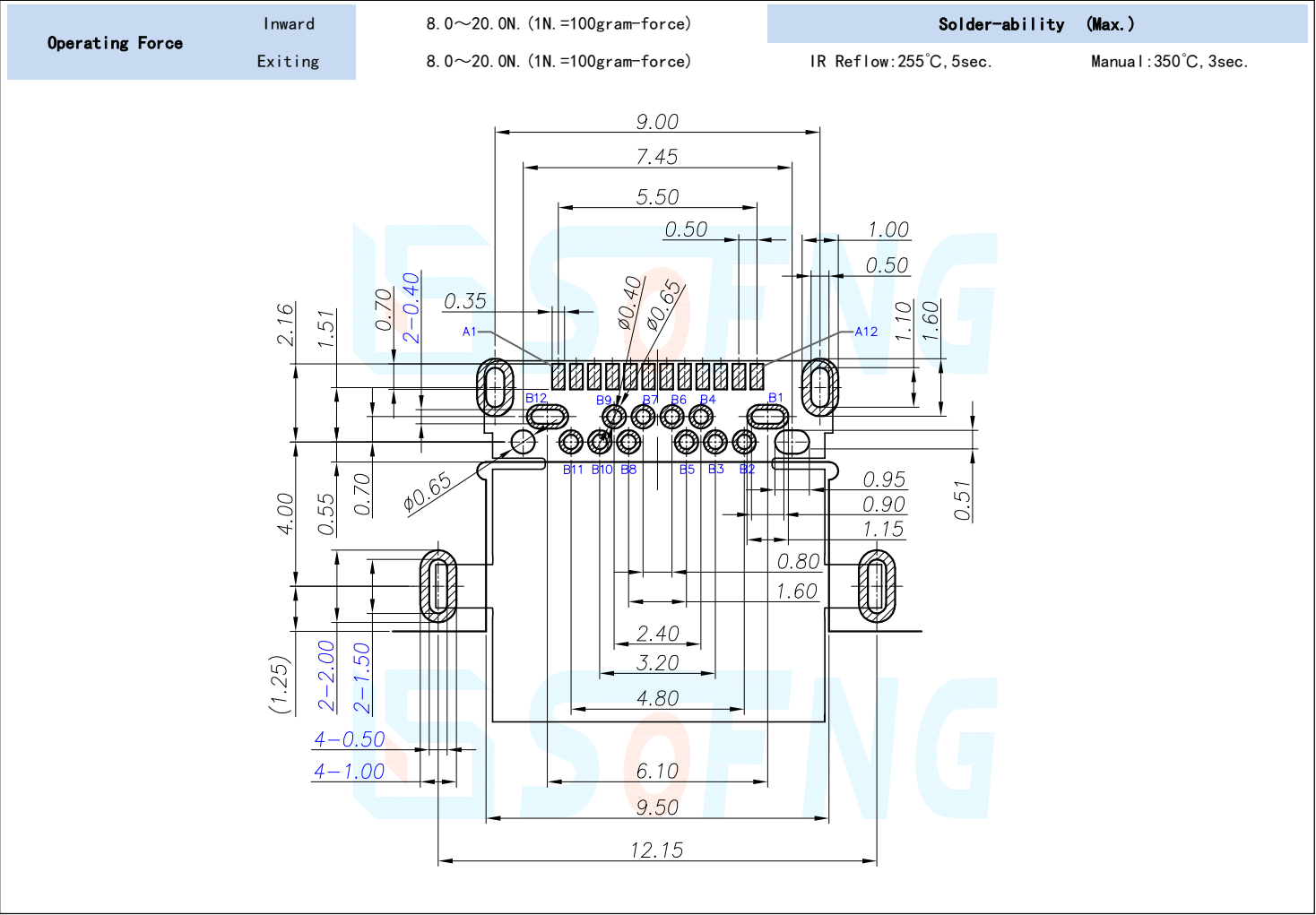
ANGLES

X.X : $\pm 3^\circ$ X.XX : $\pm 2^\circ$ 

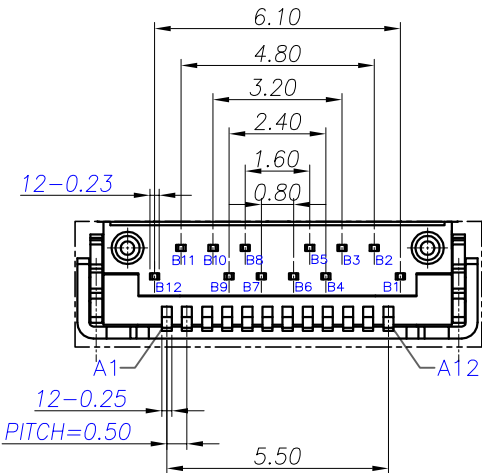
Material declaration

No.	NAME	MATERIAL	DESCRIPTION
① A	TERMINAL 接触端子	COPPER ALLOY 【G/F】	2.0 μm Ni PLATED OVERALL; 0.25 μm Au PLATED CONTACT AREA; GOLD FLASH ON SOLDER AREA.
② B	HOUSING 基座	THERMOPLASTIC	UL 94V-0,COLOR:BLACK;
③ C	SHIELDING PLATE 屏蔽壳	STAINLESS STEE	【G/F】 0.25 μm Ni PLATED OVERALL;
④ D	SHELL 外壳	STAINLESS STEE	【G/F】 0.25 μm Ni PLATED OVERALL;
⑤ E	GND RING 接地件	STAINLESS STEE	STAINLESS STEEL;

MATERIAL



PIN ASSIGNMENTS



PIN	Signal NAME	Description	PIN	Signal NAME	Description
A 1	GND	Ground return	B12	GND	Ground return
A 2	SSTXp1	Positive half of firs SuperSpeed TX differential pair	B11	SSRXp1	Positive half of second SuperSpeed RX differential pair
A 3	SSTXn1	Negative half of first SuperSpeed TX differential pair	B10	SSRXn1	Negative half of second SuperSpeed RX differential pair
A 4	V BUS	Bus Power	B 9	V BUS	Bus Power
A 5	CC1	Configuration Channel	B 8	SBU2	Sideband Use (SBU)
A 6	Dp1	Positive half of the USB 2.0 differential pair-Position 1	B 7	Dn2	Negative half of the USB 2.0 differential pair-Position 2
A 7	Dn1	Negative half of the USB 2.0 differential pair-Position 1	B 6	Dp2	Positive half of the USB 2.0 differential pair-Position 2
A 8	SBU1	Sideband Use (SBU)	B 5	CC2	Configuration Channel
A 9	V BUS	Bus Power	B 4	V BUS	Bus Power
A10	SSRXn2	Negative half of second SuperSpeed RX differential pair	B 3	SSTXn2	Negative half of first SuperSpeed TX differential pair2
A11	SSRXp2	Positive half of second SuperSpeed RX differential pair	B 2	SSTXp2	Positive half of firs SuperSpeed TX differential pair2
A12	GND	Ground return	B 1	GND	Ground return

注記 NOTICE

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