TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS III)

SSM6N15AFE

Load Switching Applications

• 2.5 V drive

N-ch 2-in-1

• Low ON-resistance: $R_{DS(ON)}$ = 3.6 Ω (max) (@V_{GS} = 4.0 V)

 $R_{DS(ON)} = 6.0 \Omega \text{ (max) } (@V_{GS} = 2.5 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	30	٧	
Gate-Source voltage		V_{GSS}	±20	٧	
Drain current	DC	ΙD	100	mA	
	Pulse	I_{DP}	400		
Power dissipation		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note:

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

1.6±0.05
1.2±0.05
1.2±0.05
1.2±0.05
1.2±0.05
1.2±0.05
1.2±0.07
20.0+0.1
1.5ource1 4.Source2
2.Gate1 5.Gate2
3.Drain2 6.Drain1

JEDEC —
JEITA —

2-2N1D

Weight: 3.0 mg (typ.)

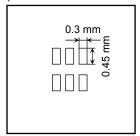
TOSHIBA

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

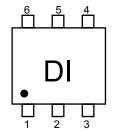
Note 1: Total rating

Mounted on FR4 board

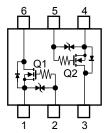
 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 0.135 \text{ mm}^2 \times 6)$



Marking



Equivalent Circuit (top view)



Start of commercial production 2010-11

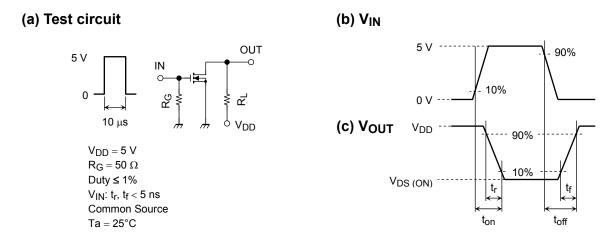
Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Drain-Source breakdown voltage		V (BR) DSS	$I_D = 0.1 \text{ mA}, V_{GS} = 0 \text{ V}$	30	_	_	V
		V (BR) DSX	$I_D = 0.1 \text{ mA}, V_{GS} = -10 \text{ V}$ (Note 3)	16	_	_	
Drain cut-off current		I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	_	_	1	μА
Gate leakage current		I _{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Gate threshold voltage	je	V _{th}	$V_{DS} = 3 \text{ V}, I_D = 0.1 \text{ mA}$	0.8	_	1.5	V
Forward transfer adm	nittance	Y _{fs}	$V_{DS} = 3 \text{ V}, I_D = 10 \text{ mA}$ (Note 2)	35	_	_	mS
Drain-Source ON resistance		D	$I_D = 10 \text{ mA}, V_{GS} = 4 \text{ V}$ (Note 2)	_	2.3	3.6	Ω
		R _{DS} (ON)	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note 2)	_	3.5	6.0	
Input capacitance		C _{iss}	V _{DS} = 3 V, V _{GS} = 0 V, f = 1 MHz	_	13.5	_	pF
Output capacitance		Coss		_	8.0	_	
Reverse transfer capacitance		C _{rss}		_	6.5	_	
Switching time	Turn-on time	t _{on}	$V_{DD} = 5 \text{ V}, I_D = 10 \text{ mA},$ $V_{GS} = 0 \text{ to } 5 \text{ V}, R_G = 50 \Omega$	_	5.5	_	ns
	Turn-off time	t _{off}		_	35	_	
Drain-source forward voltage		V _{DSF}	$I_D = -100 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 2)	_	-0.85	-1.2	V

Note 2: Pulse test

Note 3: If a reverse bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit



Precaution

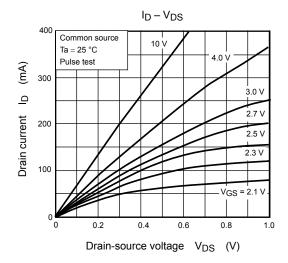
 V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 0.1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$) Please take this into consideration for using the device.

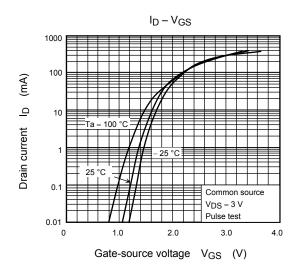
Do not use this device under avalanche mode. It may cause the device to break down.

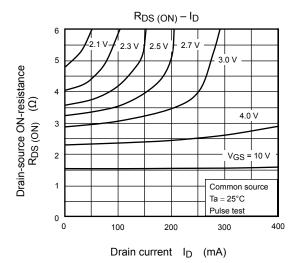
Handling Precaution

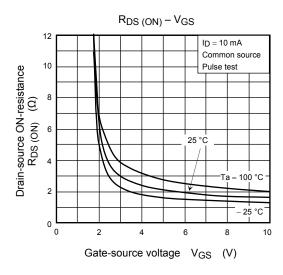
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

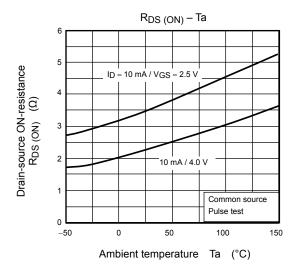
Thermal resistance $R_{th\ (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

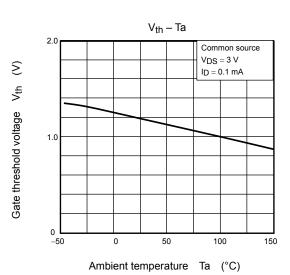






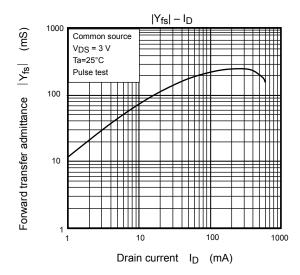


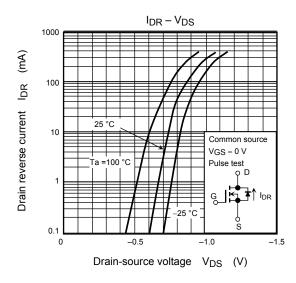


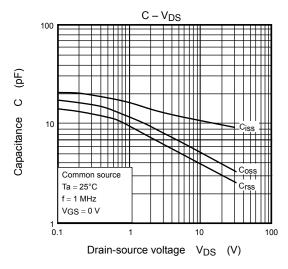


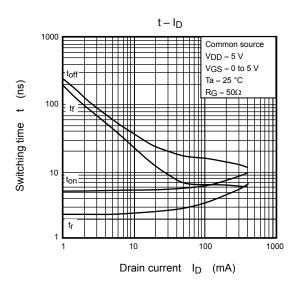
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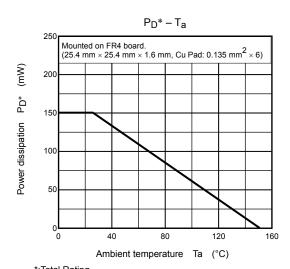
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*:Total Rating

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