OKI

Open up your dreams

OKI Semiconductor

ML22420/ML22460

Preliminary

4-Channel Mixing Speech Synthesis LSI with Built-In Serial ROM Interface

GENERAL DESCRIPTION

The ML22420/ML22460 are speech synthesis LSIs that use voice data ROM externally.

These LSIs incorporate into them an edit ROM, ADPCM2 decoder, 16-bit D/A converter, low-pass filter, monaural speaker amplifier, and an interface for external memory.

With functions necessary for a voice output circuit all integrated into a sigle chip, these LSIs can be incorporated into compact mobile devices more easily.
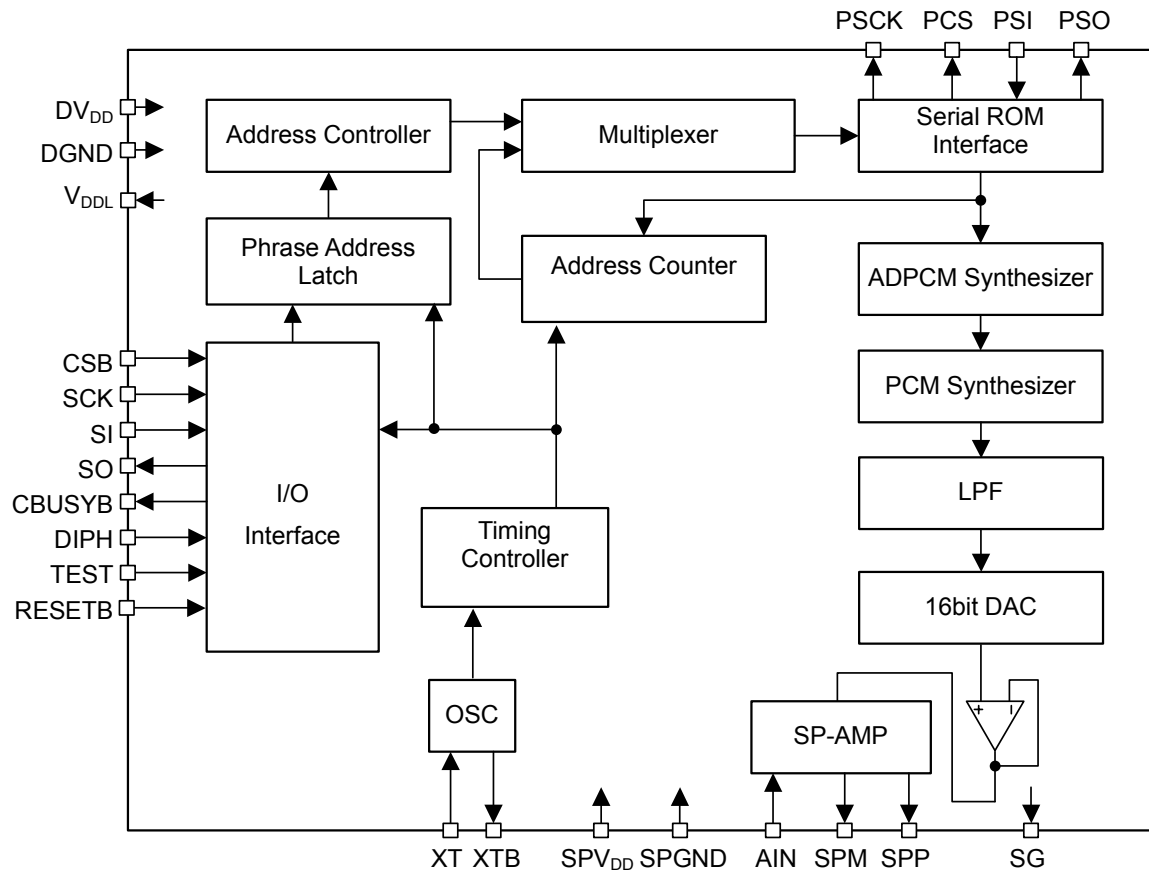
- Speech synthesis method: 4-bit OKI ADPCM2
                                      8-bit Nonlinear PCM
                                      8-bit PCM/16-bit PCM
                                      Can be specified for each phrase.
- Sampling frequency: 4.0 / 5.3 / 6.4 / 8.0 / 10.6 / 12.0 / 12.8 / 16.0 / 21.3 / 24.0 / 25.6 / 32.0 / 48.0 kHz
                                      Can be specified for each phrase.
- Built-in low-pass filter and 16-bit D/A converter
- Speaker driver amplifier: 0.7 W 8Ω (when VDD = 5 V) TBD
                                      Analog input: 2ch (internal: 1ch; external: 1ch)
- CPU command interface: Clock-synchronized 3-wired serial (ML22420) / I2C (ML22460)
- Maximum number of phrases: 1024 phrases, from 000h to 3FFh
- Volume control: Can be adjusted in 31 levels or set to OFF
- Repeat function: LOOP command
- Source oscillation frequency: 4.096 MHz
- Power supply voltage: 2.7 to 5.5 V
- Operating temperature range: –40 to +85°C
- Package: 30-pin plastic SSOP (SSOP30-P-56-0.65-K)
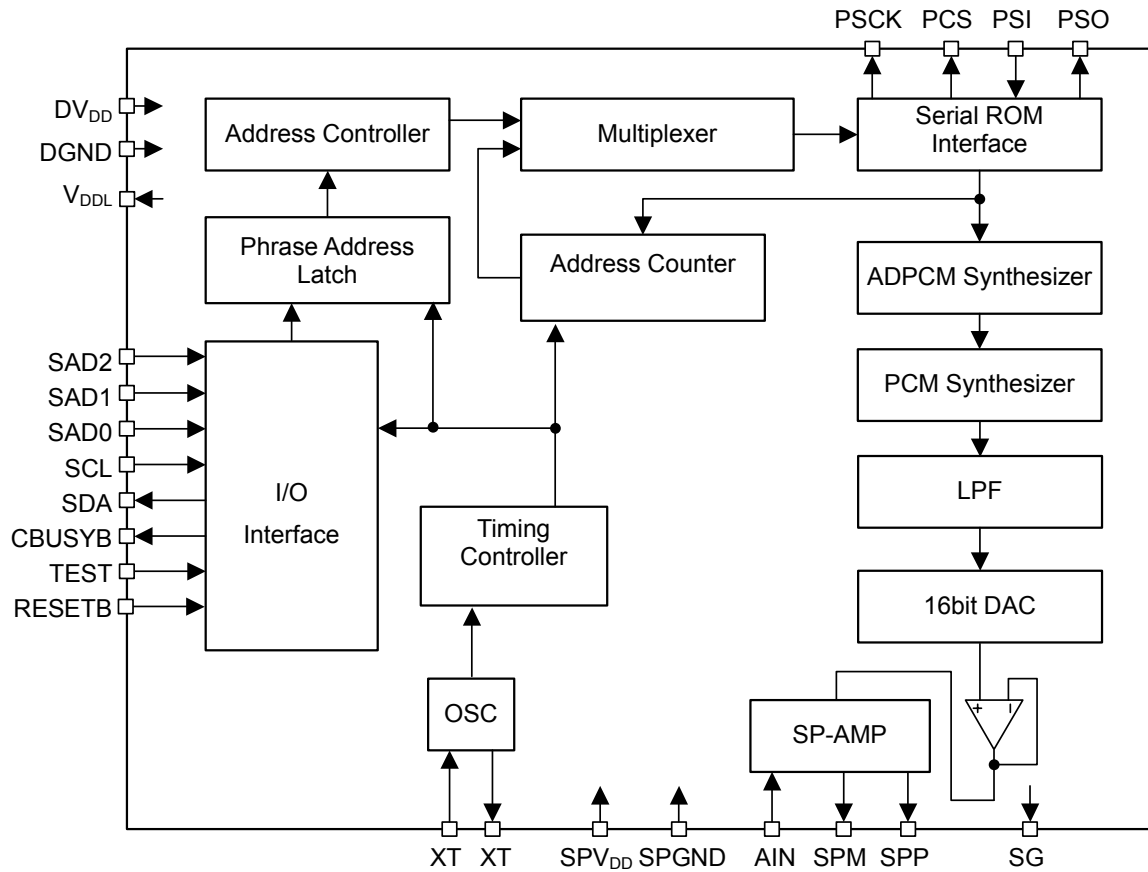- Product name: ML22420MB, ML22460MB

The table below summarizes the differences between the exsisting speech synthesis LSIs that use external memory and the ML22420/ML22460.

Item	MSM9841	ML2240	ML22420	ML22460
CPU interface	Parallel	Parallel/Serial	Serial	I2C
Memory interface	8-/16-bit parallel	8-bit parallel	Serial ROM	←
Playback method	4-bit ADPCM 4/5/6/7/8-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	4-bit ADPCM2 8-bit straight PCM 8-bit non-linear PCM 16-bit straight PCM	←	←
Maximum number of phrases	—	256	1024	←
Sampling frequency (kHz)	4.0/6.4/8.0/ 12.8/16.0/32.0	4.0/5.3/6.4/ 8.0/10.7/12.8 16.0	4.0/5.3/6.4/8.0/ 10.7/12.0/12.8/ 16.0/21.3/24.0/ 25.6/32.0/48.0	←
Clock frequency	4.096 MHz (has a crystal oscillator circuit built-in)	←	←	←
D/A converter	14-bit voltage-type	14-bit voltage-type	16-bit voltage-type	←
Low-pass filter	2D comb filter	FIR interpolation filter	←	←
Speaker driving amplifier	No	No	Built-in, 7W TBD (8Ω, when VDD = 5 V)	←
Simultaneous sound production function (mixing function)	Monaural	4-channel	←	←
Edit ROM	Yes	←	←	←
Volume control	8 levels	29 levels	32 levels	←
Silence insertion	—	20 to 1024 ms (4 ms steps)	←	←
Repeat function	Yes	←	←	←
External voice data reproduction function	Yes	No	No	No
Interval at which a seam is silent during continuous playback	No	←	←	←
Power supply voltage	2.7 V to 5.5 V	←	←	←
Package	56-pin QFP	80-pin TQFP	30-pin SSOP	←

*1: Continuous playback as shown on the right is possible.
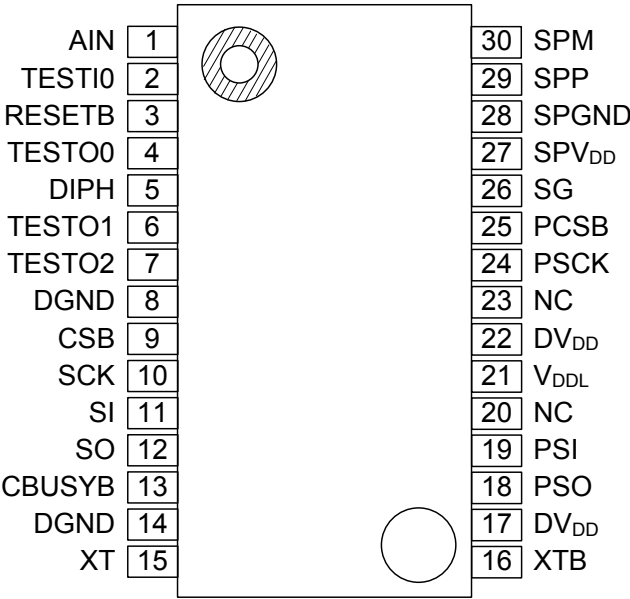

1 phrase   1 phrase

No silence interval
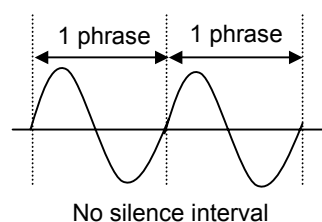
BLOCK DIAGRAM

ML22420 (synchronous serial interface)

ML22460 (I2C interface)

PIN CONFIGURATION (TOP VIEW)

ML22420 (Synchronous Serial Interface)

AIN	1	30	SPM
TESTI0	2	29	SPP
RESETB	3	28	SPGND
TESTO0	4	27	SPV_{DD}
DIPH	5	26	SG
TESTO1	6	25	PCSB
TESTO2	7	24	PSCK
DGND	8	23	NC
CSB	9	22	DV_{DD}
SCK	10	21	V_{DDL}
SI	11	20	NC
SO	12	19	PSI
CBUSYB	13	18	PSO
DGND	14	17	DV_{DD}
XT	15	16	XTB

NC: No Connection

30-Pin Plastic SSOP

ML22460 (I2C Interface)

AIN	1	30	SPM
TESTI0	2	29	SPP
RESETB	3	28	SPGND
TESTO0	4	27	SPV_{DD}
SAD0	5	26	SG
TESTO1	6	25	PCSB
TESTO2	7	24	PSCK
DGND	8	23	NC
SAD1	9	22	DV_{DD}
SCL	10	21	V_{DDL}
SDA	11	20	NC
SAD2	12	19	PSI
CBUSYB	13	18	PSO
DGND	14	17	DV_{DD}
XT	15	16	XTB

NC: No Connection

30-Pin Plastic SSOP

OKI Semiconductor **ML22420/ML22460**
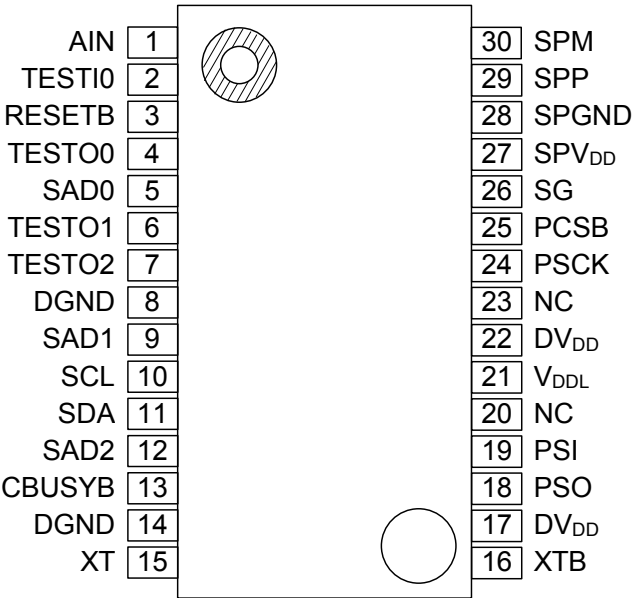
PIN DESCRIPTION

ML22420 (Synchronous Serial Interface)

Pin	Symbol	I/O	Initial value (*1)	Description
1	AIN	I	0	Speaker amplifier input pin.
2	TESTI0	I	0	Input pin for testing. Tie this pin at a "L" level (DGND level). This pin has a pull-down resistor built in.
3	RESETB	I	0 (*2)	Reset input pin. At "L" level input, the LSI enters the initial state. During a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a "L" level to this pin. After the power supply voltage is stabilized, drive this pin at a "H" level. By driving this pin at a "H" level, the entire circuit can be powered up. This pin has a pull-up resistor built in.
4	TESTO0	O	Hi-Z	Output pin for testing. Leave this pin open.
5	DIPH	I	0	Serial interface switching pin. Pin for choosing between rising edges and falling edges as to the edges of the SCK pulses used for shifting serial data input to the SI pin into the inside of the LSI. When this pin is at a "L" level, SI input data is shifted into the LSI on the rising edges of the SCK clock pulses; when this pin is at a "H" level, SI input data is shifted into the LSI on the falling edges of the SCK clock pulses.
6, 7	TESTO1 TESTO2	O	Hi-Z	Output pins for testing. Leave these pins open.
8, 14	DGND	—	—	Digital ground pin. Also serves as a ground pin for the internal memory.
9	CSB	I	1	Chip select pin. A "L" level on this pin accepts the SCK or SI inputs. When this pin is at a "H" level, neither the SCK nor SI signal is input to the LSI.
10	SCK	I	1	Synchronous serial clock input pin.
11	SI	I	0	Synchronous serial data input pin. When the DIPH pin is at a "L" level, data is shifted in on the rising edges of the SCK clock pulses. When the DIPH pin is at a "H" level, data is shifted in on the falling edges of the SCK clock pulses.
12	SO	O	Hi-Z	Synchronous serial data output pin. When the DIPH pin is at a "L" level, data is output on the falling edges of the SCK clock pulses. When the DIPH pin is at a "H" level, data is output on the rising edges of the SCK clock pulses. When the CSB pin is at a "H" level, this pin goes into a Hi-Z state.
13	CBUSYB	O	1	Command processing status output pin. This pin outputs a "L" level during command processing. Be sure to enter commands with the CBUSYB pin driven at a "H" level.

OKI Semiconductor   **ML22420/ML22460**

Pin	Symbol	I/O	Initial value (*1)	Description
15	XT	I	0	Connects to a crystal or a ceramic resonator. A feedback resistor of around 1 MΩ is built in between this XT pin and the XTB pin. When using an external clock, input the clock from this pin. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
16	XTB	O	1	Connects to a crystal or a ceramic resonator. When using an external clock, leave this pin open. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
17, 22	DV$_{DD}$	—	—	Digital power supply pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.
18	PSO	O	Hi-Z	Serial data output pin, for serial data for voice data.
19	PSI	I	0	Serial data input pin, for serial data for voice data.
20, 23	N.C	—	—	No-connect pins. Leave these pins open.
21	V$_{DDL}$	—	0	Regulator output pin for internal logic. Connect a capacitor of 10 μF or more between this pin and DGND.
24	PSCK	O	0	Serial clock input pin for memory interface.
25	PCSB	O	1	Chip select pin for memory interface. A "L" level on this pin accepts the PSCK/PSI signals. A "H" level on this pin does not accept the PSCK/PSI signals.
26	SG	—	0	Built-in speaker amplifier's reference voltage output pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.
27	SPV$_{DD}$	—	—	Speaker amplifier power supply pin. Connect a capacitor of 0.1 μF or more between this pin and SPGND.
28	SPGND	—	—	Speaker amplifier ground pin.
29	SPP	—	0	Positive output pin of the built-in speaker amplifier. Serves as a LINE output(*3) pin if the built-in speaker amplifier is not used.
30	SPM	—	Hi-Z	Negative output pin of the built-in speaker amplifier.

*1: Indicates the initial value at reset input or during power down.
*2: "H" during power down.
*3: A LINE output (signal) is a voice signal before being amplified by the built-in speaker amplifier.

ML22460 (I2C interface)

Pin	Symbol	I/O	Initial value (*1)	Description
1	AIN	I	0	Speaker amplifier input pin.
2	TESTI0	I	0I	Input pin for testing. Tie this pin at a "L" level (DGND level). This pin has a pull-down resistor built in.
3	RESETB	I	0 (*2)	Reset input pin. At "L" level input, the LSI enters the initial state. During a reset input, the entire circuit is stopped and enters a power down state. Upon power-on, input a "L" level to this pin. After the power supply voltage is stabilized, drive this pin at a "H" level. By driving this pin at a "H" level, the entire circuit can be powered up. This pin has a pull-up resistor built in.
4	TESTO0	O	Hi-Z	Output pin for testing. Leave this pin open.
5, 9, 12	SAD0 SAD1 SAD2	I	0	Slave address select pins.
6, 7	TESTO1 TESTO2	O	Hi-Z	Output pins for testing. Leave these pins open.
8, 14	DGND	—	—	Digital ground pin. Also serves as a ground pin for the internal memory.
10	SCL	I	0	I2C serial clock input pin.
11	SDA	IO	0	I2C serial data input/output pin. Input/output pin used to set write mode/read mode, write addresses, and write/read data. When configured as output: N-channel open drain output When configured as input: High-impedance input
13	CBUSYB	O	1	Command processing status output pin. This pin outputs a "L" level during command processing. Be sure to enter commands with the CBUSYB pin driven at a "H" level.
15	XT	I	0	Connects to a crystal or a ceramic resonator. A feedback resistor of around 1 MΩ is built in between this XT pin and the XTB pin. When using an external clock, input the clock from this pin. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
16	XTB	O	1	Connects to a crystal or a ceramic resonator. When using an external clock, leave this pin open. If a crystal or a ceramic resonator is used, connect it as close to the LSI as possible.
17, 22	DV$_{DD}$	—	—	Digital power supply pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.
18	PSO	O	Hi-z	Serial data output pin for voice data.
19	PSI	I	0	Serial data input pin for voice data.
20, 23	N.C	—	—	No-connect pins. Leave these pins open.
21	V$_{DDL}$	—	0	Regulator output pin for internal logic. Connect a capacitor of 10 μF or more between this pin and DGND.

OKI Semiconductor   **ML22420/ML22460**

Pin	Symbol	I/O	Initial value (*1)	Description
24	PSCK	O	0	Serial clock input pin for memory interface.
25	PCSB	O	1	Chip select pin for memory interface. A "L" level on this pin accepts the PSCK/PSI signals. A "H" level on this pin does not accept the PSCK/PSI signals.
26	SG	—	0	Built-in speaker amplifier's reference voltage output pin. Connect a capacitor of 0.1 μF or more between this pin and DGND.
27	SPV$_{DD}$	—	—	Speaker amplifier power supply pin. Connect a capacitor of 0.1 μF or more between this pin and SPGND.
28	SPGND	—	—	Speaker amplifier ground pin.
29	SPP	—	0	Positive output pin of the built-in speaker amplifier. Serves as a LINE output(*3) pin if the built-in speaker amplifier is not used.
30	SPM	—	Hi-Z	Negative output pin of the built-in speaker amplifier.

*1: Indicates the initial value at reset input or during power down.
*2: "H" during power down.
*3: A LINE output (signal) is a voice signal before being amplified by the built-in speaker amplifier.

OKI Semiconductor   **ML22420/ML22460**

ABSOLUTE MAXIMUM RATINGS

(DGND = SPGND = 0 V, Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	−0.3 to +7.0	V
Input voltage	V_{IN}	—	−0.3 to DV_{DD}+0.3	V
Power dissipation	P_D		1.0	W
Output short-circuit current	I_{OS}	Applies to all pins except SPM, SPP, and V_{DDL}.	10	mA
		Applies to SPM and SPP pins.	TBD	mA
		Applies to V_{DDL} pin.	50	mA
Storage temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(DGND = SPGND = 0 V)

Parameter	Symbol	Condition	Range			Unit
Power supply voltage	DV_{DD}, SPV_{DD}	—	2.7 to 5.5			V
Operating temperature	T_{OP}	—	−40 to +85			°C
Master clock frequency	f_{OSC}	—	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
External crystal	Cd, Cg	—	15	30	45	pF

OKI Semiconductor

ELECTRICAL CHARACTERISTICS

DC Characteristics (3 V)

$DV_{DD} = SPV_{DD} = 2.7$ to 3.6 V, $DGND = SPGND = 0$ V, $Ta = -40$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.86 \times V_{DD}$	—	V_{DD}	V
"L" input voltage	V_{IL}	—	0	—	$0.14 \times V_{DD}$	V
"H" output voltage 1	V_{OH1}	$I_{OH} = -1$ mA	$V_{DD}-0.4$	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	$I_{OH} = -100$ µA	$V_{DD}-0.4$	—	—	V
"L" output voltage 1	V_{OL1}	$I_{OL} = 2$ mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	$I_{OL} = 100$ µA	—	—	0.4	V
"L" output voltage 3 (*4)	V_{OL3}	$I_{OL} = 3$ mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" input current 2 (*2)	I_{IH2}	$V_{IH} = V_{DD}$	0.3	2.0	15	µA
"H" input current 3 (*3)	I_{IH3}	$V_{IH} = V_{DD}$	2	30	200	µA
"L" input current 1	I_{IL1}	$V_{IL} = GND$	−10	—	—	µA
"L" input current 2 (*2)	I_{IL2}	$V_{IL} = GND$	−15	−2.0	−0.3	µA
"L" input current 3 (*6)	I_{IL3}	$V_{IL} = GND$	−200	−30	−2	µA
"H" output leakage current (*5)	I_{ILOH}	$V_{OH} = V_{DD}$	—	—	10	µA
"L" output leakage current (*5)	I_{ILOL}	$V_{OL} = GND$	−10	—	—	µA
Supply current during playback	I_{DD}	$f_{OSC} = 4.096$ MHz No output load	—	—	15	mA
Power-down supply current	I_{DDS2}	$Ta = -40$ to $+40°C$	—	1	10	µA
		$Ta = -40$ to $+85°C$	—	1	20	µA

*1: Applies to the XTB pin.
*2: Applies to the XT pin.
*3: Applies to the TESTI0 pin.
*4: Applies to the SCL and SDA pins.
*5: Applies to the TESTO0, TESTO1, and TESTO2 pins.
*6: Applies to the RESETB pin.

OKI Semiconductor **ML22420/ML22460**

DC Characteristics (5 V)

$DV_{DD} = SPV_{DD} = 4.5$ to 5.5 V, $DGND = SPGND = 0$ V, $Ta = -40$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	$0.8 \times V_{DD}$	—	V_{DD}	V
"L" input voltage	V_{IL}	—	0	—	$0.2 \times V_{DD}$	V
"H" output voltage 1	V_{OH1}	$I_{OH} = -1$ mA	$V_{DD}-0.4$	—	—	V
"H" output voltage 2 (*1)	V_{OH2}	$I_{OH} = -1$ 00μA	$V_{DD}-0.4$	—	—	V
"L" output voltage 1	V_{OL1}	$I_{OL} = 2$ mA	—	—	0.4	V
"L" output voltage 2 (*1)	V_{OL2}	$I_{OL} = 100$ μA	—	—	0.4	V
"L" output voltage 3 (*4)	V_{OL3}	$I_{OL} = 3$ mA	—	—	0.4	V
"H" input current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	μA
"H" input current 2 (*2)	I_{IH2}	$V_{IH} = V_{DD}$	0.8	5.0	20	μA
"H" input current 3 (*3)	I_{IH3}	$V_{IH} = V_{DD}$	20	100	400	μA
"L" input current 1	I_{IL1}	$V_{IL} = GND$	−10	—	—	μA
"L" input current 2 (*2)	I_{IL2}	$V_{IL} = GND$	−20	−5.0	−0.8	μA
"L" input current 3 (*6)	I_{IL3}	$V_{IL} = GND$	−400	−100	−20	μA
"H" output leakage current (*5)	I_{ILOH}	$V_{OH} = V_{DD}$	—	—	10	μA
"L" output leakage current (*5)	I_{ILOL}	$V_{OL} = GND$	−10	—	—	μA
Supply current during playback	I_{DD}	$f_{OSC} = 4.096$ MHz No output load	—	—	25	mA
Power-down supply current	I_{DDS2}	$Ta = -40$ to $+40°C$	—	1	15	μA
		$Ta = -40$ to $+85°C$	—	1	30	μA

*1: Applies to the XTB pin.
*2: Applies to the XT pin.
*3: Applies to the TESTI0 pin.
*4: Applies to the SCL and SDA pins.
*5: Applies to the TESTO0, TESTO1, and TESTO2 pins.
*6: Applies to the RESETB pin.

OKI Semiconductor   **ML22420/ML22460**

Analog Section Characteristics (3 V)

$DV_{DD} = SPV_{DD} = 2.7$ to 3.6 V, $DGND = SPGND = 0$ V, $Ta = -40$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}		—	—	2.0	Vp-p
LINE output load resistance	R_{LA}	During "silence" output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	0.1	—	2.0	V
SG output voltage	V_{SG}	—	$0.95 \times V_{DDL}/2$	$V_{DDL}/2$	$1.05 \times V_{DDL}/2$	V
SG output resistance	R_{SG}	During power down	92	115	138	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	$SPV_{DD} = 3.3V$, f = 1kHz $R_{SPO} = 8\Omega$, THD$\geq$10%	100	300	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

Analog Section Characteristics (5 V)

$DV_{DD} = SPV_{DD} = 4.5$ to 5.5 V, $DGND = SPGND = 0$ V, $Ta = -40$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AIN input resistance	R_{AIN}	—	15	20	25	kΩ
AIN input voltage range	V_{AIN}	—	—	—	2.0	Vp-p
LINE output load resistance	R_{LA}	During "silence" output	10	—	—	kΩ
LINE output voltage range	V_{AO}	No output load	$DV_{DD}/6$	—	$DV_{DD} \times 4/6$	V
SG output voltage	V_{SG}	—	$0.95 \times V_{DDL}/2$	$V_{DDL}/2$	$1.05 \times V_{DDL}/2$	V
SG output resistance	R_{SG}	During power down	92	115	138	kΩ
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω
Speaker amplifier output power	P_{SPO}	$SPV_{DD} = 5.0$ V, f = 1 kHz, $R_{SPO} = 8\Omega$, THD$\geq$10%	500	700	—	mW
Output offset voltage between SPM and SPP with no signal present	V_{OF}	SPIN–SPM gain = 0dB With a load of 8Ω	–50	—	+50	mV

AC Characteristics

$DV_{DD} = SPV_{DD} = 2.7$ to 3.6 V, 4.5 to 5.5 V, DGND = SPGND = 0 V, Ta = –40 to +85°C

Parameter	Applicable command	Symbol	Condition	Min.	Typ.	Max.	Unit
Master clock duty cycle		f_{duty}	—	40	50	60	%
RESETB input pulse width		t_{RST}	—	100	—	—	μs
Reset noise rejection pulse width		t_{NRST}	—	—	—	0.1	μs
Command input interval time	STOP, SLOOP, CLOOP, CVOL, AVOL	t_{INT}	f_{OSC} = 4.096 MHz	6	—	—	μs
	PUP1, PLAY	t_{INTP}		10	—	—	ms
Command input enable time	SLOOP (during continuous playback)	t_{cm}	f_{OSC} = 4.096 MHz	—	—	10	ms
CBUSYB "L" level output time	PUP	t_{PUP1}	f_{OSC} = 4.096 MHz When an external clock is input	4.8	5	5.2	ms
	PDWN	t_{PD1}	f_{OSC} = 4.096 MHz	—	—	6	μs
	AMODE (PUP = "0" DAEN (or SPEN) = "0"→"1")	t_{PUPA1}	f_{OSC} = 4.096 MHz When an external clock is input	1.8	2	2.2	ms
	AMODE (PUP = "1" DAEN (or SPEN) = "0"→"1")	t_{PUPA2}	f_{OSC} = 4.096 MHz When an external clock is input	64	66	68	ms
	AMODE (PUP = "0" DAEN (or SPEN) = "1"→"0")	t_{PDA1}	f_{OSC} = 4.096 MHz When an external clock is input	1.8	2	2.2	ms
	AMODE (PUP = "1" DAEN (or SPEN) = "1"→"0")	t_{PDA2}	f_{OSC} = 4.096 MHz When an external clock is input	64	66	68	ms
CBUSYB "L" level output time 1(*1)		t_{CB1}	f_{OSC} = 4.096 MHz	—	—	6	μs
SCK input enable time from CSB fall		t_{ESCK}	—	100	—	—	ns
SCK hold time from CSB rise		t_{CSH}	—	100	—	—	ns
Data floating time from CSB rise		t_{DOZ}	R_L = 3 kΩ	—	—	100	ns
Data setup time from SCK rise		t_{DIS1}	DIPH = "L"	50	—	—	ns
Data hold time from SCK rise		t_{DIH1}	DIPH = "L"	50	—	—	ns
Data output delay time from SCK rise		t_{DOD1}	R_L = 3 kΩ	—	—	80	ns
Data setup time from SCK fall		t_{DIS2}	DIPH = "H"	50	—	—	ns
Data hold time from SCK fall		t_{DIH2}	DIPH = "H"	50	—	—	ns
Data output delay time from SCK rise		t_{DOD2}	R_L = 3 kΩ	—	—	80	ns
SCK "H" level pulse width		t_{SCKH}	—	100	—	—	ns
SCK "L" level pulse width		t_{SCKL}	—	100	—	—	ns
CBUSYB output delay time from SCK rise		t_{DBSY1}	DIPH = "L"	—	—	150	ns
CBUSYB output delay time from SCK fall		t_{DBSY2}	DIPH = "H"	—	—	150	ns

Note: Output pin load capacitance = 45 pF (Max.)

*1: Applies to cases where a command is input except after a PUP, PDWN, or AMODE command input.

OKI Semiconductor
ML22420/ML22460

$DV_{DD} = SPV_{DD} = 2.7$ to 3.6 V, 4.5 to 5.5 V, $DGND = SPGND = 0$ V, $Ta = -40$ to $+85°C$

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Repeated START condition setup time	$t_{SU;STA}$	ML22460	0.6	—	—	μs
Data hold time: for I2C bus devices	$t_{HD;DAT}$	ML22460	0	—	0.9	μs
Data setup time	$t_{SU;DAT}$	ML22460	100	—	—	ns
SDA and SCL signal rise time	t_r	ML22460	20	—	300	ns
SDA and SCL signal fall time	t_f	ML22460	20	—	300	ns
START condition setup time	$t_{SU;STO}$	ML22460	0.6	—	—	μs
Bus free time between a STOP condition and a START condition	t_{BUF}	ML22460	1.3	—	—	μs
Capacitive load for each bus line	C_b	ML22460	—	—	400	PF
Noise margin at a "L" level in each device connected (including hysteresis)	V_{nL}	ML22460	$0.1 \times DV_{DD}$	—	—	V
Noise margin at a "H" level in each device connected (including hysteresis)	V_{nH}	ML22460	$0.1 \times DV_{DD}$	—	—	V
PSCK input enable time for PCSB fall	t_{EPCK}	—	200	—	—	ns
PSCK hold time for PCSB fall	t_{PCSH}	—	200	—	—	ns
Data floating time for PCSB rise	t_{DQZ}	$R_L = 3$ kΩ	—	—	100	ns
Data setup time for PSCK rise	t_{DDS}	—	50	—	—	ns
Data hold time for PSCK rise	t_{DDH}	—	50	—	—	ns
Data output delay time for PSCK rise	t_{DQD}	$R_L = 3$ kΩ	—	—	100	ns
PSCK a "H" level pulse width	t_{PCKH}	—	200	—	—	ns
PSCK a "L" level pulse width	t_{PCKL}	—	200	—	—	ns

Note: Output pin load capacitance = 55 pF (Max.)

OKI Semiconductor   **ML22420/ML22460**

TIMING DIAGRAMS

Serial CPU Interface Timing (When DIPH = "L") (for ML22420)
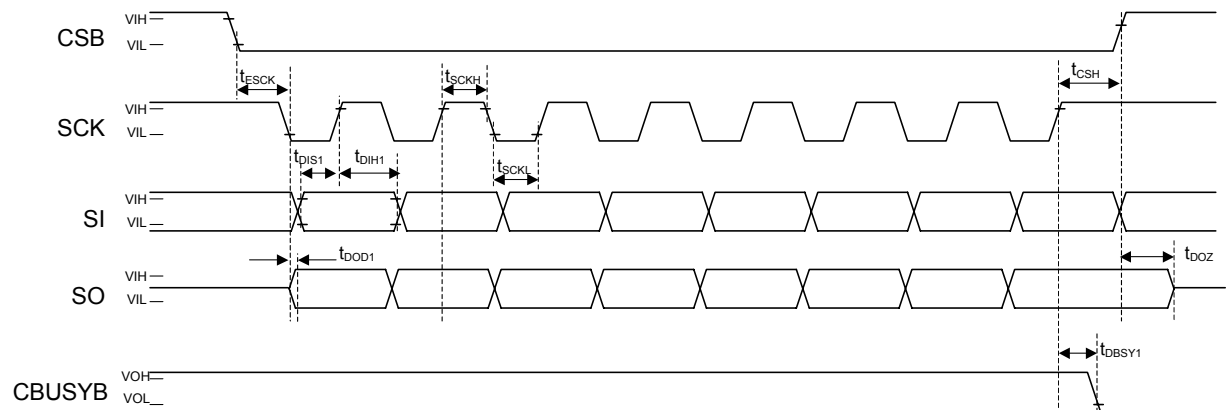
Serial CPU Interface Timing (When DIPH = "H") (for ML22420)
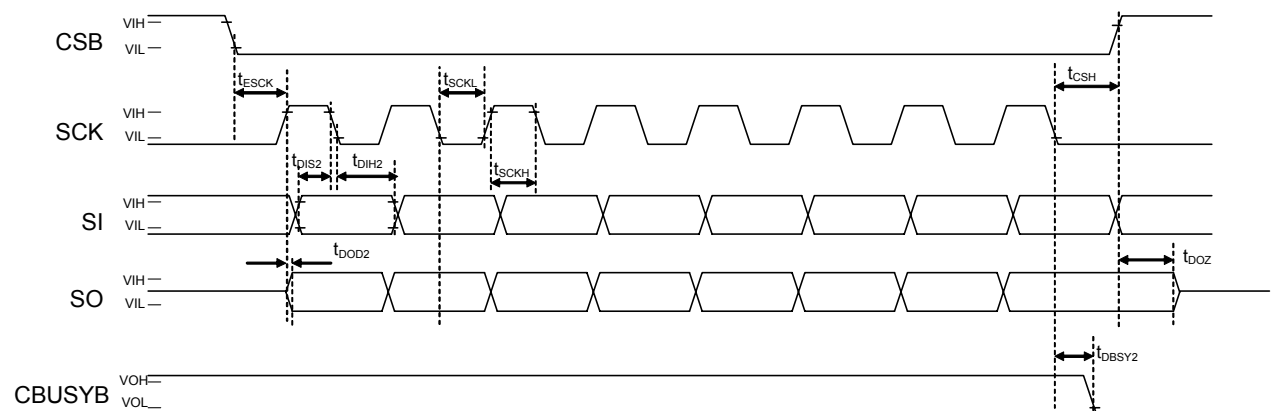
I2C Interface Timing (for ML22460)

ML22420/ML22460
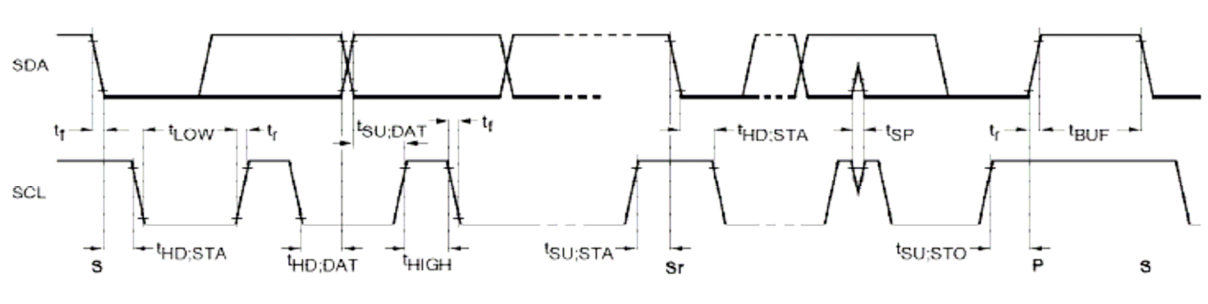
Serial Memory Interface Timing

Power-On Timing

Oscillation is stopped at power-on.
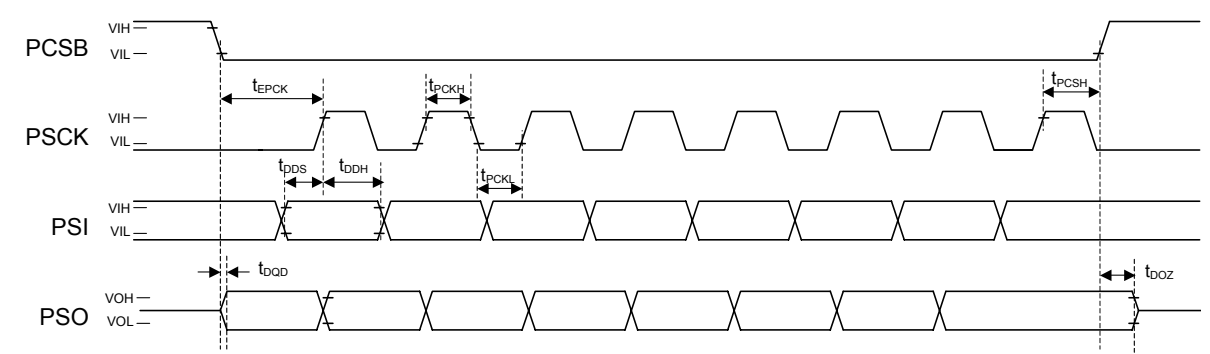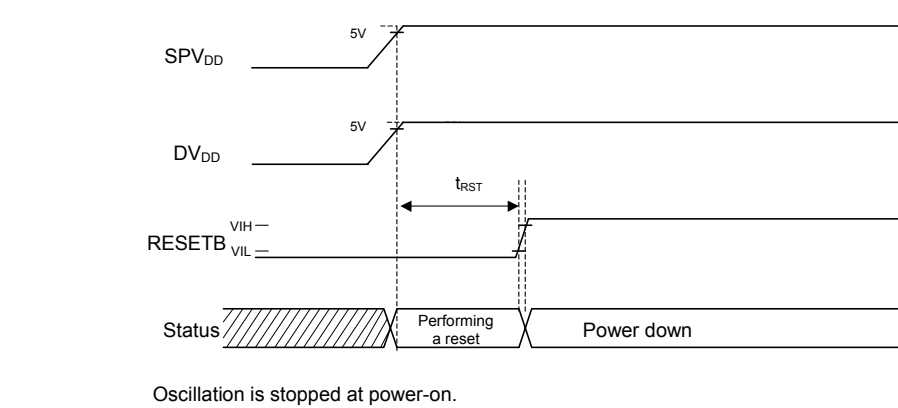
Power-Up Timing (for ML22420)
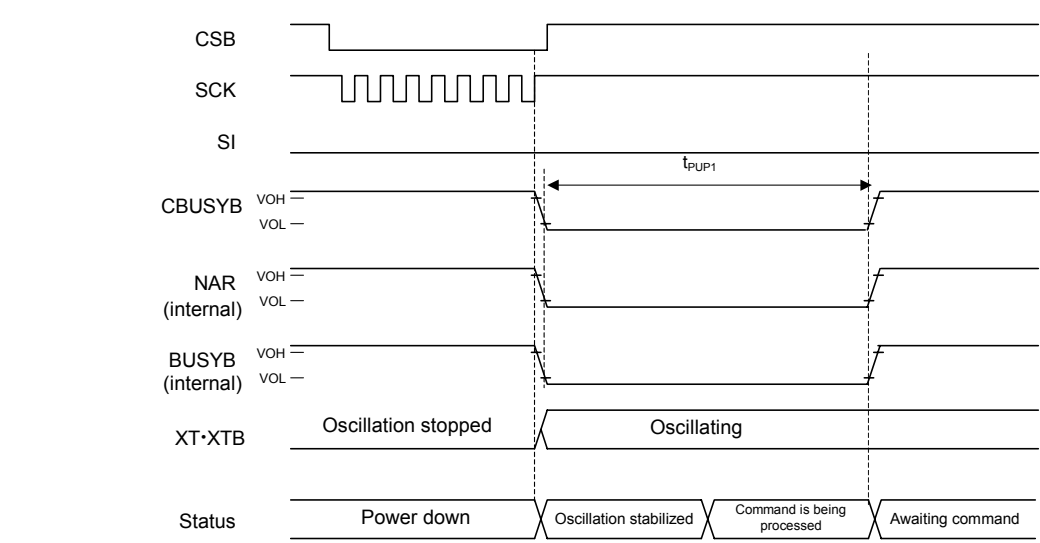
Power-Down Timing (for ML22420)
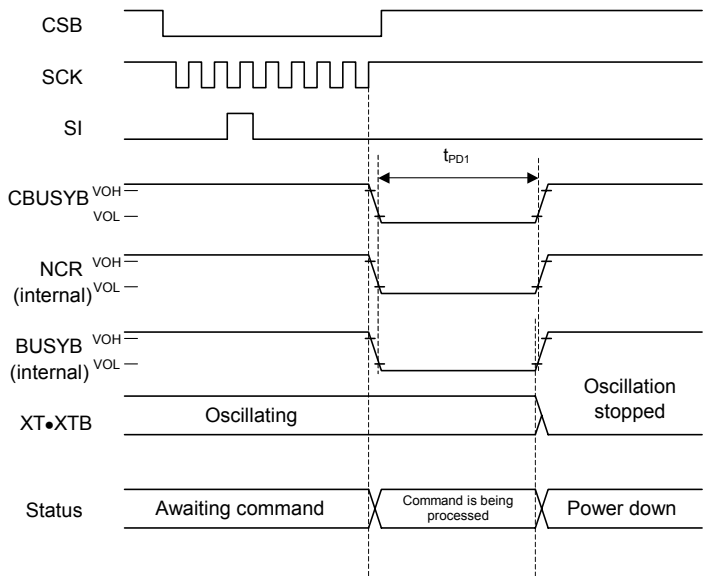
At RESET input
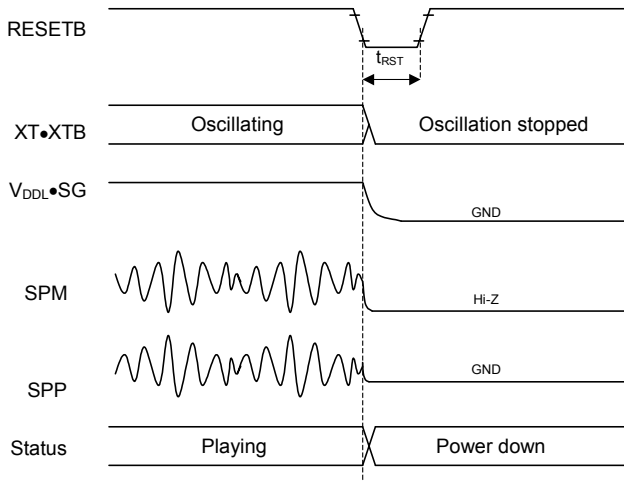
Note: The same timing applies in cases where the RESETB signal is input during waiting for command.

Playback Timing by the PLAY Command (for ML22420)
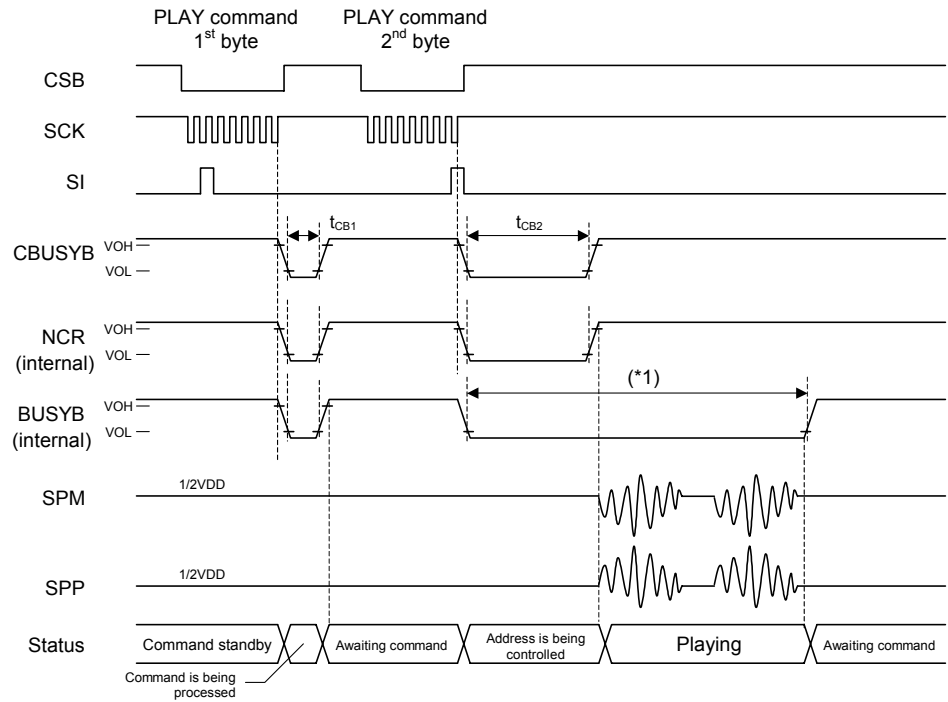
Note: Length of a "L" interval of BUSYB is = t_{CB2} + voice reproduction time length.

Playback Stop Timing (for ML22420)
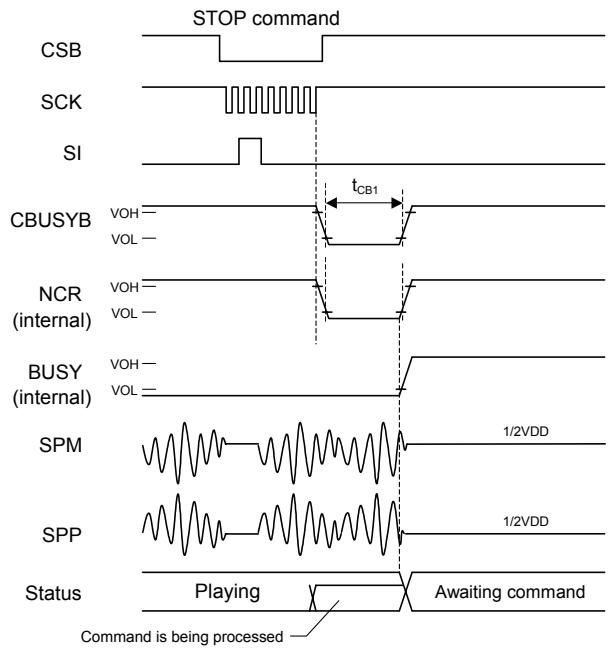
Continuous Playback Timing by the PLAY Command (for ML22420)
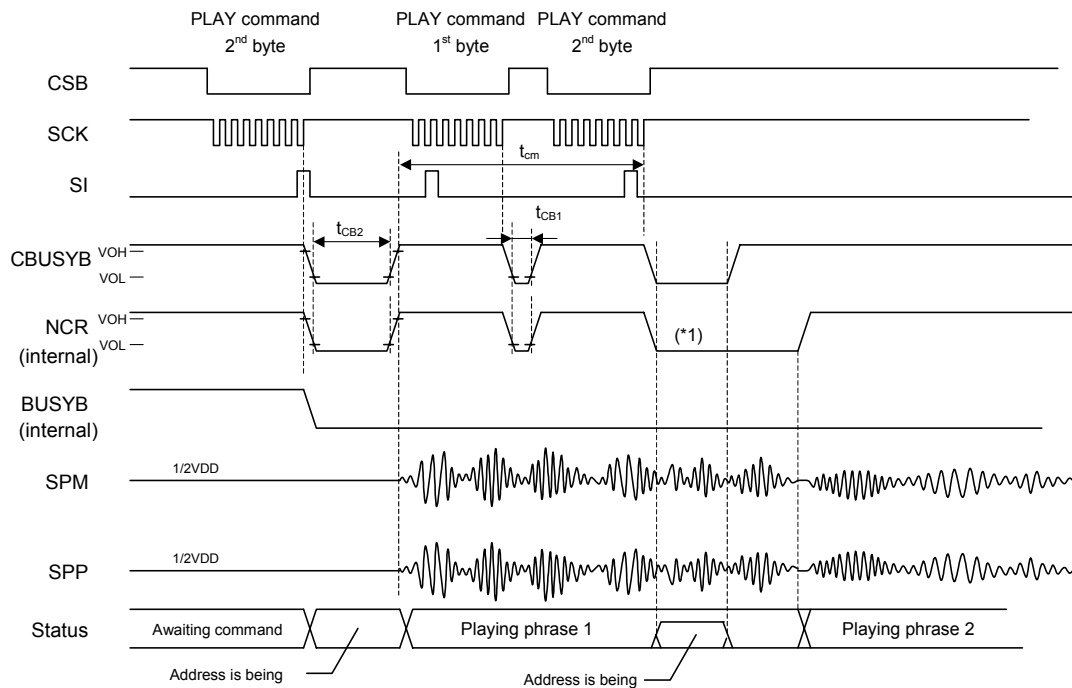
Silence Insertion Timing by the MUON Command (for ML22420)
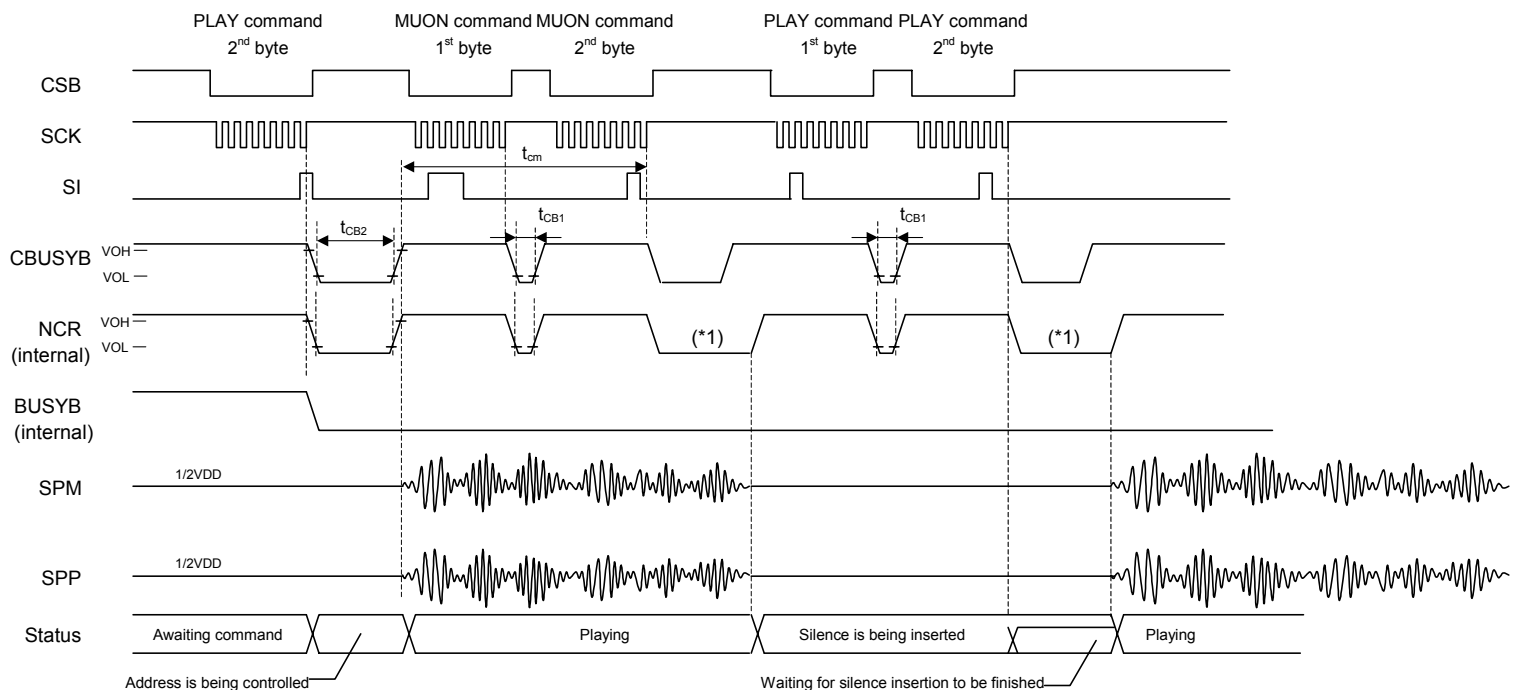
*1: The "L" level period of the NCR pin during playback or silence insertion operation varies depending on the timing at which the MUON command is input.

Repeat Playback Set/Release Timing by the SLOOP and CLOOP Commands (for ML22420)
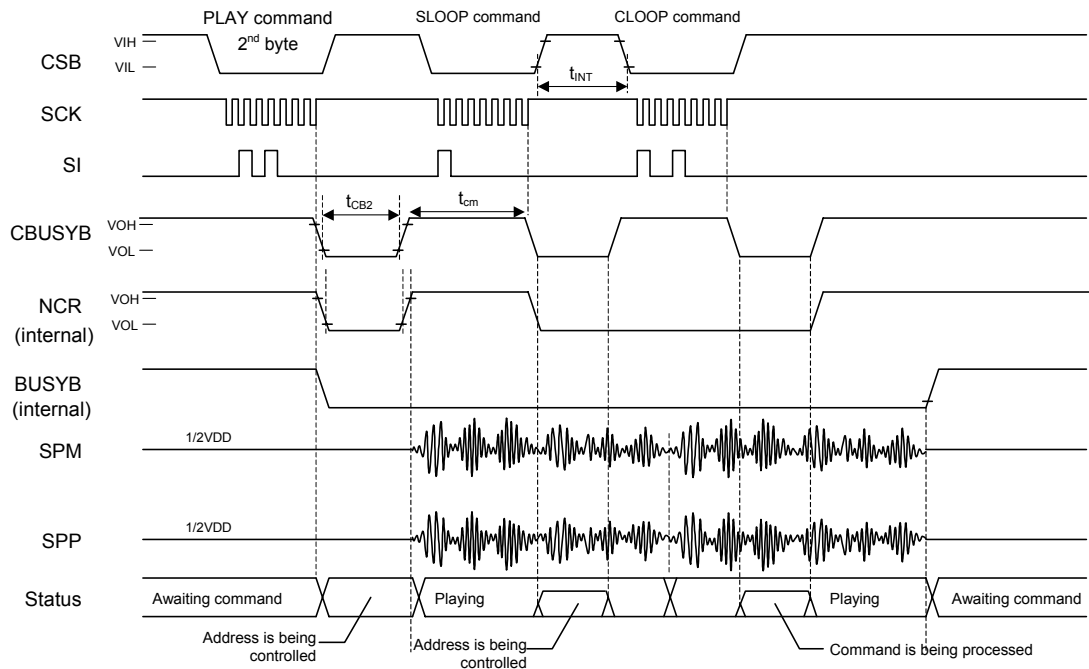
Timing of Volume Change by the CVOL Command (for ML22420)
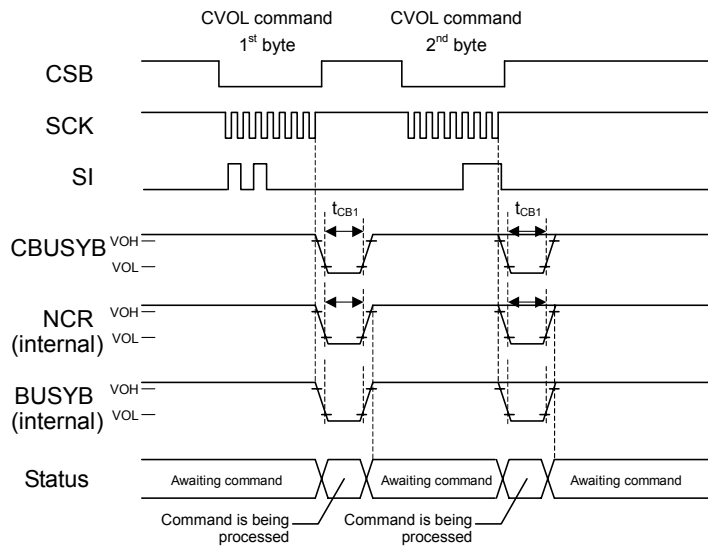
FUNCTIONAL DESCRIPTION

Synchronous Serial Interface (Applies to ML22420)

The CSB, SCK, SI, and SO pins are used to input various commands and data or read the status of the ML22420. Driving the CSB pin at a "L" level enables the serial CPU interface.

After the CSB pin is driven "L", command and data are input through the SI pin from the MSB in synchronization with the SCK clock signal.   Next, the data input through the SI pin is shifted into the LSI on the rising or falling edges of the SCK clock pulses. Then, a command is executed at the rising or falling edge of the eighth pulse of the SCK clock.

As for status reading, stauts is output from the SO pin in sync with the SCK clock signal after a "L" level is input to the CSB pin.

Choosing between rising edges and falling edges of the clock pulses input through the SCK pin is determined by the signal input through the DIPH pin:
- When the DIPH pin is at a "L" level, the data input through the SI pin is shifted into the LSI on the rising edges of the SCK clock pulses.
- When the DIPH pin is at a "H" level, the data input through the SI pin is shifted into the LSI on the falling edges of the SCK clock pulses.
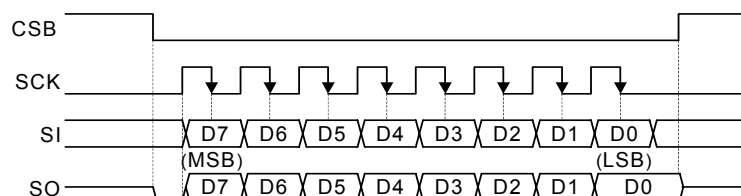
It is possible to input command and data in the LSI even by tying the CSB pin to a "L" level.   However, if unexpected pulses caused by noise are induced through the SCK pin, SCK clock pulses are incorrectly counted, causing a failure in normal recognition of command.   Driving the CSB pin at a "H" level returns the count of the SCK clock pulses to the initial state.

Command and Data Input Timing

• SCK rising edge operation (when DIPH pin = "L" level)
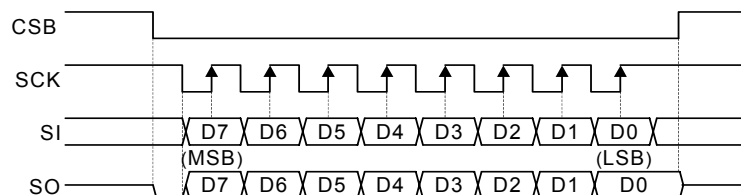
• SCK falling edge operation (when DIPH pin = "H" level)

OKI Semiconductor **ML22420/ML22460**

The table below shows the contents of each data output at a status read.

	Output status signal
MSB	Channel 3 BUSYB output (BUSYB3)
7SB	Channel 2 BUSYB output (BUSYB2)
6SB	Channel 1 BUSYB output (BUSYB1)
5SB	Channel 0 BUSYB output (BUSYB0)
4SB	Channel 3 NCR output (NCR3)
3SB	Channel 2 NCR output (NCR2)
2SB	Channel 1 NCR output (NCR1)
LSB	Channel 0 NCR output (NCR0)

The BUSYB signal outputs a "L" level when either a command is being processed or the playback of a particular channel is going on.   In other states, the BUSYB signal outputs a "H" level.   The NCR signal outputs a "L" level when either a command is being processed or a particular channel is in standby for playback.   In other states, the NCR signal outputs a "H" level.

OKI Semiconductor   **ML22420/ML22460**


I2C Interface (Applies to ML22460)

The I2C Interface is an interface (slave) that is compliant with I2C bus specification.   It supports Fast mode and enables data transmission/reception at 400 kbps.   The SCL and SDA pins are used to input various commands and data or read the status of the ML22460.   SAD0–2 pins are used to set a slave address.
For the master on the I2C bus to communicate with the ML22460, input the slave address of the ML22460 with the first seven bits after a START condition.   In the ML22460, the upper three bits of a slave address can be set using the SAD0–2 pins.   Next, determine the communication direction with the eighth bit: if the eighth bit is "0", it indicates that data is written from the master and if it is "0", it indicates that data is read from the master. From this onward, communication is made in units of bytes.   In this case, each byte is required to be acknowledged.   Use the protocols shown below to make I2C communication.
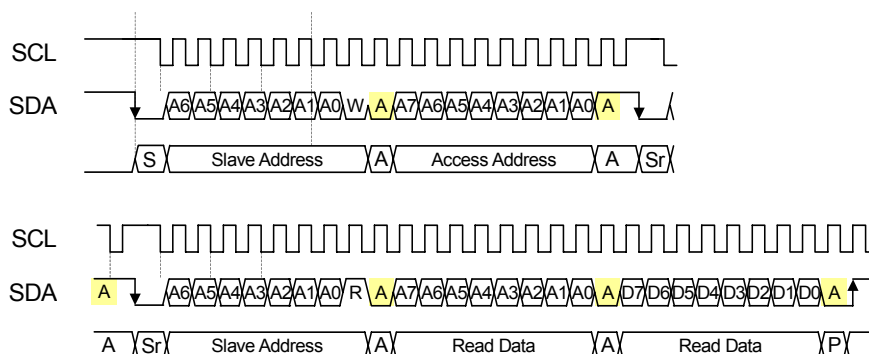

− Command flow at data write
   START condition
   Slave address +W(0)
   Write address
   Write data
   STOP condition

• Data write timing
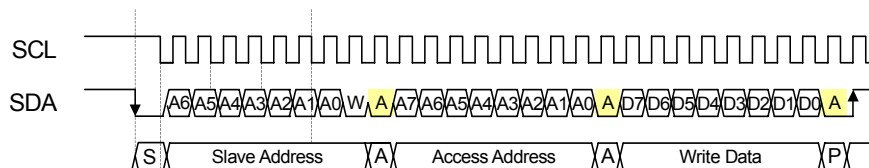
− Command flow at data read
   START condition
   Slave address +W(0)
   Read address
   START condition
   Slave address +R(1)
   Read data

• Data read timing

Use the SAD0–2 pins to set a slave address as follows:

SAD2	SAD1	SAD0	Lower 4 bits
0	0	0	0101
0	0	1	0101
0	1	0	0101
0	1	1	0101
1	0	0	0101
1	0	1	0101
1	1	0	0101
1	1	1	0101

The table below shows the contents of each data output at a status read.   Status is updated by the RDSTAT command; therefore, in order to read status, be sure to input the RDSTAT command.

	Output status signal (M/C bit = "0")
MSB	Channel 3 BUSYB output (BUSYB3)
7SB	Channel 2 BUSYB output (BUSYB2)
6SB	Channel 1 BUSYB output (BUSYB1)
5SB	Channel 0 BUSYB output (BUSYB0)
4SB	Channel 3 NCR output (NCR3)
3SB	Channel 2 NCR output (NCR2)
2SB	Channel 1 NCR output (NCR1)
LSB	Channel 0 NCR output (NCR0)

The BUSYB signal outputs a "L" level when either a command is being processed or the playback of a particular channel is going on.   In other states, the BUSYB signal outputs a "H" level.   The NCR signal outputs a "L" level when either a command is being processed or a particular channel is in standby for playback.   In other states, the NCR signal outputs a "H" level.

OKI Semiconductor   **ML22420/ML22460**

Command List

Each command is configured in 1-byte (8-bit) units. Each of the AMODE, AVOL FADR, PLAY, MUON, and CVOL commands forms one command by two bytes.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
PUP	0	0	0	0	0	0	0	0	Power-up command. Shifts the device currently powered down to a command wait state.
PDWN	0	0	1	0	0	0	0	0	Power-down command. Shifts the device from a command wait state to a power-down state.
RDSTAT	1	0	1	1	0	0	0	0	Command status read command. Reads the command status on each channel.
AMODE	0	0	0	0	0	1	0	0	Analog section control command. Configures settings for power-up operation and analog input/output.
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	PUP	
PLAY	0	1	0	0	F9	F8	C1	C0	Playback start command. Use the data of the 2nd byte to specify a phrase number. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
STOP	0	1	1	0	CH3	CH2	CH1	CH0	Playback stop command. Can be specified for each channel.
FADR	0	0	1	1	F9	F8	C1	C0	Playback phrase specification command. Can be specified for each channel.
	F7	F6	F5	F4	F3	F2	F1	F0	
START	0	1	0	1	CH3	CH2	CH1	CH0	Playback start command without phrase specification. Used to start playback on multiple channels at the same time after phrases are specified with the FADR command. After a phrase is played with the PLAY command, the same phrase can be played with this command.
MUON	0	1	1	1	CH3	CH2	CH1	CH0	Silence insertion command. Use the data of the 2nd byte to specify the length of silence. Can be specified for each channel.
	M7	M6	M5	M4	M3	M2	M1	M0	

OKI Semiconductor

ML22420/ML22460

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
SLOOP	1	0	0	0	CH3	CH2	CH1	CH0	Repeat playback setting command. The setting is enabled during playback. Can be specified for each channel.
CLOOP	1	0	0	1	CH3	CH2	CH1	CH0	Repeat playback cancellation command. When the STOP command is input, repeat playback mode is released automatically. Can be specified for each channel.
CVOL	1	0	1	0	CH3	CH2	CH1	CH0	Volume setting command. Use the data of the 2nd byte to specify volume. Can be specified for each channel.
	0	0	0	CV4	CV3	CV2	CV1	CV0	
AVOL	0	0	0	0	1	0	0	0	Analog volume setting command. Use the data of the 2nd byte to specify volume.
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	

- **Voice Synthesis Algorithm**

The ML22420/ML22460 contain four algorithm types to match the characteristic of playback voice: 4-bit ADPCM2 algorithm, 8-bit straight ADPCM2 algorithm, 8-bit non-linear PCM algorithm, and 16-bit straight PCM algorithm.
Key feature of each algorithm is described in the table below.

Voice synthesis algorithm	Applied waveform	Feature
OKI 4-bit ADPCM2	Normal voice waveform	OKI's specific speech synthesis algorithm of improved waveform follow-up with improved 4-bit ADPCM.
OKI 8-bit Nonlinear PCM	High-frequency components inclusive sound effect etc.	Algorithm, which plays back mid-range of waveform as 10-bit equivalent voice quality.
8-bit PCM		Normal 8-bit PCM algorithm
16-bit PCM		Normal 16-bit PCM algorithm

OKI Semiconductor   **ML22420/ML22460**

- Memory Allocation and Creating Voice Data

The ROM is partitioned into four data areas: voice (i.e., phrase) control area, test area, voice area, and edit ROM area.

The voice control area manages the ROM's voice data. It contains data for controlling the start/stop addresses of voice data for 1024 phrases, use/non-use of the edit ROM function and so on.

The test area contains data for testing.

The voice area contains actual waveform data.

The edit ROM area contains data for effective use of voice data. For the details, refer to the section of "Edit ROM Function."

No edit ROM area is available unless the edit ROM is used.

The ROM data is created using a dedicated tool.

<u>Configuration of ROM data</u>

Address	Area
0x00000 ... 0x01FFF	Voice control area (Fixed 64 Kbits)
0x02000 ... 0x02007	Test area
0x02008 ... max: 0xFFFFFF	Voice area
... max: 0xFFFFFF	Edit ROM area Depends on creation of ROM data.

Playback Time and Memory Capacity

The playback time depends on the memory capacity, sampling frequency, and playback method.
The equation showing the relationship is given below.
The equation below gives the playback time when the edit ROM function is not used.

$$\text{Playback time [sec]} = \frac{1.024 \times (\text{Memory capacity} - 64)\ [\text{Kbits}]}{\text{Sampling frequency [kHz]} \times \text{Bit length}}$$

where the bit length is 4 bits for 4-bit ADPCM2 and 8 or 16 bits for PCM.

Example: Let the sampling frequency be 16 kHz and 4-bit ADPCM2 algorithm. Then the playback time is approx. 261 seconds, as shown below.

$$\text{Playback time} = \frac{1.024 \times (16834 - 16)\ [\text{Kbits}]}{16\ [\text{kHz}] \times 4\ [\text{bits}]} \cong 261\ [\text{sec}]$$

- **Edit ROM Function**

The edit ROM function makes it possible to play back multiple phrases in succession.   The following functions are set using the edit ROM function:

・Continuous playback: There is no limit to the number of times a continuous playback can be specified.
                             It depends on the memory capacity only.
・Silence insertion function: 20 to 1024 ms

Using the edit ROM function enables an effective use of the memory capacity of voice ROM.
Below is an example of the ROM configuration in the case of using the edit ROM function.

Example 1   Phrases Using the Edit ROM Function
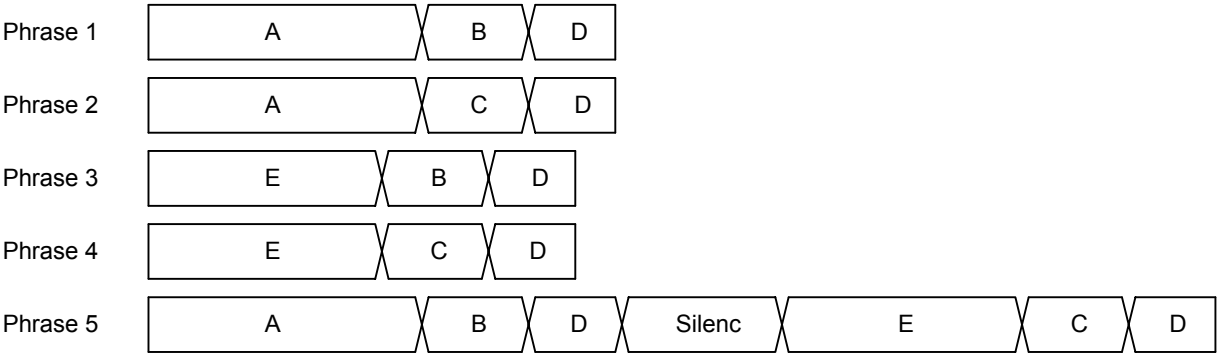
Example 2   Example of ROM Data Where Contents of Example 1 Are Stored in ROM
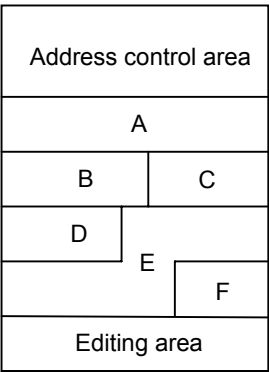
- **Mixing Function**

The ML22420/ML22460 can perform simultaneous mixing of four channels. It is possible to specify FADR, PLAY, STOP, and CVOL for each channel separately. Mixing is available regardless of frequency group.

・Precautions for Waveform Clamp at the Time of Channel Mixing
If channel mixing is done, the possibility of an occurrence of a clamp increases from the mixing calculation point of view. If it is known beforehand that a clamp will occur, then adjust the sound volume of each channel using the VOL command.

Figures below show cases where a phrase is played at a sampling frequency belonging to a different sampling frequency group.
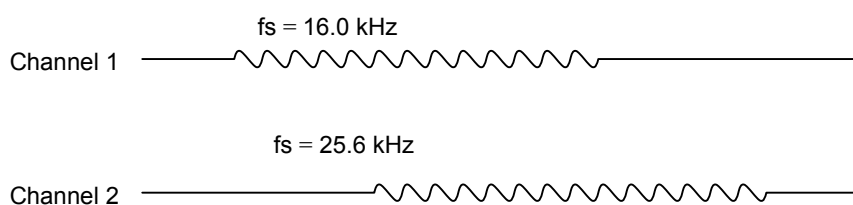
Figure 1   Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group during playback on channels 1 and 2
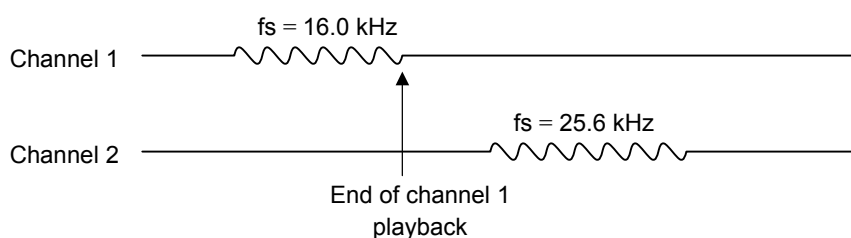
Figure 2   Case where a phrase is played at a sampling frequency belonging to a different sampling frequency group after playback is finished at the other channel

- **Description of Command Functions**
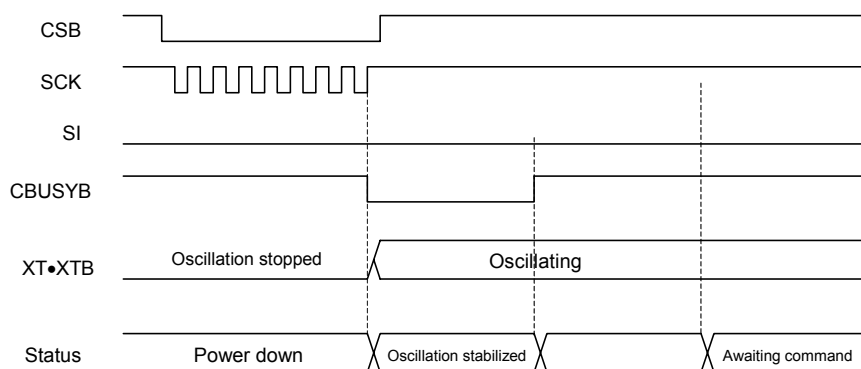
1. PUP command

· command

0	0	0	0	0	0	0	0

The PUP command is used to shift the ML22420/ML22460 from a power down state to a command waiting state.
The ML22420/ML22460 can only accept the PUP command while it is in a power down state.   Therefore, in a power-down state, the device will ignore any other command if entered.
The ML22420/ML22460 enters a power down state under any of the following conditions:
    1) When power is turned on
    2) At RESETB input
   3) When CBUSYB go to a "H" level after inputting the power down command

The regulator starts operating after the PUP command is entered.   Any command will be ignored if entered while oscillation is stabilized.   However, if a "L" level is input to the RESETB pin, the LSI enters a power down state immediately.
The built-in amplifier is not powered up by the PUP command.   It is powered up by the AMODE command.

2. PDWN command

command	0	0	1	0	0	0	0	0

The PDWN command is used to shift the ML22420/ML22460 from a command waiting state (both NCR and BUSYB are "H") to a power down state.   However, since every setting will be retained even after entering a power down state, no initial setting is required after power-up.   This command is invalid during playback.
To resume playback after the ML22420/ML22460 has shifted to a power down state, first input the PUP command and then input the PLAY command.
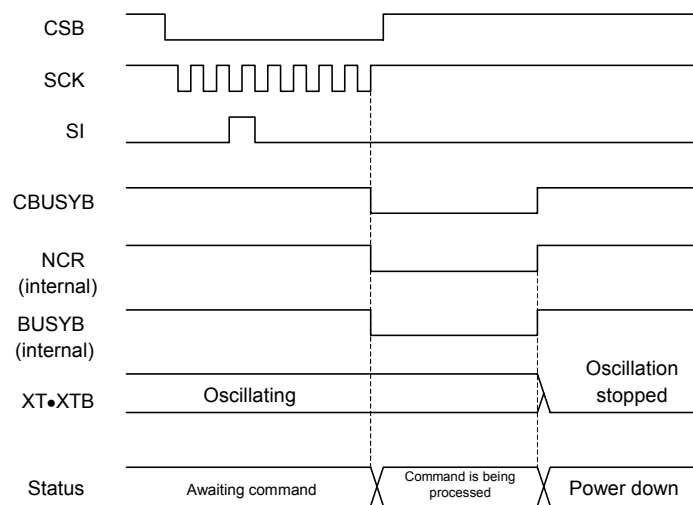
The regulator and the speaker amplifier stop operation after a lapse of command processing time after the PDWN command is input.   At this time, the SPM output of the speaker amplifier goes into a Hi-Z state to prevent generation of pop noise.

Initial stauts at reset input and status during power down
The status of each output pin is as follows:

Analog output pin	State
V_{DDL}	GND
SG	GND
SPM	HiZ
SPP	GND

3. RDSTAT command

·command	1	0	1	1	0	0	0	0

The RDSTAT command is used to read the NCR and BUSY signals that indicate the status of internal operation. The NCR signal outputs a "L" level while this LSI is performing command processing and goes to a "H" level when the LSI enters a command waiting state.   The BUSY signal outputs a "L" level during voice playback. The table below shows the contents of each data output at a status read.

	Output status signal
MSB	Channel 3 BUSYB output (BUSYB3)
7SB	Channel 2 BUSYB output (BUSYB2)
6SB	Channel 1 BUSYB output (BUSYB1)
5SB	Channel 0 BUSYB output (BUSYB0)
4SB	Channel 3 NCR output (NCR3)
3SB	Channel 2 NCR output (NCR2)
2SB	Channel 1 NCR output (NCR1)
LSB	Channel 0 NCR output (NCR0)

4. AMODE command

· command	0	0	0	0	0	1	0	0	1st byte
	FAD	DAG1	DAG0	AIG1	AIG0	DAEN	SPEN	PUP	2nd byte

The AMODE command is used to configure various settings for power-up operation and the analog section. This command is ignored in a power-down state, during transition to a power-up state, or during transition to a power-down state.
The detailed command settings are shown below.
Each setting is initialized upon reset release or power-up.

The FAD bit specifies whether to perform fade-out processing when the STOP command is input.   If the bit is set to "1" (Yes), fade-out processing is performed during a period of approx. 3 ms after the STOP command is input.   The BUSYB signal goes to a "H" level after fade-out processing.

| FAD	Fade-out processing
0	No (initial value)
1	Yes

The PUP bit specifies whether to suppress generation of "pop" noise.

- When the bit is set to "0" (No), if the DAEN bit is "1", the signal level on the SPP pin rises from the GND level to the SG level, at which time the speaker amplifier enters a power-up state.   If the SPEN bit is "1", the speaker amplifier enters a power-up state in about 2 ms.   If DAEN is "0", the signal level on the SPP pin changes from the SG level to the GND level, at which time the speaker amplifier enters a power-down state.   If SPEN is "0", the speaker amplifier enters a power-down state in about 2 ms.

- When the PUP bit is set to "1" (Yes), if the DAEN bit is "1", the SPP pin goes into a standby state in about 66 ms and then the signal level on the SPP pin goes to the SG level, at which time the speaker amplifier enters a power-up state.   If the SPEN bit is "1", the speaker amplifier enters a power-up state in about 66 ms.   If the DAEN bit is "0", the SPP pin goes into a standby state in about 66 ms and then the signal level on the SPP pin goes to the GND level, at which time the speaker amplifier enters a power-down state.   If the SPEN bit is "0", the speaker amplifier enters a power-down state in about 66 ms.

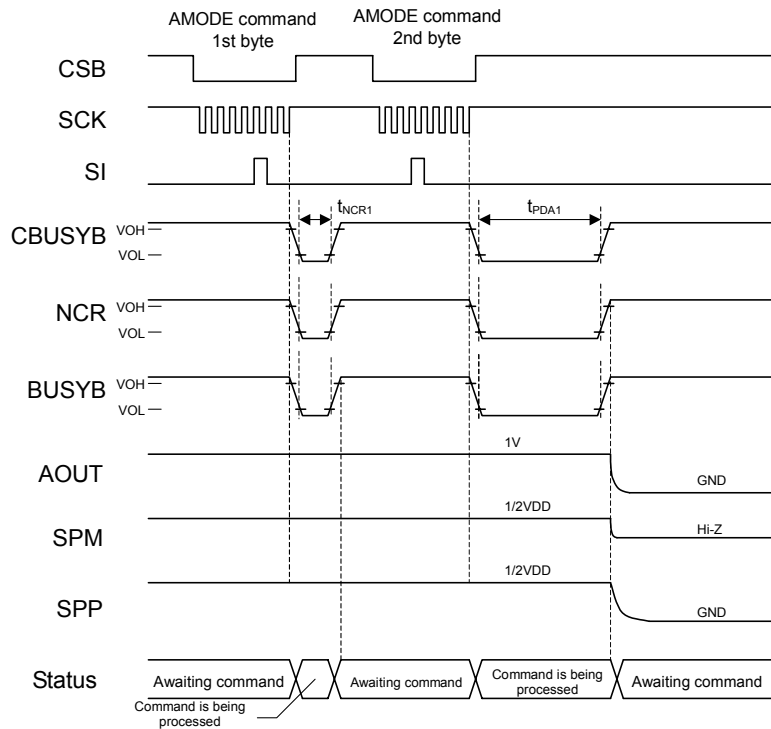| PUP	Pop noise suppression
0	No (initial value)
1	Yes

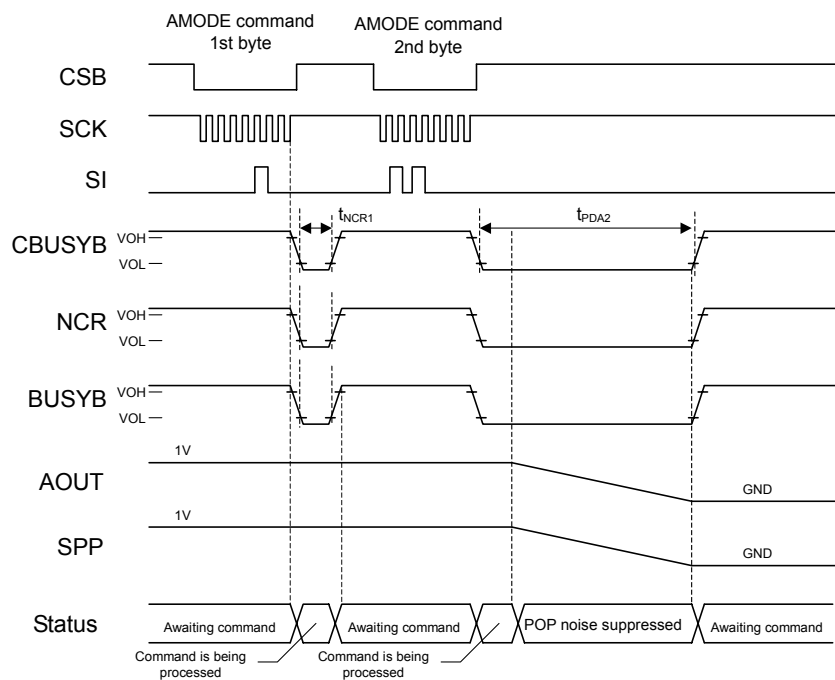• When PUP bit = "0", DAEN and SPEN bits = "0" → "1"
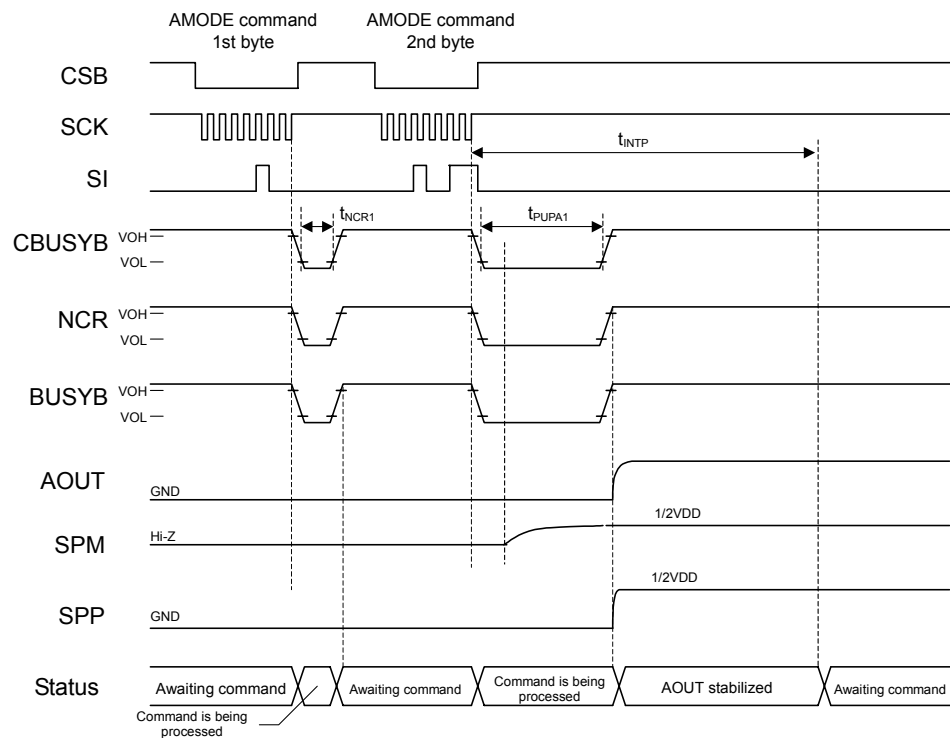
• When PUP bit = "1", DAEN and SPEN bits = "0" → "1"
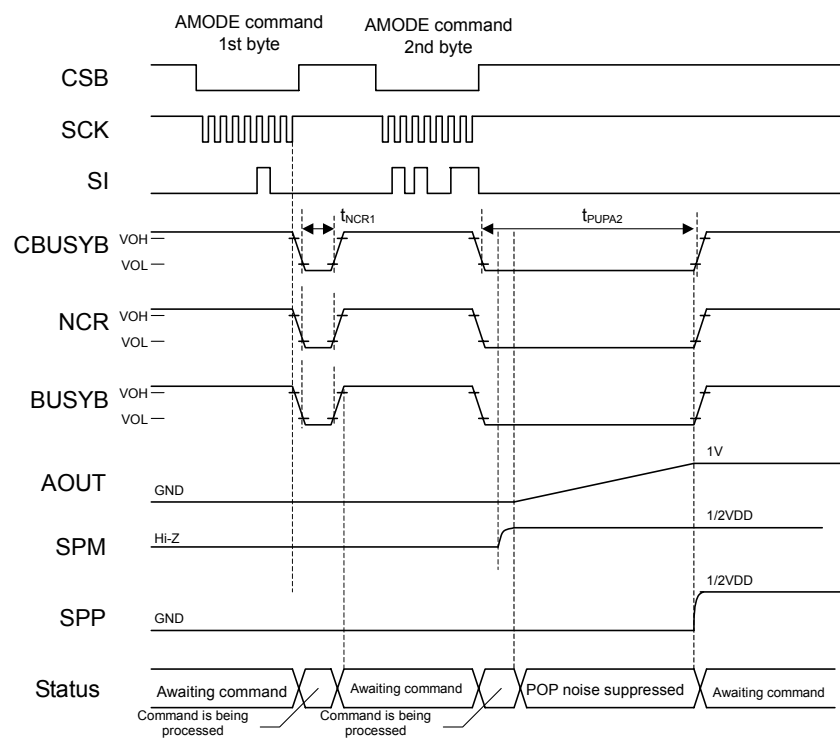
• When PUP bit = "0", DAEN and SPEN bits = "1" → "0"

• When PUP bit = "1", DAEN and SPEN bits = "1" → "0" (Applies only when SPEN = "0")

The DAG1–0 bits are used to set the gain of the internal DAC signal.   The AIG1–0 bits are used to set the gain of an analog signal from the AIN pin.

DAG1	DAG0	Volume
0	0	Input OFF
0	1	Input ON (–6 dB)
1	0	Input ON (0 dB) (initial value)
1	1	Setting prohibited (input ON (0 dB))

AIG1	AIG0	Volume
0	0	Input OFF (initial value)
0	1	Input ON (–6 dB)
1	0	Input ON (0 dB)
1	1	Setting prohibited (input ON (0 dB))

The DAEN bit takes power-up and power-down control of the DAC section.

DAEN	Status of the DAC section
0	Power-down state (initial value)
1	Power-up state

The SPEN bit takes power-up and power-down control of the speaker section.
When the SPEN bit = "0", the SPP pin is configured as a LINE output.

SPEN	Status of the speaker section
0	Power-down state (initial value)
1	Power-up state

5. PLAY command

· command

0	1	0	0	F9	F8	C1	C0	1st byte
F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The PLAY command is used to start playback with phrase specified.   This command can be input for each channel when the NCR signal is at a "H" level.

Since it is possible to specify a playback phrase (F9 to F0) at the time of creating a ROM that stores voice data, specify the phrase that was specified when the ROM was created.

The figure below shows the timing of phrase (F9 to F0 = 01H) playback.
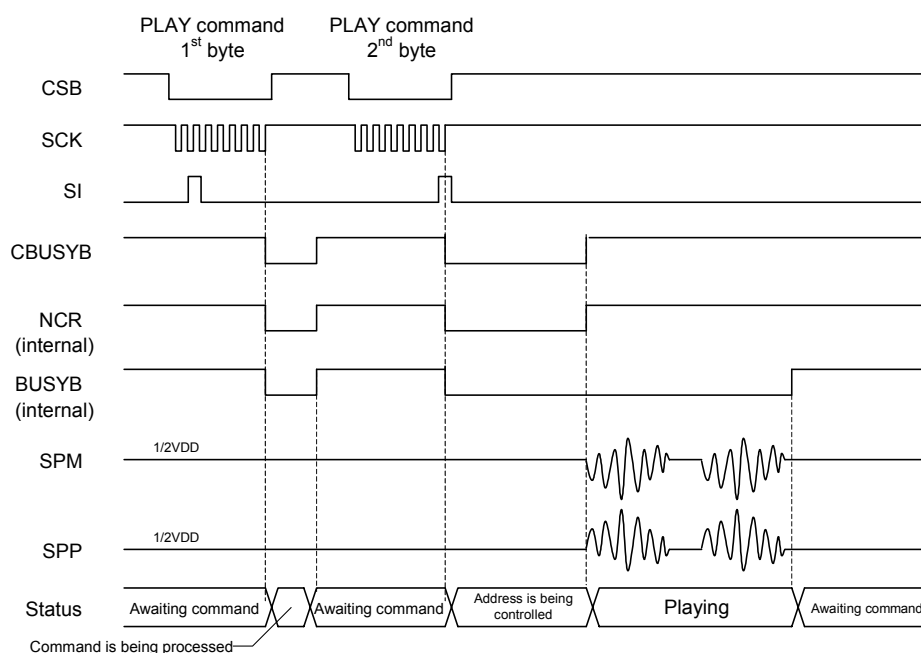
When the 1st byte of the PLAY command is input, the device enters a state awaiting input of the 2nd byte of the PLAY command after a lapse of command processing time.   When the 2nd byte of PLAY command is input, after a lapse of command processing time, the device starts reading from the ROM the address information of the phrase to be played.   Thereafter, playback operation starts, the playback is performed up to the specified ROM address, and then the playback terminates automatically.

The NCR1 signal is at a "L" level during address control, and goes "H" when the address control is finished. When this NCR signal goes "H", then it is possible to input the PLAY command for the next playback phrase.

During address control, the BUSYB signal is at a "L" level during playback and goes "H" when playback is finished.   Whether the playback is going on can be known by the BUSYB signal.

Channel settings

C1	C0	Channel
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

PLAY Command Input Timing for Continuous Playback

The diagram below shows the PLAY command input timing in cases where one phrase is played and then the next phrase is played in succession.
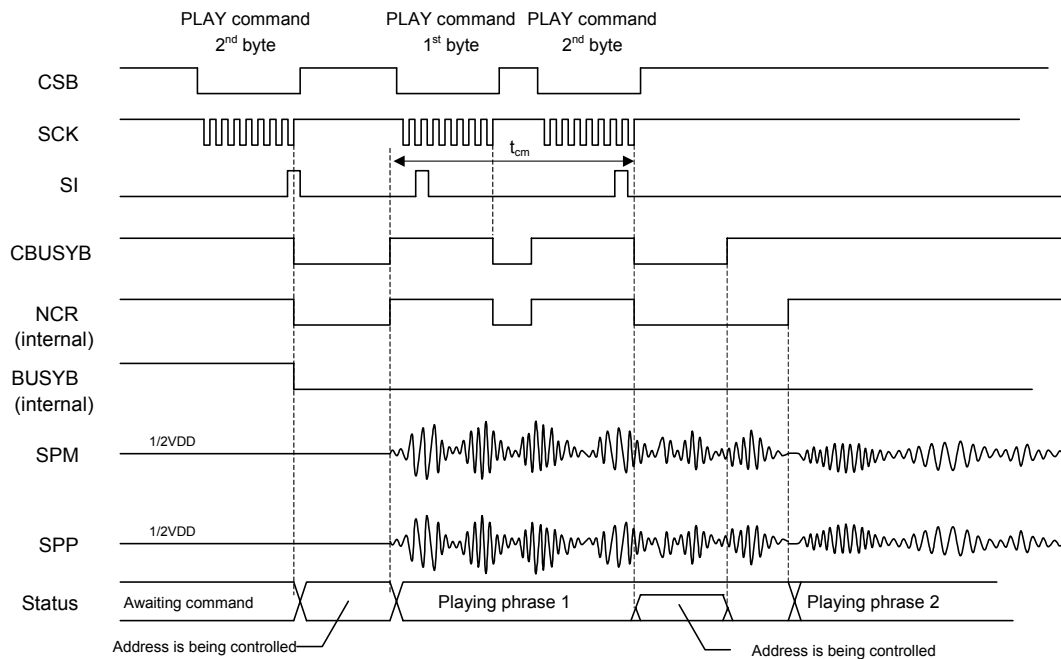
As shown in the diagram above, if continuous playback is carried out, input the PLAY command for the second phrase within 10 ms (tcm) after NCR goes "H".   This will make it possible to start playing the second phrase immediately after the playback of the first phrase finishes.   Phrases can thus be played continuously without inserting silence between phrases.
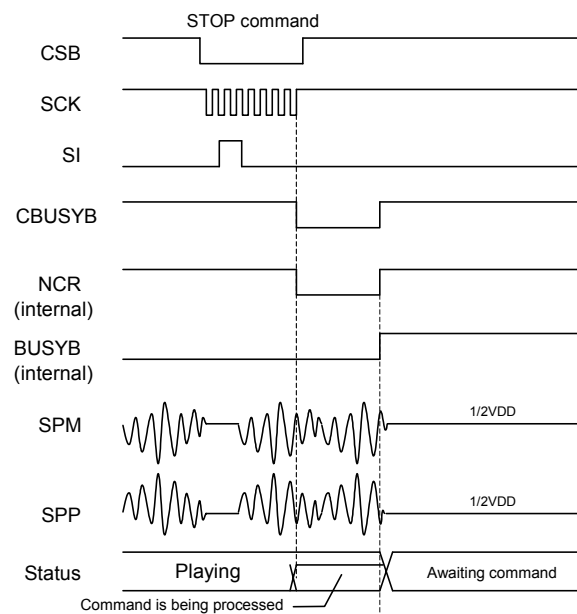
6. STOP command

· command	0	1	1	0	CH3	CH2	CH1	CH0

The STOP command is used to stop playback.   Setting any bit(s) from CH0 to CH3 to "1" stops playback on the corresponding channel(s).   If the speech synthesis processing for all channels stops, the NCRn and BUSYB signals go to a "H" level.

Although it is possible to input the STOP command regardless of the status of NCR during playback, a prescribed command interval time needs taking.

Note that the STOP command will be ignored if entered during power down or during a transition to a power-up or power-down state.

Channel settings

	Channel
CH0	Channel 0
CH1	Channel 1
CH2	Channel 2
CH3	Channel 3

The STOP command allows simultaneous specification of multiple channels.

7. FADR command

· command	0	0	1	1	F9	F8	C1	C0	1st byte
	F7	F6	F5	F4	F3	F2	F1	F0	2nd byte

The FADR command is used to specify a phrase to be played.   A playback channel and a playback phrase are set by this command.   The FADR command can be set for each channel; however, the command cannot be input for multiple channels simultaneously.

When a playback phrase is specified for each channel, use the START command to start playback.

Since it is possible to specify a playback phrase (F9 to F0) at the time of creating a ROM that stores voice data, specify the phrase that was specified when the ROM was created.

8. START command

· command

0	1	0	1	CH3	CH2	CH1	CH0

The START command starts playback of the phrase specified by the FADR command.   It is necessary to specify a playback phrase using the FADR command before inputting the START command.   Use the START command when starting playback on multiple channels simultaneously.   Setting any bits from CH0 to CH3 to "1" starts playback on the corresponding channels.

The figure below shows the timing when starting playback on channel 00 and channel 1 simultaneously.

OKI Semiconductor
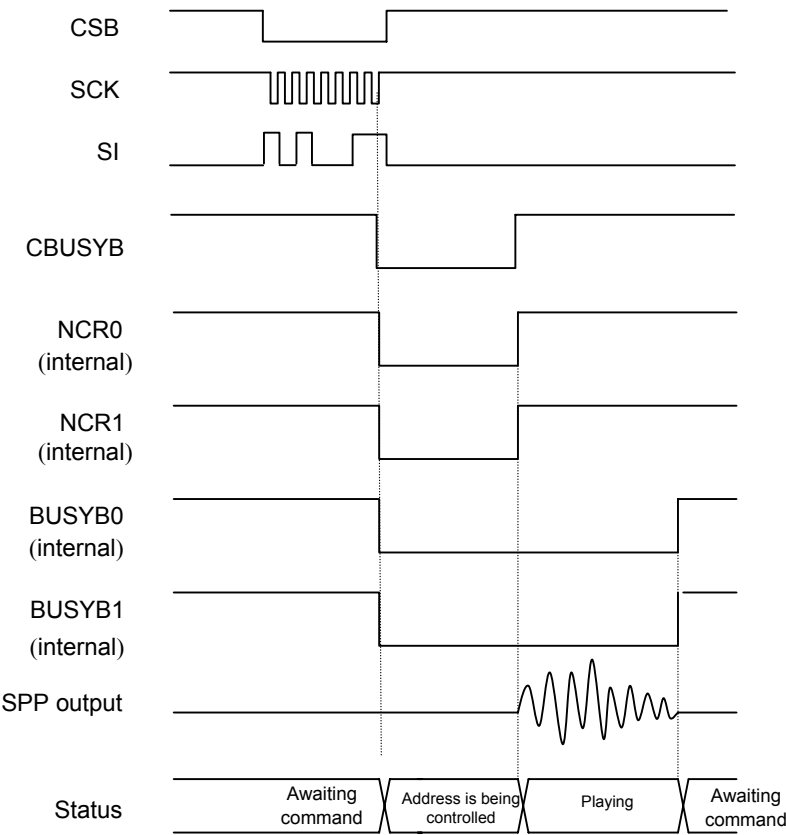
9. MUON command

· command

0	1	1	1	CH3	CH2	CH1	CH0	1st byte
M7	M6	M5	M4	M3	M2	M1	M0	2nd byte

The MUON command is a 2-byte command. This command is used to insert a silence between two playback phrases. The MUON command can be input when the NCR signal is at a "H" level.
Set the silence time length after inputting this command.
As the silence length (M7 to M0), a value between 20 ms and 1024 ms can be set at 4 ms intervals (252 steps in total).
The equation to set the silence time length is shown below.
The silence length (M7 to M0) must be set to 04h or higher.

$$t_{mu} = (2^7 \times (M7) + 2^6 \times (M6) + 2^5 \times (M5) + 2^4 \times (M4) + 2^3 \times (M3) + 2^2 \times (M2) + 2^1 \times (M1) + 2^0 \times (M0) + 1) \times 4ms$$

The figure below shows the timing of inserting a silence of 20 ms between the repetitions of a phrase of (F7–F0) = 01h.
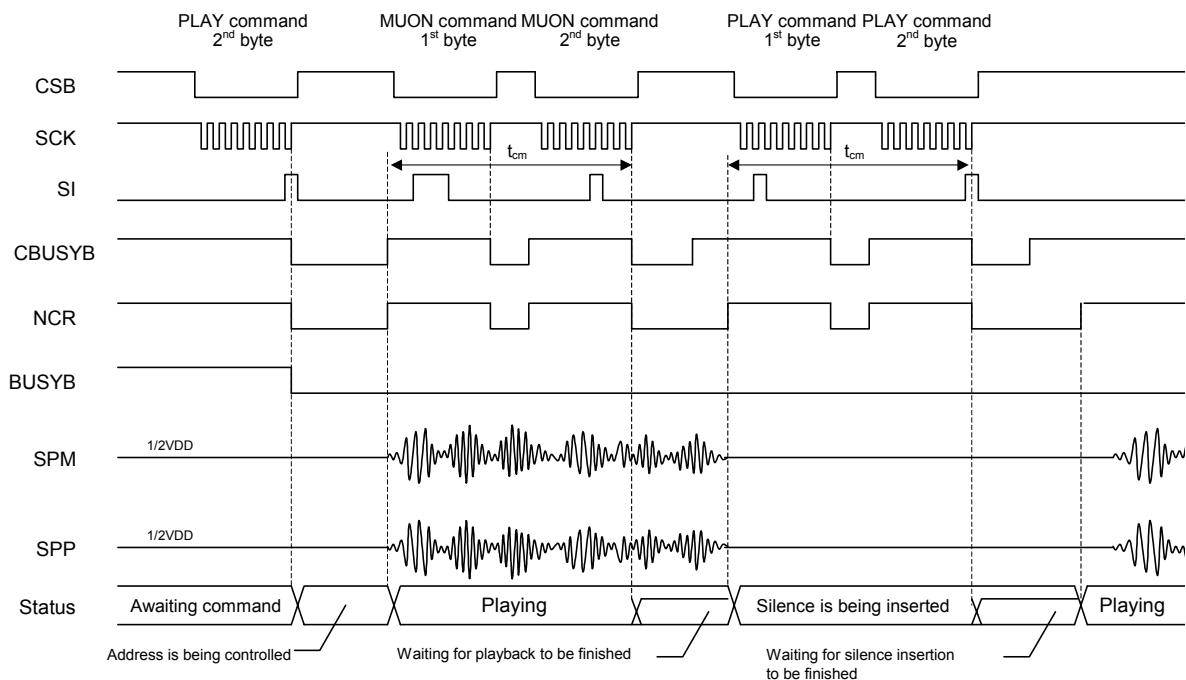
When the PLAY command is input, the address control over phrase 1 ends, the phrase playback starts, and the CBUSYB and NCR signals go to a "H" level. Input the MUON command after this CBUSYB signal changes to a "H" level. After the MUON command input, the NCR signal remains "L" until the end of phrase 1 playback, and the device enters a state waiting for the phrase 1 playback to terminate.
When the phrase 1 playback is terminated, the silence playback starts and the NCR1 signal goes to a "H" level. After this NCR signal has changed to a "H" level, re-input the PLAY command in order to play phrase 1.
After the PLAY command input, the NCR signal once again goes to a "L" level and the device enters a state waiting for the end of silence playback.
When the silence playback is terminated and then the phrase 1 playback starts, the NCR signal goes "H", and the device enters a state where it is possible to input the next PLAY or MUON command.
The BUSYB signal remains "L" until the end of a series of playback.

OKI Semiconductor **ML22420/ML22460**

10. SLOOP command

· command

| 1	0	0	0	CH3	CH2	CH1	CH0

The SLOOP command is used to set repeat playback mode.　Repeat playback can be specified for each channel. To release repeat playback mode, use the CLOOP command.

Since the SLOOP command is only valid during playback, be sure to input the SLOOP command while the NCR signal is at a "H" level after the PLAY command is input.　The NCR signal remains "L" during repeat playback mode.

Once repeat playback mode is set, the current phrase is repeatedly played until the repeat playback setting is released by the SLOOP command or until playback is stopped by the STOP command.　In the case of a phrase that was edited using the edit function, the edited phrase is repeatedly played.

Repeat playback mode is released if playback is stopped by the STOP command; therefore, if desired to repeat playback after the release of repeat playback mode, input the SLOOP command once again.

Following shows the SLOOP command input timing.
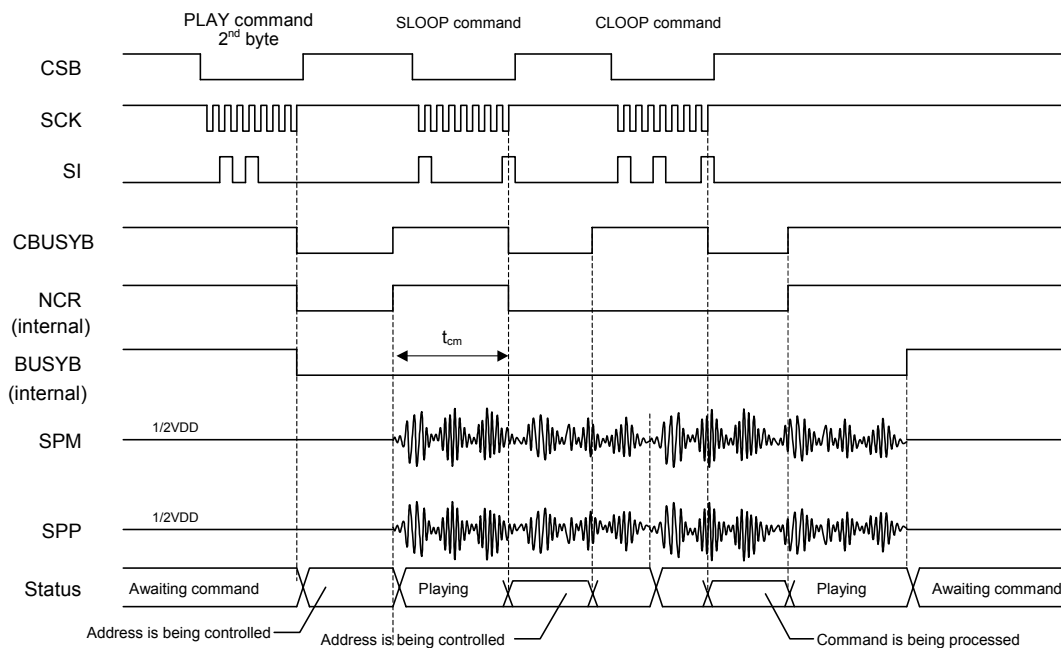
Effective Range of SLOOP Command Input

After the PLAY command is input, input the SLOOP command within 10 ms (t_{cm}) after NCR goes "H".　This will enable the SLOOP command, so that repeat playback will be carried out.

OKI Semiconductor   **ML22420/ML22460**

11. CLOOP command

· command

1	0	0	1	CH3	CH2	CH1	CH0

The CLOOP command releases repeat playback mode.   The command can be input for each channel.   Setting any bit(s) from CH0 to CH3 to "1" releases repeat playback on the corresponding channel(s).   When repeat playback mode is released, the NCR signal goes "H".
It is possible to input the CLOOP command regardless of the status of the NCR signal during playback, but a prescribed command interval needs taking.

OKI Semiconductor   **ML22420/ML22460**

12. CVOL command

· command

1	0	1	0	CH3	CH2	CH1	CH0	1st byte
0	0	0	CV4	CV 3	CV 2	CV 1	CV 0	2nd byte

The CVOL command is a 2-byte command.   It is used to adjust the playback volume.   It is possible to input the VOL command regardless of the status of the NCR signal.   Note that the CVOL command will be ignored if entered during power down or during a transition to a power-up or power-down state.
The CVOL command can be set for each channel.   The CVOL command allows simultaneous specification of multiple channels.   Setting any bit(s) from CH0 to CH3 to "1" sets the playback volume on the corresponding channel(s).
The command enables 32-level adjustment of volume, as shown in the table below.   The initial value after reset release is set to 0 dB.   Upon reset release or during power-up, the value set by the VOL command is initialized.

CV	CV	CV	CV	CV	Volume
0	0	0	0	0	0 dB (initial value)
0	0	0	0	1	−0.28
0	0	0	1	0	−0.58
0	0	0	1	1	−0.88
0	0	1	0	0	−1.20
0	0	1	0	1	−1.53
0	0	1	1	0	−1.87
0	0	1	1	1	−2.22
0	1	0	0	0	−2.59
0	1	0	0	1	−2.98
0	1	0	1	0	−3.38
0	1	0	1	1	−3.81
0	1	1	0	0	−4.25
0	1	1	0	1	−4.72
0	1	1	1	0	−5.22
0	1	1	1	1	−5.74
1	0	0	0	0	−6.31
1	0	0	0	1	−6.90
1	0	0	1	0	−7.55
1	0	0	1	1	−8.24
1	0	1	0	0	−9.00
1	0	1	0	1	−9.83
1	0	1	1	0	−10.74
1	0	1	1	1	−11.77
1	1	0	0	0	−12.93
1	1	0	0	1	−14.26
1	1	0	1	0	−15.85
1	1	0	1	1	−17.79
1	1	1	0	0	−20.28
1	1	1	0	1	−23.81
1	1	1	1	0	−29.83
1	1	1	1	1	OFF

13. AVOL command

· command	0	0	0	0	1	0	0	0	1st byte
	0	0	AV5	AV4	AV3	AV2	AV1	AV0	2nd byte

The AVOL command is a 2-byte command. It is used to adjust the volume of the built-in amplifier. It is possible to input the AVOL command regardless of the status of the NCR signal. This command will be ignored if entered during power down or during a transition to a power-up or power-down state.

The command enables 49-level adjustment of volume, as shown in the table below. The initial value after reset release is set to 0 dB. Upon reset release or during power-up, the value set by the VOL command is initialized.

AV5–0	Volume (dB)	AV5–0	Volume (dB)
3F	+16.0	1F	−4.0
3E	+15.5	1E	−5.0
3D	+15.0	1D	−6.0
3C	+14.5	1C	−7.0
3B	+14.0	1B	−8.0
3A	+13.5	1A	−9.0
39	+13.0	19	−10.0
38	+12.5	18	−12.0
37	+12.0	17	−14.0
36	+11.5	16	−16.0
35	+11.0	15	−18.0
34	+10.5	14	−20.0
33	+10.0	11	−22.0
32	+9.5	12	−24.0
31	+9.0	11	−26.0
30	+8.5	10	−28.0
2F	+8.0	0F	−30.0
2E	+7.5	0E	OFF
2D	+7.0	0D	OFF
2C	+6.5	0C	OFF
2B	+6.0	0B	OFF
2A	+5.5	0A	OFF
29	+5.0	09	OFF
28	+4.5	08	OFF
27	+4.0	07	OFF
26	+3.0	06	OFF
25	+2.0	05	OFF
24	+1.0	04	OFF
23	0.0 (initial value)	03	OFF
22	−1.0	00	OFF
21	−2.0	01	OFF
20	−3.0	00	OFF

Handling of the SG Pin

The SG pin is the signal ground pin for the built-in speaker amplifier.   Connect a capacitor between this pin and the analog ground so that this pin will not carry noise.
The recommended capacitance value is shown below; however, it is recommended that the user determine the capacitance value after evaluation.
Always start playback after each output voltage is stabilized.

Pin	Recommended capacitance value	Remarks
SG	1.0 μF ±20%	The larger the connection capacitance, the longer the speaker amplifier output pin (SPM and SPP) voltage stabilization time.

Handling of the V$_{DDL}$ Pin

The V$_{DDL}$ pin is the power supply pin for the internal circuits.   Connect a capacitor between this pin and the ground in order to prevent noise generation and power fluctuation.
The recommended capacitance value is shown below; however, it is recommended that the user determine the capacitance value after evaluation.
Always start the next operation after each output voltage is stabilized.

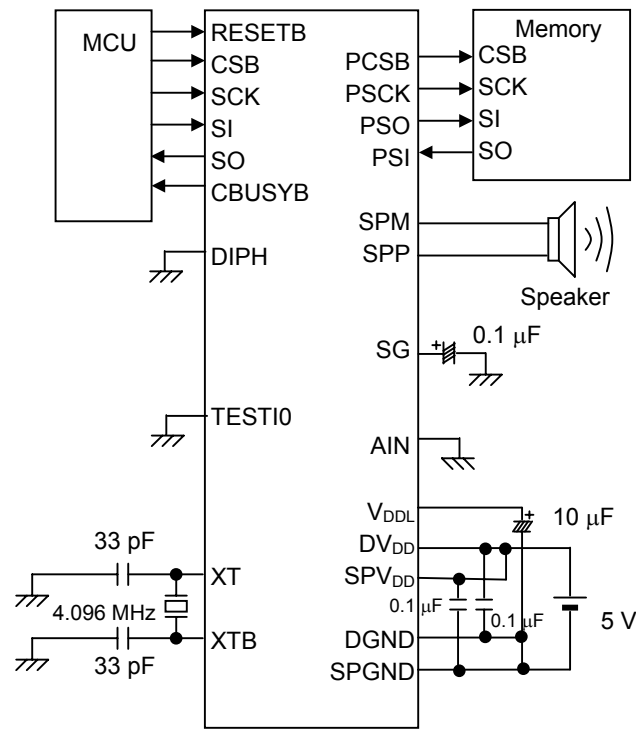| Pin	Recommended capacitance value	Remarks
V$_{DDL}$	1.0 μF ±20%	The larger the connection capacitance, the longer the stabilization time of each output voltage.

Power Supply Wiring

The power supplies of this LSI are divided into the following two:
- Digital power supply (DV_{DD})
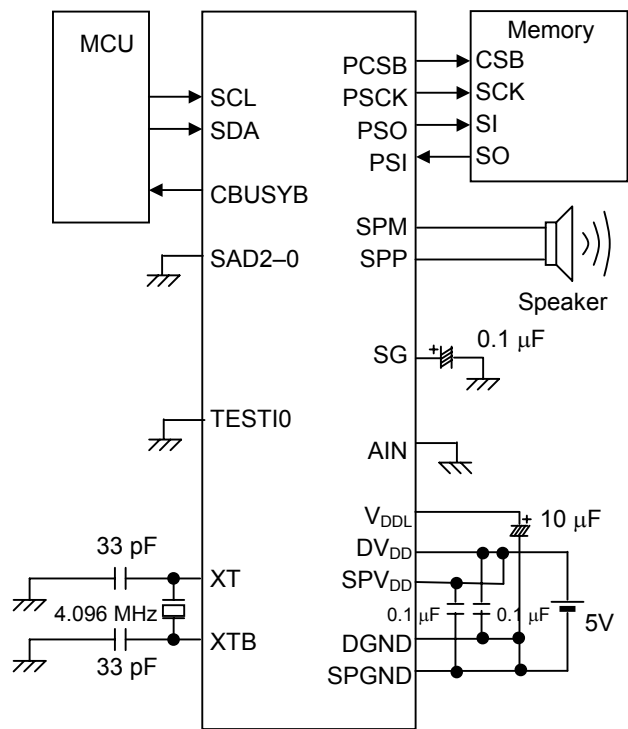- Speaker amplifier power supply (SPV_{DD})

As shown in the figure below, supply DV_{DD} and SPV_{DD} from the same power supply, and separate them into analog and digital power supplies in the wiring.
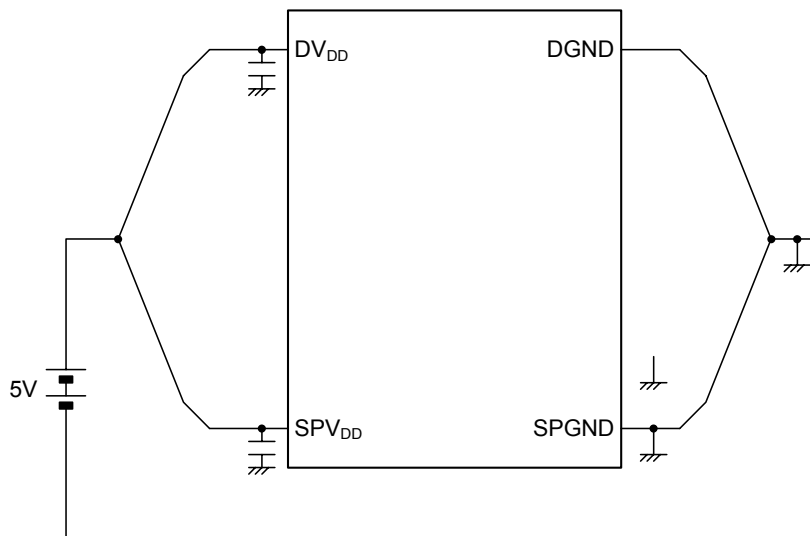
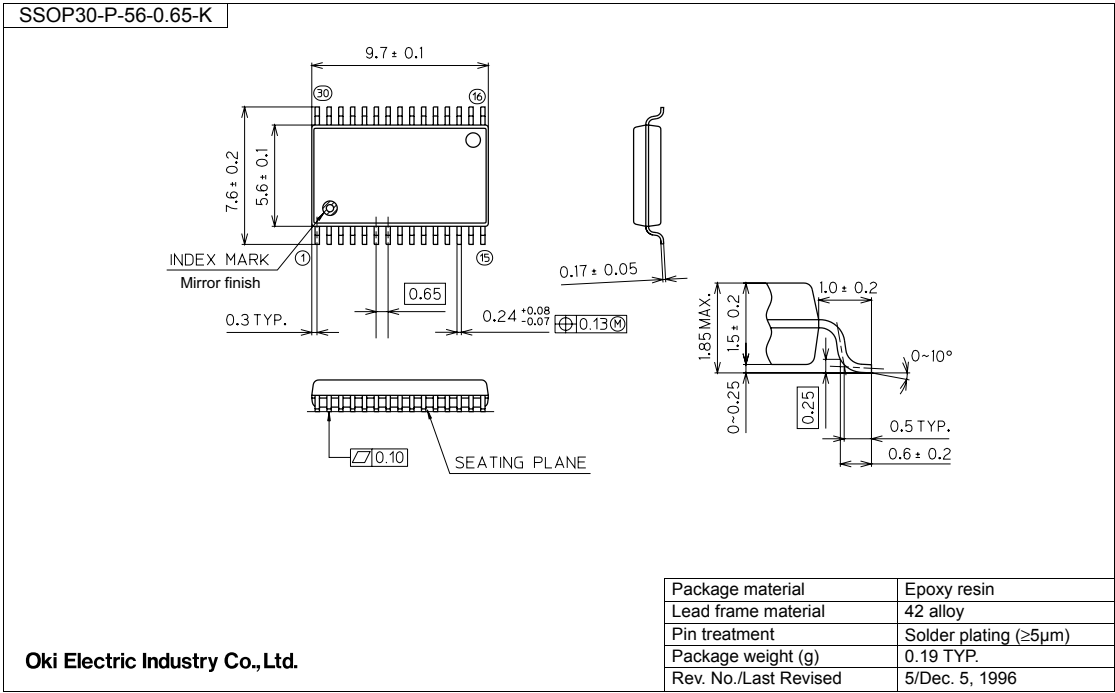**APPLICATION CIRCUIT (DV$_{DD}$ = SPV$_{DD}$ = 5V, ML22420)**

APPLICATION CIRCUIT (DV$_{DD}$ = SPV$_{DD}$ = 5V, ML22460)

OKI Semiconductor **ML22420/ML22460**

PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact OKI's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

OKI Semiconductor **ML22420/ML22460**

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL22420FULL-01	Nov. 30, 2007	–	–	Preliminary edition 1

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. OKI assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not, unless specifically authorized by OKI, authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.