Features

- I2C-bus to 16 bit GPIO expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - 3.0 μA (typical at 5 V VDD)
  - 1.5 μA (typical at 3.3 V VDD)
- 400 kHz Fast-mode I2C-bus
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output (INT)
- Configurable Slave Address with 3 Address Pins
- Internal power-on reset
- Power-up with all channels configured as inputs with weak pull-up resistors
- Latch-Up performance exceeds 200 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model
  - 1500-V Charged-Device Model

Applications

- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers

Description

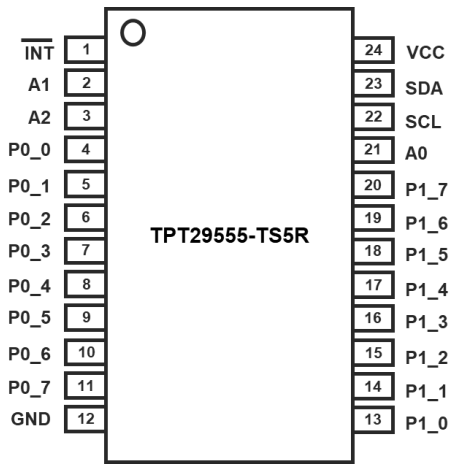
The TPT29555 is a 16-bit GPIO expander with interrupt and weak pull-up resistors for I2C-bus applications. The power supplier voltage range is 1.65 V to 5.5 V and allows the TPT29555 to interconnect with 1.8V microcontrollers.

The TPT29555 contains the register set of four pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers. The open-drain interrupt (INT) output is changeable when any input state changes from its related register state and is used to indicate to the system master that an input state has changed. INT can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I2C-bus. Thus, the TPT29555 can remain a simple slave device. The power-on reset sets the registers to their default values and initializes the device state machine

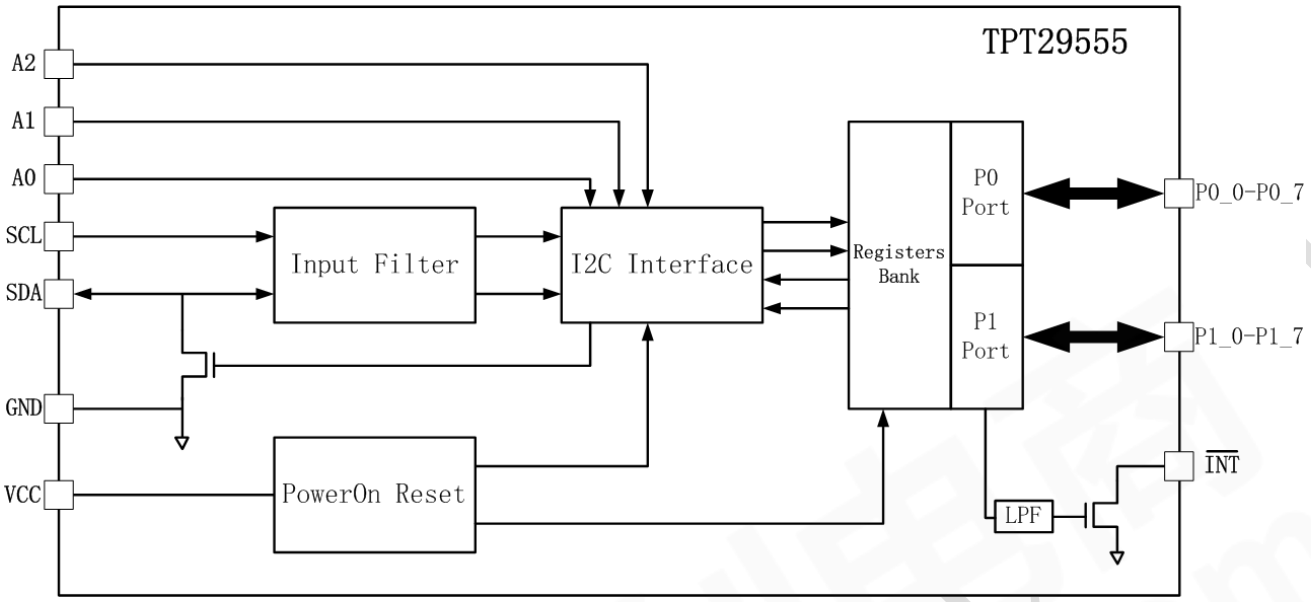
All input/output pins have internal weak pull-up resistors to remove external components. Three hardware pins (A0, A1, A2) select the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus.

TPT29555 is available in TSSOP24 and QFN24 package, and is characterized from –40°C to +85°C.

Function block



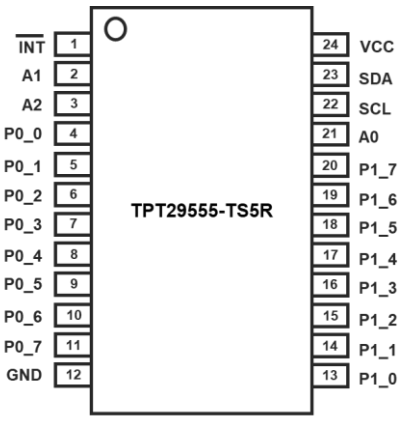
Function block or application schematic

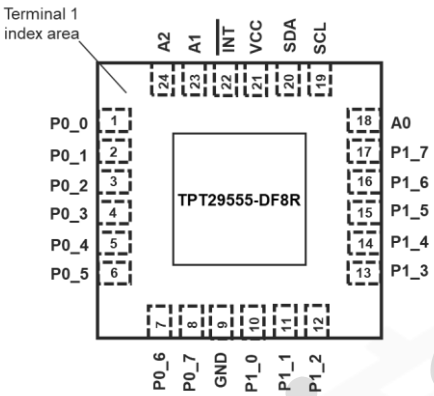


Revision History

Date	Revision	Notes
2020/6/12	Rev. Pre 0.0	Initial Version

Pin Configuration and Functions





TPT29555-TS5R Pin Functions

Pin		I/O	Description
A0	21	Input	Address input 0. Connect directly to V_{CC} or ground
A1	2	Input	Address input 1. Connect directly to V_{CC} or ground
A2	3	Input	Address input 2. Connect directly to V_{CC} or ground
GND	12	GND	Ground
INT	1	Output	Interrupt output. Connect to V_{CC} through a pull-up resistor
P00	4	I/O	P-port I/O. Push-pull design structure. At power on, P00 is configured as an input
P01	5	I/O	P-port I/O. Push-pull design structure. At power on, P01 is configured as an input
P02	6	I/O	P-port I/O. Push-pull design structure. At power on, P02 is configured as an input
P03	7	I/O	P-port I/O. Push-pull design structure. At power on, P03 is configured as an input
P04	8	I/O	P-port I/O. Push-pull design structure. At power on, P04 is configured as an input
P05	9	I/O	P-port I/O. Push-pull design structure. At power on, P05 is configured as an input
P06	10	I/O	P-port I/O. Push-pull design structure. At power on, P06 is configured as an input
P07	11	I/O	P-port I/O. Push-pull design structure. At power on, P07 is configured as an input
P10	13	I/O	P-port I/O. Push-pull design structure. At power on, P10 is configured as an input
P11	14	I/O	P-port I/O. Push-pull design structure. At power on, P11 is configured as an input
P12	15	I/O	P-port I/O. Push-pull design structure. At power on, P12 is configured as an input
P13	16	I/O	P-port I/O. Push-pull design structure. At power on, P13 is configured as an input
P14	17	I/O	P-port I/O. Push-pull design structure. At power on, P14 is configured as an input
P15	18	I/O	P-port I/O. Push-pull design structure. At power on, P15 is configured as an input
P16	19	I/O	P-port I/O. Push-pull design structure. At power on, P16 is configured as an input
P17	20	I/O	P-port I/O. Push-pull design structure. At power on, P17 is configured as an input
SCL	22	Input	Serial clock bus. Connect to V_{CC} through a pull-up resistor
SDA	23	Input	Serial data bus. Connect to V_{CC} through a pull-up resistor
Vcc	24	Supply	Supply voltage

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity
TPT29555-TS5R	-40 to 85°C	24-Pin TSSOP	T29555	MSL3	4,000
TPT29555-QF8R	-40 to 85°C	24-Pin QFN	29555	MSL3	3,000

Absolute Maximum Ratings*

Table 1.

Parameters		Condition	Min	Max	Unit
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage		–0.5	6	V
V_O	Output voltage		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
IIOK	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
T_J	Maximum Junction Temperature			150	°C
T_A	Operating Temperature Range		–45	85	°C
Tstg	Storage temperature		–65	150	°C

*** Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(1) This data was taken with the JEDEC low effective thermal conductivity test board.
(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Table 2.

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV

Thermal Information

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP24	110	60	°C/W
QFN4X4-24L	50	65	°C/W

Recommended Operating Conditions

Symbol	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	SCL, SDA	SCL, SDA	0.7 × V_{CC}	V_{CC}(1)	V
	A2–A0, P07–P00, P17–P10	A2–A0, P07–P00, P17–P10	0.7 × V_{CC}	5.5	V
V_{IL}	SCL, SDA	SCL, SDA	–0.5	0.3 × V_{CC}	mA
	A2–A0, P07–P00, P17–P10	A2–A0, P07–P00, P17–P10	–0.5	0.3 × V_{CC}	mA
I_{OH}	P07–P00, P17–P10	P07–P00, P17–P10		–10	mA
IOL	P07–P00, P17–P10	P07–P00, P17–P10		25	mA
	$\overline{INT}$, SDA			6	mA

Electrical Characteristics-Video Filter Part

All test condition is VDD = 1.65V~5.5V, TA = -40 ~ +85°C, unless otherwise noted.

Table 4.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input Electrical Specifications						
VIK	input clamping voltage	I_I = -18 mA	-1.2	-	-	V
VPOR	power-on reset voltage	V_I = V_{DD} or V_{SS}; I_O = 0 mA	-	1.2	1.4	V
IOL	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 1.65 V to 5.5 V				
		SDA	3	-	-	mA
		INT	3		-	mA
		P port				
		V_{OL} = 0.5 V; V_{DD} = 1.65 V	8		-	mA
		V_{OL} = 0.7 V; V_{DD} = 1.65 V	10		-	mA
		V_{OL} = 0.5 V; V_{DD} = 2.3 V	12		-	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V	15		-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	20		-	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V	20		-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	30		-	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V	30		-	mA
VOH	HIGH-level output voltage	P port				
		I_{OH} = -8 mA; V_{DD} = 1.65 V	1.3	-	-	V
		I_{OH} = -10 mA; V_{DD} = 1.65 V	1.25	-	-	V
		I_{OH} = -8 mA; V_{DD} = 2.3 V	2.0	-	-	V
		I_{OH} = -10 mA; V_{DD} = 2.3 V	1.95	-	-	V
		I_{OH} = -8 mA; V_{DD} = 3.0 V	2.8	-	-	V
		I_{OH} = -10 mA; V_{DD} = 3.0 V	2.75	-	-	V
		I_{OH} = -8 mA; V_{DD} = 4.5 V	4.3	-	-	V
		I_{OH} = -10 mA; V_{DD} = 4.5 V	4.25	-	-	V
VOL	LOW-level output voltage	P port; I_{OL} = 8 mA				
		V_{DD} = 1.65 V	-	-	0.35	V
		V_{DD} = 2.3 V	-	-	0.3	V
		V_{DD} = 3.0 V	-	-	0.25	V
		V_{DD} = 4.5 V	-	-	0.2	V
I_I	input current	V_{DD} = 1.65 V to 5.5 V				
		SCL, SDA, RESET; V_I = V_{DD} or V_{SS}	-	-	-1	uA
		A0, A1, A2; V_I = V_{DD} or V_{SS}	-	-	-1	uA
IIH	HIGH-level input current	P port; V_I = V_{DD}; V_{DD} = 1.65 V to 5.5 V	-	-	1	uA
IIL	LOW-level input current	P port; V_I = V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	-100	uA
IDD	supply current	SDA, P port, A0, A1, A2; V_I on SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz				

		V_{DD} = 3.6 V to 5.5 V	-		25	uA
		V_{DD} = 2.3 V to 3.6 V	-		15	uA
		V_{DD} = 1.65 V to 2.3 V	-		9	uA
		SCL, SDA, P port, A0, A1, A2; V_I on SCL, SDA = V_{DD} or V_{SS}; V_I on P port and A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 0 kHz				
		V_{DD} = 3.6 V to 5.5 V	-	3	7	uA
		V_{DD} = 2.3 V to 3.6 V	-	2	3.2	uA
		V_{DD} = 1.65 V to 2.3 V	-	1	1.7	uA
		Active mode; P port, A0, A1, A2; V_I on P port, A0, A1, A2 = V_{DD}; I_O = 0 mA; I/O = inputs; f_{SCL} = 400 kHz, continuous register read				
		V_{DD} = 3.6 V to 5.5 V	-	60	125	uA
		V_{DD} = 2.3 V to 3.6 V	-	40	75	uA
		V_{DD} = 1.65 V to 2.3 V	-	20	45	uA
		with pull-ups enabled; P port, A0, A1, A2; V_I on SCL and SDA = V_{DD} or V_{SS}; V_I on P port = V_{SS}; V_I on A0, A1, A2 = V_{DD} or V_{SS}; I_O = 0 mA; I/O = inputs with pull-up enabled; f_{SCL} = 0 kHz				
		V_{DD} = 1.65 V to 5.5 V	-	1.1	1.5	mA
⊿IDD	additional quiescent supply current	SCL, SDA; one input at V_{DD} -0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	25	uA
		P port, A0, A1, A2; one input at V_{DD} -0.6 V, other inputs at V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	-	80	uA
C_i	input capacitance	V_I = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	6	7	pF
Cio	input/output capacitance	$V_{I/O}$ = V_{DD} or V_{SS}; V_D = 1.65 V to 5.5 V	-	7	8	pF
		$V_{I/O}$ = V_{DD} or V_{SS}; V_{DD} = 1.65 V to 5.5 V	-	7.5	8.5	pF

Typical performance characteristics

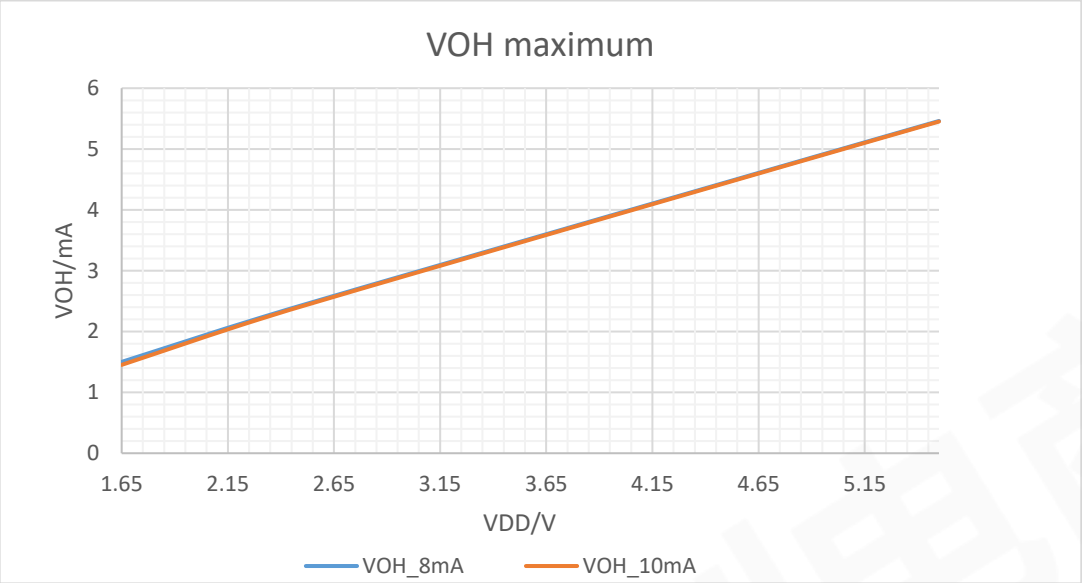


Figure 2. Voh maximum measurement

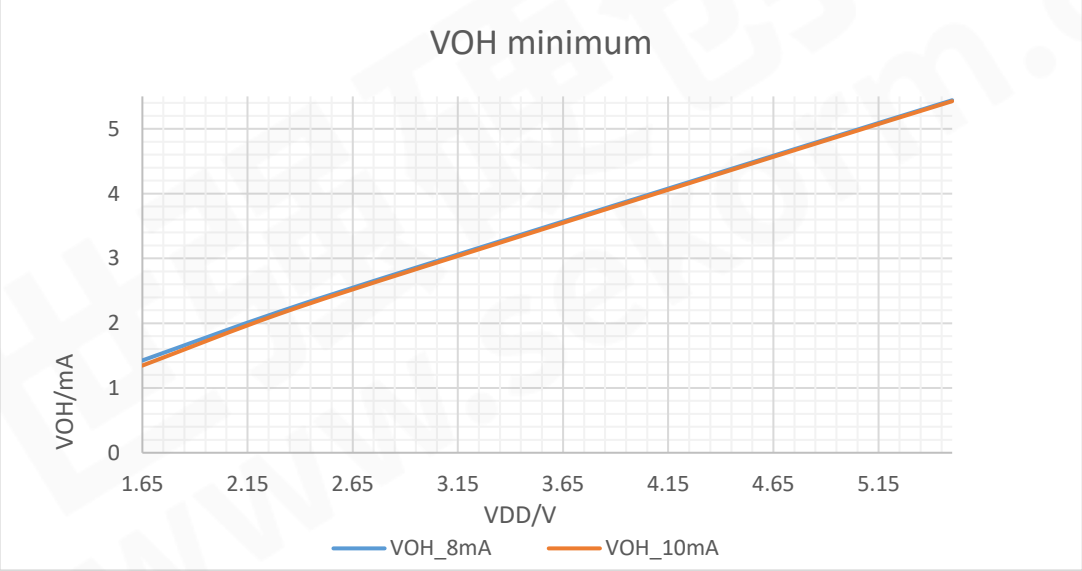


Figure 3. Voh minimum measurement

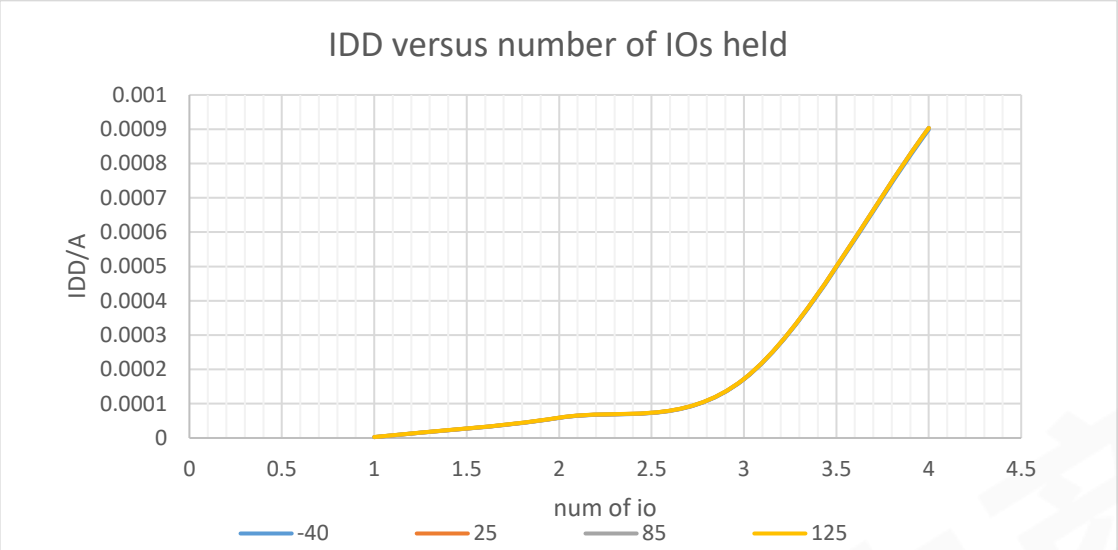


Figure 4.IDD versus number of IOS measurement

Parameter measurement waveforms:

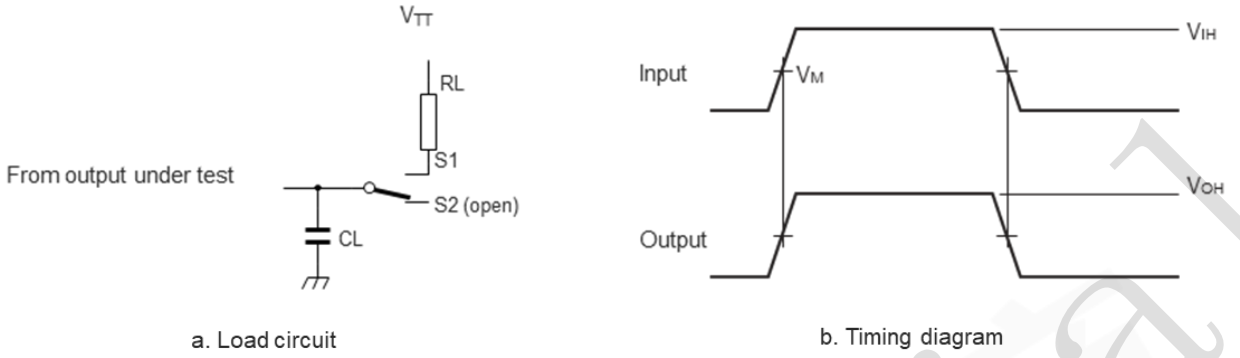
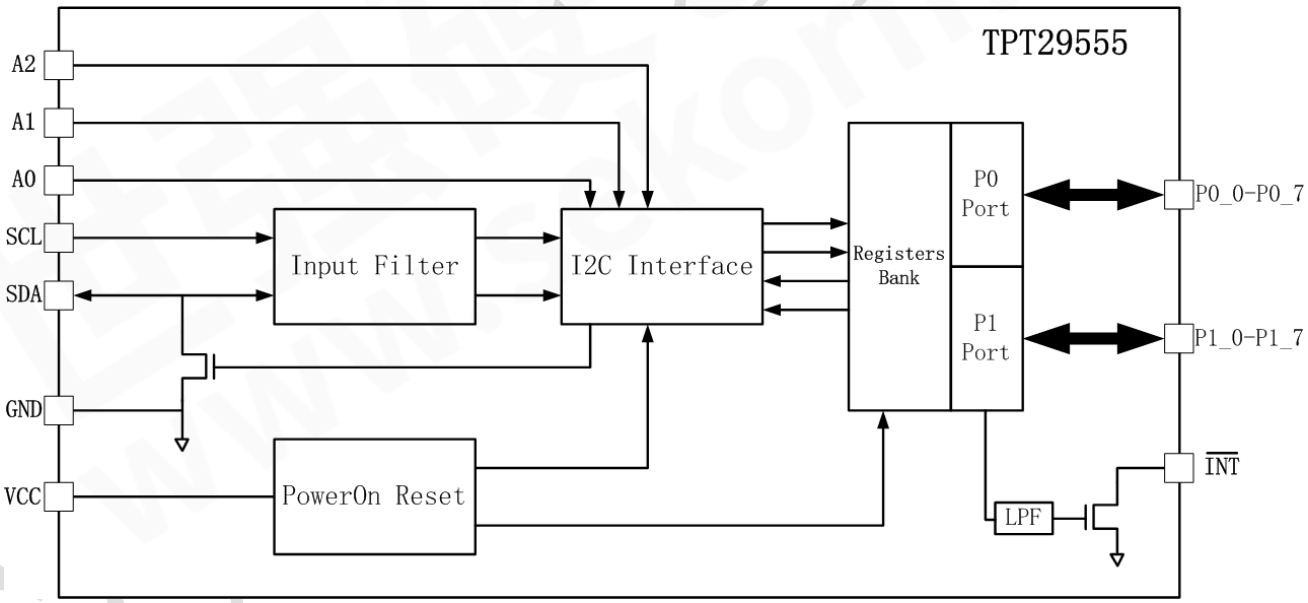


Figure 10. Load circuit for outputs

Function Block diagram:



Application information

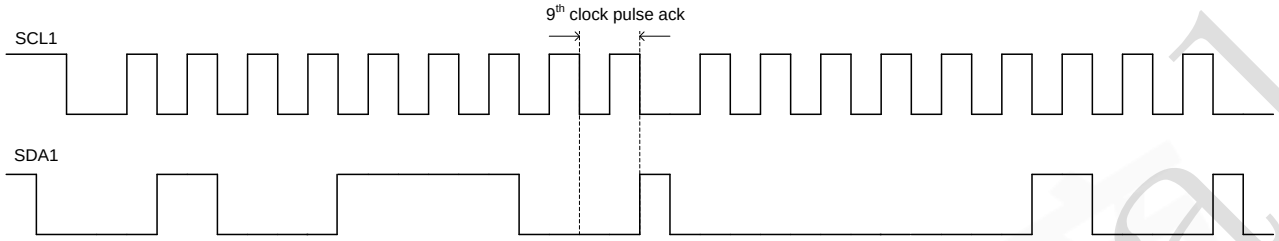
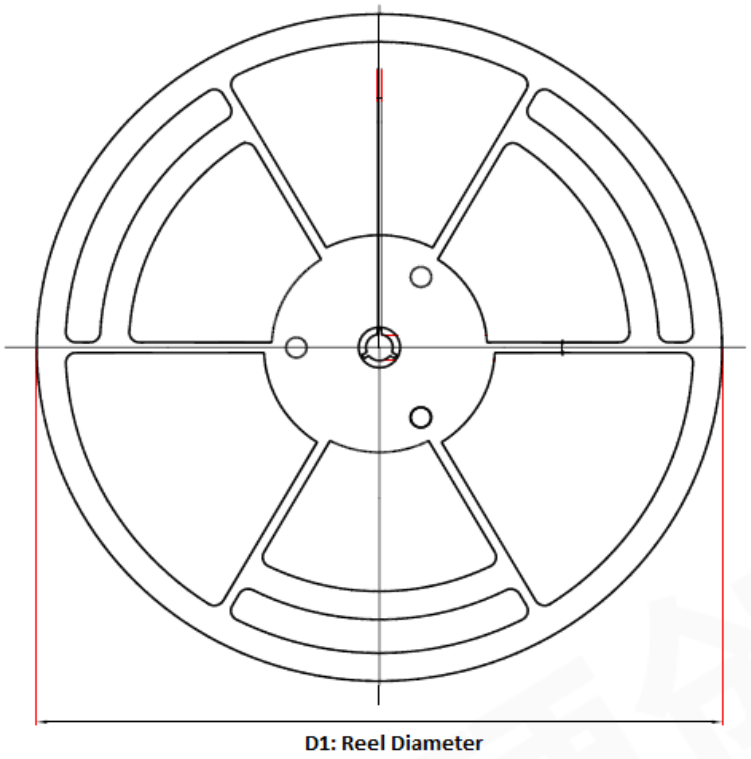


Figure 11. I2C BUS（1.65V~5.5V) waveform

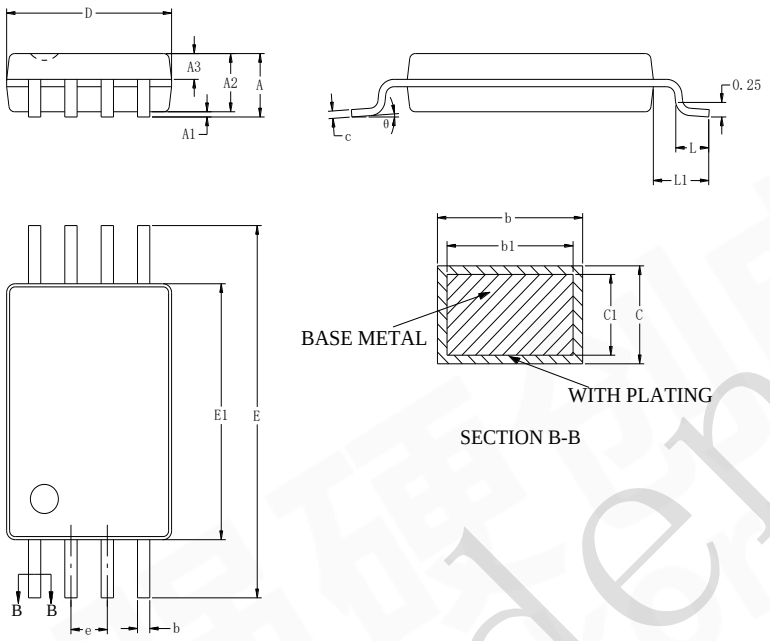
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPT29555-TS5R	24-Pin TSSOP								

Package Outline Dimensions

TS5R (TSSOP24)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	2.90	3.00	3.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°