2.5GBPS Post Amplifier and 1.25GBPS LD Driver with MCU

GENERAL DESCRIPTION

CS6721 integrates three main functions in a single chip providing optimal solutions for various fiber module applications. The functional blocks include a 2.5G post-amplifier, a 1.25G burst or continuous mode LD driver, and an 8-bit MCU for configuring and controlling the module functions.

The post-amplifier receives AC coupled differential signal from pre-amplifier and performs the quantization amplifications. There are total four amplification stages excluding the output stage. The offset cancellation is built-in on chip. The LOS status is also configurable as a set peak level detection by the post-amplifier or combined with ADC detection on peak level.

The LD driver performs the transmit function that receives the PECL differential signal TXINP/TXINN and convert to drive LD output driver. The LD driver is also controlled by burst-enable signal BENN/BENP. The polarity of control can be configured. The laser driver includes differential modulation outputs and DC bias control output. The setting of output power level is controlled through automatic power control loop and is configurable by MCU. The output can be connected to Laser diode either by AC or DC coupled. The transmit path can be enabled or disabled by TXEN signal.

The on-chip MCU is the flexibility and versatility of controlling and configurations of fiber module design. Almost all configurations and parameters of the PA and LD driver parameters and can be controlled by MCU through software. The 12-bit ADC associated with MCU can be used to acquire various internal and external analog signals such on-chip temperature sensor and reference voltages. The MCU has 2K boot ROM and 2K SRAM for program storage which can meet the need of application of SFP/PON, Also the boot ROM is responsible for uploads the user program from external serial EEPROM(with capacity of 2k 4k 8k), The I^2C slave interface also serves as ISP/IAP interface as well as SFP/SFF DMI function.

CS6721 integrates essential building blocks for Fiber module design. The integration of MCU allows precision control to tailor various module applications and facilitates configuration and automatic calibration in the manufacturing process. Using CS6721, the module can achieve low cost and high performance and can be applied in FTTH, BPON, GEPON, and GPON.

APPLICATIONS

- SONET/SDH, FTTH, GEPON, GPON

FEATURES

Post Amplifier

- 1.25GBPS – 2.5GBPS
- -3dB bandwidth 50KHz – 2GHz
- 2mV sensitivity
- On-chip offset cancellation
- Programmable signal detect level and hysteresis
- Programmable LOS function and Power detection
  - SD control
  - Peak/ADC control
  - External Monitor/ADC control
- Programmable power down
- CML output

LD Driver

- Programmable bias current (up to 100mA)
- Programmable modulation current (up to 80mA)
- Digital automatic power control loop
  - Fast acquisition of laser power < 3 bursts
  - Programmable loop time constant
  - Update only at burst-off state
  - Loop monitoring by MCU
- Rise/Fall time < 200psec
- Burst or continuous mode compatible
- Programmable polarity and FAIL status
  - DCBIAS fail
  - MPD fail
  - APC fail
- Programmable power down and TX enable/disable function
- Laser power monitor and burst-on monitor

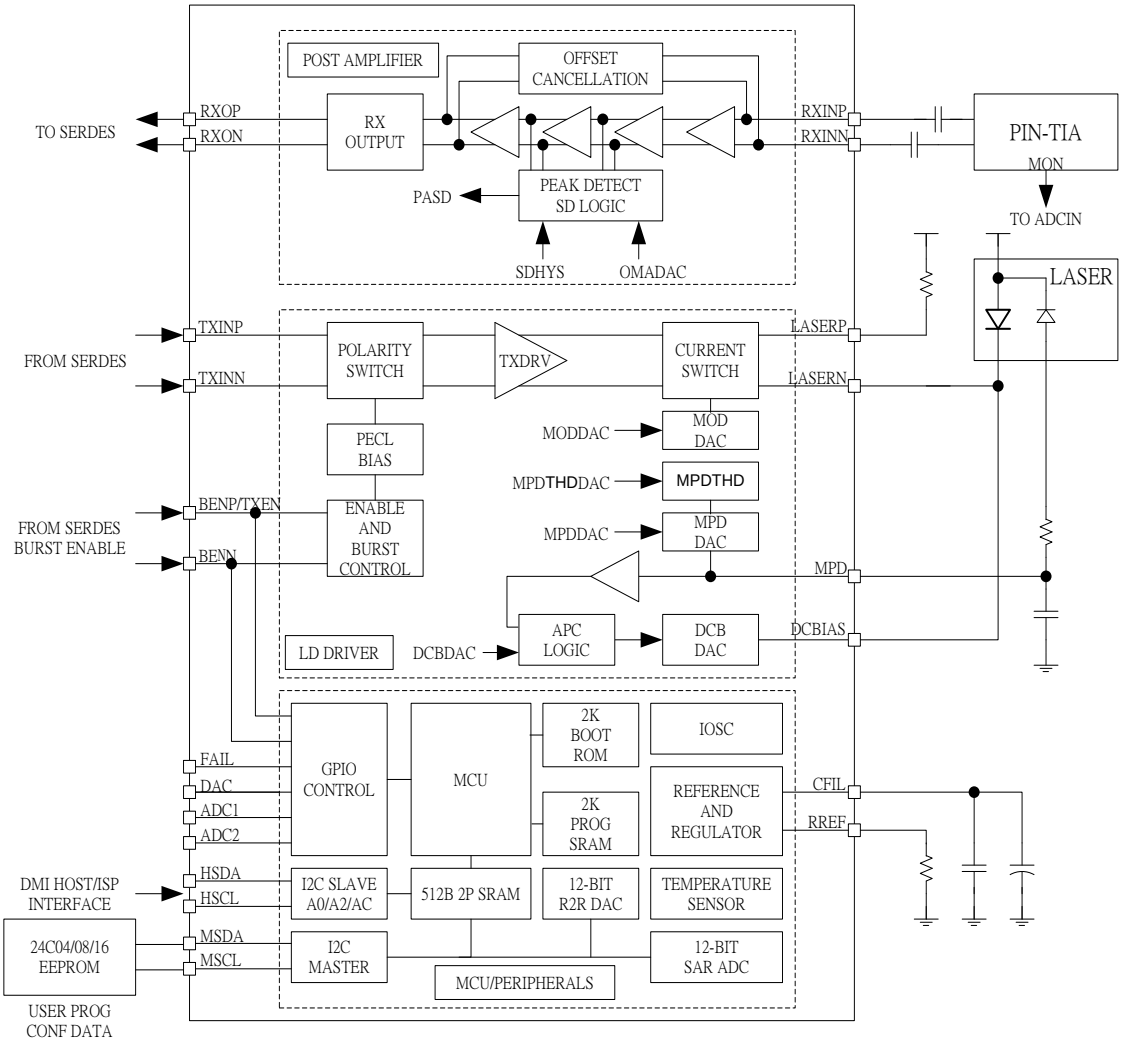
Micro Controller (MCU)

- RISC CPU – 12.5MHz
  - 2K Program ROM for Boot
  - 2K Program SRAM for user program
  - Watchdog timer
  - Low voltage reset
- I^2C master for EEPROM program upload and data storage
- I^2C slave for host ISP/IAP and DMI
  - Two level password protection for A0/A2 access
  - Support software TX_DISABLE
  - Burst Counter
  - A0/A2 or B0/B2 configurable
- 8-Channel 12-bit ADC
- 10-bit R2R DAC
- On-chip temperature sensor

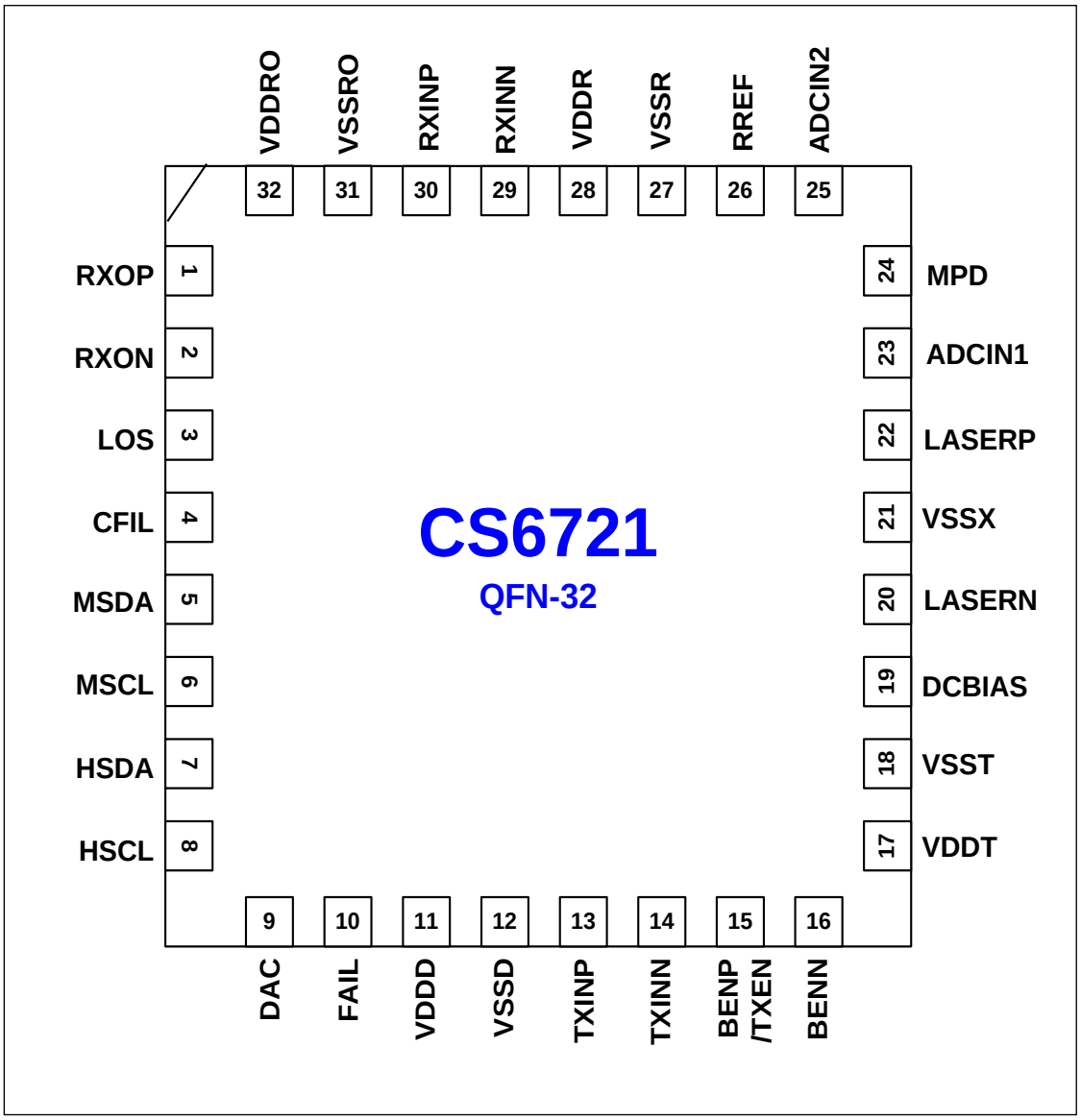
General

- Low power consumption (300mW)
- Single 3.3V supply with on-chip regulator
- Extended temperature range -40°C ~ +85°C
- RoHS compliance package

BLOCK DIAGRAM



PIN CONNECTION DIAGRAM



PIN DESCRIPTION

NAME	PIN #	TYPE	DESCRIPTION
RXOP	1	A, OUT	Post Amplifier Positive Data Output. This is a CML output.
RXON	2	A, OUT	Post Amplifier Negative Data Output. This is a CML output.
LOS	3	AD, IO	Loss of Signal. This pin can be configured in CMOS, OD, or PECL output. It can also can be configured as an GPIO pin to the MCU.
CFIL	4	P	Internal 1.8V regulator output. The regulator supplies internal analog circuits and digital core logic. A good decoupling should be connected from this pin to VSS, typically 0.1uF in parallel with 10uF.
MSDA	5	D, OD, IO	Master Serial Interface Data. This pin is connected to the data signal of external 24C32 EEPROM for application program and calibration data. It is an open-drain I/O and an external pull-up resistor is required.
MSCL	6	D, O, IO	Master Serial Interface Clock. This pin is connected to the clock signal of external 24C32 EEPROM for application program and calibration data. This is output only. This pin is also used to configure whether Slave I^2C address as A0/A2/AC or B0/B2/BC. If an external pull-up resistor is present, the Slave I^2C is configured as A0/A2/AC. If an external pull-down resistor is present, the slave I^2C slave is configured as B0/B2/BC. The evaluation of A0/A2/AC and B0/B2/BC is done at the end of power-on reset.
HSDA	7	D, OD, IO	Host Serial Interface Data. This pin is connected to host data line for performing DMI as well calibration and in system programming. It is an open-drain I/O and an external pull-up resistor is required.
HSCL	8	D, OD, IO	Host Serial Interface Clock. This pin is connected to host data line for performing DMI as well calibration and in system programming. It is an open-drain I/O and an external pull-up resistor is required.
DAC	9	AD, IO	DAC Output. This pin is connected to the on-chip R2R DAC output. The DAC has high source impedance. This pin can also be configured as a GPIO pin to the MCU and used for enable/disable control.
FAIL	10	D, IO	FAIL Status Output. This pin is connected to the hardware fail status. This pin can also be configured as a GPIO pin to the MCU.
VDDD	11	P	Digital Circuit Supply 3.3V. This pin should be connected to external 3.3V supply with good decoupling to VSSD.
VSSD	12	G	Digital Circuit Ground 0V. This pin connects to internal digital circuit ground and should have good decoupling to VDDD.
TXINP	13	A, I	Transmit Data Positive. This is positive of differential transmit data signals. This pin is internally biased to PECL level through 10K resistor.
TXINN	14	A, I	Transmit Data Negative. This is negative of differential transmit data signals. This pin is internally biased to PECL level through 10K resistor.
BENP	15	AD, I	Burst Enable Positive. This pin is burst-enable control and can be in single-ended PECL or CMOS level, or as differential PECL mode with BENN pin. In PECL mode, the pin is internally biased to PECL level through a 10K resistor. This pin can also be configured as a GPI pin to the MCU and used for transmit enable/disable control or other digital input.
BENN	16	AD, I	Burst Enable Negative. This pin is burst-enable control and can be in single-ended PECL or CMOS level, or as differential PECL mode with BENP pin. In PECL mode, the pin is internally biased to PECL level through a 10K resistor. This pin can also be configured as a GPO pin to the MCU and can be used for Laser Warning status.
VDDT	17	P	3.3V supply for transmit output driver. Should have good decoupling to

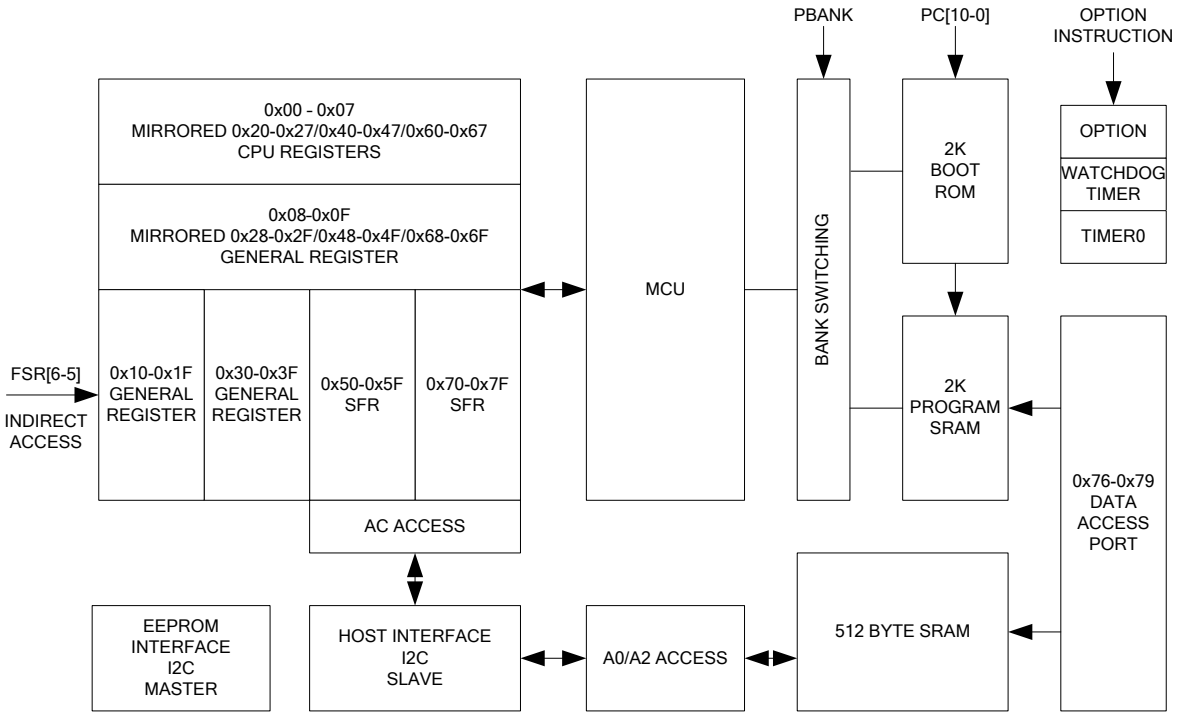
NAME	PIN #	TYPE	DESCRIPTION
			VSST. VDDT is an independent power supply that only supplies to DCB and MOD driver. When VDDT drops below VDDR-1V, the transmit path is automatically disabled.
VSST	18	G	LD DC Bias Driver Circuit Ground 0V. This pin connects to the ground of the Bias current source and should have good decoupling to VDDT.
DCBIAS	19	A, O	LD DC Bias Current Output. This pin sinks a DC bias current for the laser diode. The current sink is controlled by APC loop or can be set by MCU directly. In burst-mode, the current sink is turned-off during burst disable state.
LASERN	20	A, O	LD AC Modulation Current Negative Output. This pin switches modulation current depending on the TXINP and TXINN and the polarity can be controlled. The current is programmable by MCU.
VSSX	21	G	LD AC Modulation Driver Circuit Ground 0V. This pin connects to the ground of the modulation current source and should have good decoupling to VDDT as well supply connecting to laser.
LASERP	22	A, O	LD AC Modulation Current Positive Output. This pin switches modulation current depending on the TXINP and TXINN and the polarity can be controlled. The current is programmable by MCU.
ADCIN1	23	A, IO	ADC Input Channel 1. This pin is connected to internal ADC channel 1. Typically, this pin can be used to connect to an external temperature sensor to determine the module temperature. Under this mode, a programmable sensor DC bias current can be turned-on and connected.
MPD	24	A, I	Power Monitor Diode Input. This pin should connect to the power monitor diode of the laser. An internal programmable current source is connected to this pin for setting the laser power under APC mode.
ADCIN2	25	A, I	ADC Input Channel 2. This pin is connected to internal ADC channel 2.
RREF	26	A, I	Current Reference Setting Resistor. An external precision 10K Ohm resistor should be connected between this pin and VSSR. The resistor should be placed as close as possible to the device.
VSSR	27	G	Analog and Receive Path Circuits Ground 0V. This pin connects to circuit grounds of the reference and receive path. This pin should have good decoupling to VDDR. These are very sensitive circuit and thus should be isolated from transmit supply to avoid board-level crosstalk.
VDDR	28	P	Analog and Receive Path Circuits Supply 3.3V. An external very clean and noise free 3.3V should be connected to this pin. This pin connects to circuit grounds of the reference and receive path. This pin should have good decoupling to VDDR. These are very sensitive circuit and thus should be isolated from transmit supply to avoid board-level crosstalk.
RXINN	29	A, I	Post Amplifier Negative Input. This pin is typically connected to PIN-TIA through AC coupling. This pin is internally biased. The AC coupling capacitor and internally bias resistor (10K) set the 3dB low frequency.
RXINP	30	A, I	Post Amplifier Positive Input. This pin is typically connected to PIN-TIA through AC coupling. This pin is internally biased. The AC coupling capacitor and internally bias resistor (10K) set the 3dB low frequency.
VSSRO	31	G	Receive Output Buffer Ground 0V. This pin connects to circuit grounds of the receive output buffer. This pin should have good decoupling to VDDRO.
VDDRO	32	P	3.3V supply for the receive output buffers. Should have good decoupling to VSSRO

FUNCTIONAL DESCRIPTION

CS6721 combined three main functional blocks: Post Amplifier, Laser Driver, and Micro Controller. This combination allows significant enhancement over conventional design that offers flexibility and cost-saving through application software programming. Using external EEPROM as storage for program and data storage, the application software can designed to precision control of the parameters of the PA and LD driver and compensate for temperature variation and device fluctuations. The following section describes the functions of each block. Extensive descriptions on MCU programming and its SFR (Special Function Register) controlling on-chip peripherals are described in details.

1. MCU and Digital Peripherals

The MCU is an 8-bit CPU with 12-bit wide instructions. The instruction of the CPU is listed in the appendix, and the block diagram is shown below.



1.1 Program Memory and Space

The native addressing space of the MCU is 2K and can be bank-switched between two 2K spaces, one for on-chip ROM, and one for on-chip program SRAM. The MCU will execute the boot ROM after reset as PBANK is cleared to 0 at reset. The on-chip program SRAM is actually a two-port structure, and the content of the program SRAM can be written by CPU through special function registers using data/address port manipulations. The boot-ROM uses this feature to upload application program from the external EEPROM into the program SRAM, and then switches PBANK to 1 turning over the CPU control to application program.

Also, after reset and boot loaded procedure, the program counter is loaded with 0x000. For writing program in assembly language, the program needs to start at 0x000. In C programming, the main program also needs to be located at 0x000.

1.2 Register Map and Definitions

0x00 - 0x07 are CPU registers and are mirrored to 0x20-0x27, 0x40-0x47, and 0x60-0x6F. This space can be accessed using direct or indirect addressing mode.

0x08 - 0x0F are general-purpose data registers and are mirrored to 0x28-0x2F, 0x48-0x4F, and 0x60-0x6F. This space can be accessed using direct or indirect addressing mode.

0x10-0x1F and 0x30-0x3F are also general-purpose data register, and 0x50-0x5F, 0x70-0x7F are special function registers. These spaces are bank-switched by FSR[6-5]. 0x50 to 0x5F are special function registers that control the analog peripherals. 0x70 to 0x7F are special function registers that control on-chip digital peripherals. Both of these two ranges can also be accessed by the Host I^2C slave interface. This allows host to directly control the analog peripherals in the calibration phase and perform in-system-programming of the external EEPROM.

1.3 CPU Registers

INDF (0x00) Index Data Port R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	INDF7	INDF6	INDF5	INDF4	INDF3	INDF2	INDF1	INDF0
WRITE	INDF7	INDF6	INDF5	INDF4	INDF3	INDF2	INDF1	INDF0

INDF is not a physical register. It functions as a data port to read and write data in indirect address mode. The indirect address mode uses FSR[6-0] for register address where FSR[6-5] are used to do bank select.

TMR (0x01) Timer Register R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
WRITE	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0

TMR is an 8-bit up and wrap-over counter. CPU can read and write this location to set or clear the counter. The configurations of the timer, such as pre-scaler, and count/stop are through OPTION register using OPTION instruction. The overflow status of the timer can be obtained from the STATUS register.

PCL (0x02) Program Counter Low Byte R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0
WRITE	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0

PCL register is the low byte of the program counter. Writing to this register will cause the CPU to branch into new location. Also instruction that modifies PCL will cause PC[8] to be cleared to 0. This also includes CALL instruction.

STATUS (0x03)CPU Status Register R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PBANK	PA1	PA0	WON	TON	Z	DC	C
WRITE	PBANK	PA1	PA0	WON	TON	Z	DC	C

PBANK	This bit controls the program memory bank select. This bit is cleared to 0 after reset and selecting the on-chip Boot ROM. This bit is set to 1 to select the on-chip program SRAM.
PA1	This bit reflect the program counter's 11th bit, PC[10]. Writing to this bit will cause the CPU to branch to a new location.
PA0	This bit reflect the program counter's 10th bit, PC[9]. Writing to this bit will cause the CPU to branch to a new location. PA1 and PA2 are used together with GOTO (Unconditional Branch) instruction to perform long jump.
WON	This bit is set and latched by the watchdog timer when WDT time out (overflow) occurred. This bit must be cleared by software.

TON	This bit is set and latched by the 8-bit timer when timer time out (overflow) occurred. This bit must be cleared by software.
Z	This bit reflects the zero status of previous logic or arithmetic operations of CPU.
DC	This bit reflects the digit carry (4^{th} bit carry) status of previous ADDWF, SUBWF arithmetic operations of CPU.
C	This bit reflects the carry status of previous ADDWF, SUBWF, RRF, RLF arithmetic operations of CPU.

FSR (0x04) Indirect Register Access Address Register R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0
WRITE	-	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0

FSR[6-5]	These two bits are bank select bits for register bank.
FSR[4-0]	These bits are used for indirect address pointer for register operation. The data port of the indirect access is INDF.

PORTA, PORTB, PORTC (0x05, 0x06, 0x07) Port A, B, C Register R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	-	-	-	-	-	-	-
WRITE	-	-	-	-	-	-	-	-

In CS6721, PORT A, B, and C are not used. Therefore, these registers can be used as general-purpose data registers. There are also several implicit registers associated with the MCU, W, TRIS, OPTION, and WDT. W is the working register where ALU operand and result are stored. TRIS is the PORT A, PORT B, and PORT C IO configuration control. Since PORT A, B, and C are not used, so TRIS register and TRIS instruction will have no effect.

OPTION register is write-only and only accessible through “OPTION” instruction which transfer W into OPTION register. The OPTION register is defined as following.

OPTION (NA) Option Register W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	-	-	-	-	-	-	-
WRITE	TEN	TPS2	TPS1	TPS0	WEN	WPS2	WPS1	WPS0

TEN	Set this bit to 1 to allow Timer to count. Set this bit to 0 will stop the counting of the Timer. The Timer will remain the current counting value when stopped.
TPS[2-0]	These bits determine the pre-scaling factor of the Timer clock. 000 = SYSCLK 001 = SYSCLK/2 010 = SYSCLK/4 011 = SYSCLK/8 100 = SYSCLK/16 101 = SYSCLK/32 110 = SYSCLK/64 111 = SYSCLK/128
WEN	Set this bit to 1 to allow Watchdog Timer to count. Set this bit to 0 will stop the counting of the Watchdog Timer. WDT is always cleared at the transition from disable to enable state.
WPS[2-0]	These bits determine the pre-scaling factor of the Watchdog Timer clock. 000 = SYSCLK/2 001 = SYSCLK/4 010 = SYSCLK8 011 = SYSCLK/16

100 = SYSCLK/32
101 = SYSCLK/64
110 = SYSCLK/128
111 = SYSCLK/256

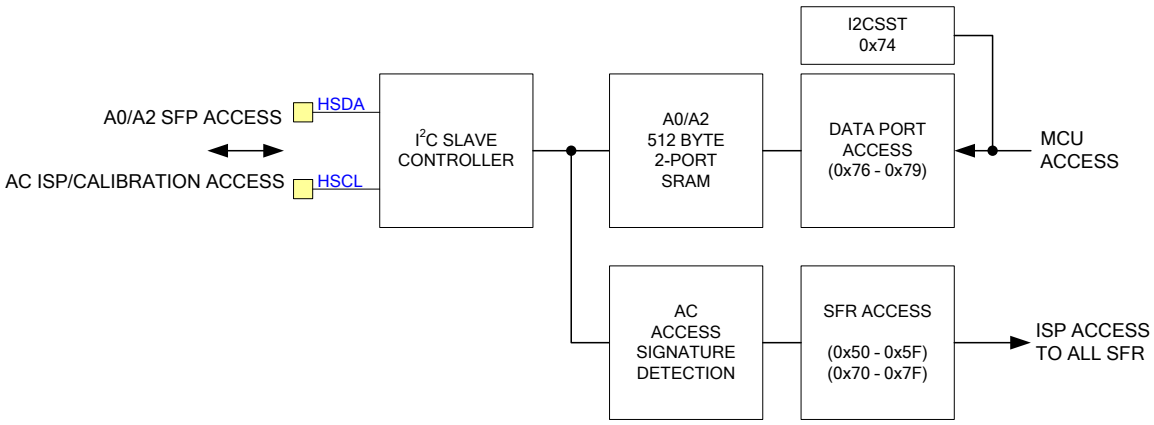
WDT is the Watchdog Timer that can only be cleared using “CLRWDT” instruction. WDT is a 16-bit counter with pre-scaling defined in the OPTION register.

2. System Digital Peripherals and Its Registers

This section describes the system digital peripherals such as I²C slave for host communication and it’s associated SFP 2-port RAM, and I²C master for EEPROM interface, and the access to on-chip 2K program SRAM.

2.1 I²C Slave Controller

The purpose of on-chip I²C Slave has several usages. Its main purpose from fiber equipment view is SFP access to allow DMI information to be passed to host. However, it is also important purpose that I²C slave is used for parameter calibration and in-system-programming during module manufacturing. The I²C slave is implemented in hardware and the following block diagram shows the implementations. The hardware is implemented using synchronous logic thus require system clock to be running. The system clock needs to be higher than 8X higher than the I²C speed. For example, if I²C has maximum of 100K bit/second, then SYSCLK needs to be set higher than 800KHz.



For normal condition after system reset, the I²C slave will respond to only A0 and A2 access requests. These requests will be passed to the on-chip 512-byte 2-port SRAM partitioned into two pages. The contents of the 2-port SRAM is uploaded and updated by the MCU through application software to meet SFP DMI requirements. The write-protection of A0/A2 access is default on which only allow modification by the host in the range of 128 to 147 of A2 page. This write-protection can be turned-off by application program.

MCU access the 2-port SRAM through a data port using RAMADDRH (0x76) and RAMADDRL(0x77) to specify the 2-port SRAM address, and then perform read/write operation through RAMDATAL(0x79) SFR locations.

There is arbitration logic to resolve contention between Host A0/A2 access and MCU access. In the contention, the access from Host has higher priority and MCU is stalled. That means Host will always get the access at higher priority. To ease the programming, I²C slave provide status to indicate host access, and also status to indicate A0/A2 modification. It is upon application program to determine if the modification should be permanent and update the data into the EEPORM.

The I²C Slave also provides a backdoor that Host can perform calibration and in-system-programming for installing application program on a blank external EEPROM. The backdoor is open upon receiving a sequence of

byte write commands to address A0:80. The write data sequence is 0x00 – 0xAA – 0x55 – 0xAC – “A” – “C” – “C” – “E” – “S” – “S”. After the slave completes detection of this exact sequence, the slave will start to respond to address AC. The sequence must be exact and any violation will cause the detection to be restarted. After AC access is turned on, any additional or further I²C host access to address A0:80 will cause the backdoor to be closed again. During the AC access, the host has full control (read and write) of all the Special Function Register while the CPU is put into idle. As the result, in this backdoor access, the host can manipulate ADC and measure the VDD18 or the present temperature sensor reading to establish parameter calibrations. The host can also manipulate the I²C master command and data registers, thus transfer application program and look-up tables to the connected external EEPROM. After these, host can also issue reset command to allow CS6721 to resume normal operations. For rare design requirement, AC access mode can also be used so that an external MCU can control CS6721’s on-chip analog functional blocks, for example, an extremely large application program space is required.

I2CSCS (0x74) I²C Slave Configuration and Status Register RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	I2CSRST	A0HMST	INFILEN	A0LMST	A2HMST	A2LMST	ACST	BUSY
WRITE	I2CSRST	A0HMST	INFILEN	A0LMST	A2HMST	A2LMST	-	-

I2CSRST — Set this bit to 1 will cause the I²C slave controller to reset. Set this bit to 0 for normal operations.

A0HMST — This bit is set by the I²C slave hardware after any of A0 location 0 to 127 was modified by the host. The modification is only valid if the corresponding password is valid. This bit must be cleared by software.

INFILEN — Set this bit to 1 will enable a pulse filter on the SDA input. The filter filters out any pulse less than 50nsec width.

A0LMST — This bit is set by the I²C slave hardware after any of A0 location 128 to 255 was modified by the host. The modification is only valid if the corresponding password is valid. This bit must be cleared by software.

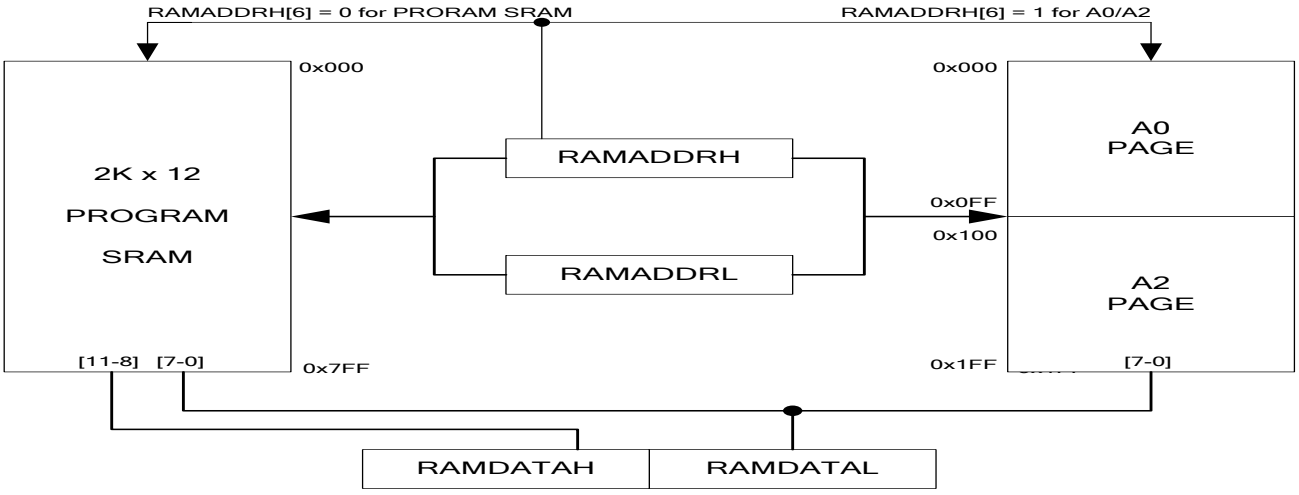
A2HMST — This bit is set by the I²C slave hardware after any of A2 location 128 to 255 was modified by the host. The modification is only valid if the corresponding password is valid. This bit must be cleared by software.

A2LMST — This bit is set by the I²C slave hardware after any of A2 location 0 to 127 was modified by the host. The modification is only valid if the corresponding password is valid. This bit must be cleared by software. Please note A2LMST is not set if the host altered A2(110) bit 6 for controlling TX_DISABLE software control function.

ACST — This bit is read-only and reflects the backdoor status. It is set to 1 by the hardware if AC access mode is on. It is automatically cleared if the backdoor is closed.

BUSY — This bit is read-only and set to 1 by hardware to indicate that host A0/A2 access is on-going, the MCU should wait after it is finished. It is recommended that application first check this bit status before access the A0/A2 2-port SRAM through the data port.

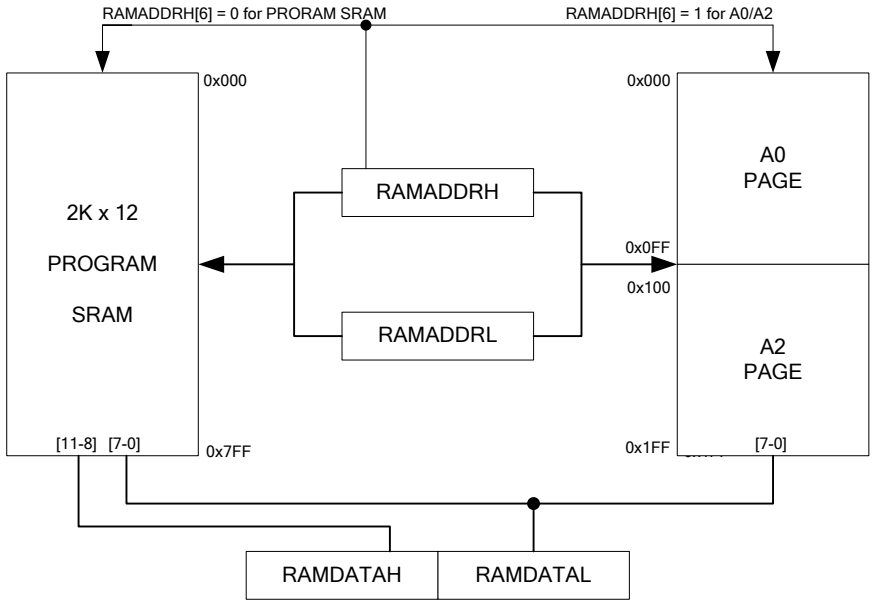
The I²C slave module supports the following transaction modes: single-write, page-write, single-read, and page-read. The formats of these four modes are shown below and the host must follow these formats for access. The byte address in the page mode is automatically incremented for each byte access.



Please note the I2C slave can be configured to respond to A0/A2/AC or B0/B2/BC access. This is useful if two CS6721 are connected in parallel on the slave I²C bus and can be separately accessed by the host. The configuration is determined at the exit of power-on reset and if MSCL pin has external pull-up resistor for A0/A2/AC, and external pull-down resistor for B0/B2/BC.

2.2 DATA Port Access to A0/A2 SRAM and Program SRAM

This section describes the read/write accesses from MCU to the A0/A2 2-port SRAM and to the 2Kx12 Program SRAM. Both accesses share the same address point SFR and data buffer SFR. The block diagram is shown in the following figure.



RAMADDRH (0x76) RAM Address Pointer High Byte RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	RAMEN	A0A2	-	-	PWEN	ADDR10	ADDR9	ADDR8
WRITE	RAMEN	A0A2	-	-	PWEN	ADDR10	ADDR9	ADDR8

RAMEN Set this bit to 1 to allow data port to operations. Set this bit to 0 to disable the access.

A0A2 Set this bit to 1 to direct the operation to the A0/A2 512-byte SRAM. Set this bit to 0 to direct the operation to the 2K x 12 program SRAM.

PWEN	Set this bit to 1 to direct the operation to the PW1(4 bytes), PW2(4 bytes) and PWCONT register address. The address is the RAMADDRL[3:0]. Setting the PW2 password to FFFFh will disable the password protection function. Set this bit to 0 to disable the access.
ADDR[10-8]	Address bit 10, 9, 8 of the pointer. For A0/A2 access, A10 and A9 are ignored.

RAMADDRL (0x77) RAM Address Pointer Low Byte RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
WRITE	ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

This register contains the low byte of the address pointer for the data port operations.

RAMDATAH (0x78) RAM Data Port High Byte RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	-	-	-	DATA11	DATA10	DATA9	DATA8
WRITE	-	-	-	-	DATA11	DATA10	DATA9	DATA8

This is a pseudo register. Operation on this register yields the execution to the SRAM location pointed by the RAM address register. For program SRAM access, only the lower four bits are used. For A0/A2 access, this register is not used and ignored.

RAMDATAL (0x79) RAM Data Port Low Byte RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
WRITE	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

This is a pseudo register. Operation on this register yields the execution to the SRAM location pointed by the RAM address register.

PWDATA (0x00~0x07) PW1 and PW2 Data Register W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	-	-	-	-	-	-	-
WRITE	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

PWCONT (0x08) Password Control Register W (0x00000000)

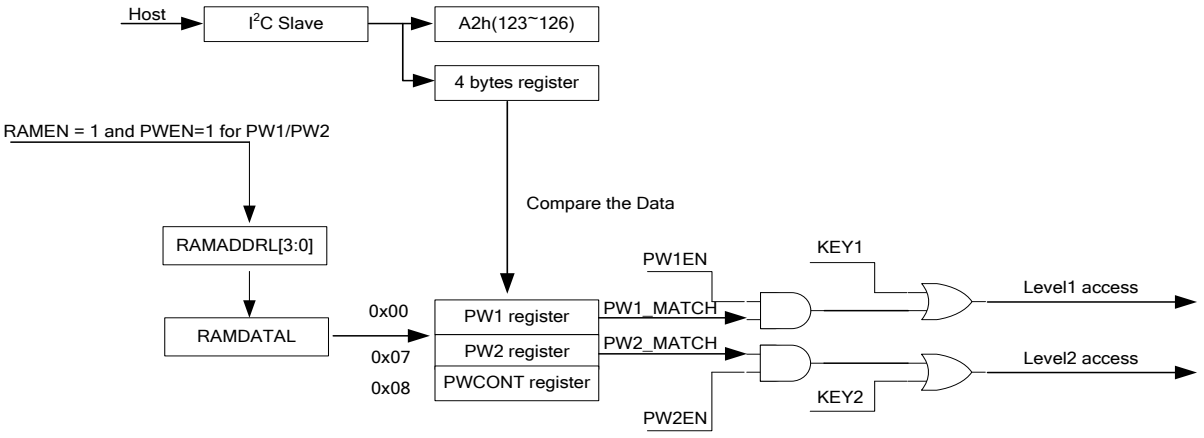
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	-	-	-	-	-	-	-
WRITE	PW1EN	PW2EN	KEY1	KEY2	-	-	-	-

PW1EN Set this bit to 1 to allow PW1 to operations. Set this bit to 0 to disable the hardware PW function.

PW2EN Set this bit to 1 to allow PW2 to operations. Set this bit to 0 to disable the hardware PW function.

KEY1 Set this bit to 1 to open Level 1 access by software. Set this bit to 0 to disable the access.

KEY2 Set this bit to 1 to open Level 2 access by software. Set this bit to 0 to disable the access.



ADDRESS RANGE		READ	WRITE	Note
A2	0~95 (Warning/Alarm Thresholds, Calibration Constants …)	all	PW2	
	96~110 (Diagnostic Monitor Data …)	all	PW2	
	110 (bit[6] Soft TX_Disable)	all	PW1/PW2	Note 1
	111~119(Alarm flags, Warning flags …)	all	PW2	
	120~126(123~126:PW1 PW2 Access …) (Note 1)	NA	all	Note 2
	127	all	PW2	
	128~255	all	PW1	
A0	0~127; 128~255	all	PW2	

Note 1: If PW1 is opened then only bit[6] soft TX_DISABLE can be written. If PW2 is opened then whole byte can be written. Also note altering bit-6 does not set A2LMST status bit.

Note 2: A2 [120-126] are write-only. The write is into password register not into the I²C SRAM.

2.3 I²C Master Controller

The I2C master controller provides the interface to I²C slave devices. The main purpose of I²C master in CS6721 is to control the external I²C EEPROM that is used to store the application program as well as configuration data and temperature look up tables. It can be programmed to operate with arbitration and clock synchronization to allow it to operate in multi-master configurations. The master uses MSCL and MSDA pins. The controller contains a built-in 8-bit timer to allow various I²C bus speed. Please note MSCL is an output only pin. MSCL is also used to configure the slave I²C address depending on the external pull-up or pull-down resistor configuration during the exit of power-on reset.

I2CMTPRD (0x71) I²C Master SCL Clock Configuration RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
WRITE	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0

This register set the period time of I2C bus clock – SCL. The SCL period time is set according to SCLPERIOD = 8 * (1 + I2CMTPRD)/SYSCLK

I2CMSA (0x72) I²C Master Slave Address Register RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	SA6	SA5	SA4	SA3	SA2	SA1	SA0	RS
WRITE	SA6	SA5	SA4	SA3	SA2	SA1	SA0	RS

SA6 – SA0 defines the slave address the I²C master uses to communicate. RS bit determines if the next operation will be a RECEIVE (1) or SEND (0).

I2CMBUF (0x73) I²C Master Data Buffer(0x00 RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
WRITE	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

I2CMBUF functions as a transmit data register when written and as a receive data register when read. When written, TD will be sent on the bus by the next SEND or BURST SEND operations. TD7 is sent first. When read, RD contains the 8-bit data that has been received the bus due to the last RECEIVE or BURST RECEIVE operations.

I2CMCR (0x70) I²C Master Status and Configuration RW (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

READ	-	BUSBUSY	IDLE	ARBLOST	DATAACK	ADDRACK	ERROR	BUSY
WRITE	INFILEN	I2CMRST	-	HS	ACK	STOP	START	RUN

INFILEN Set this bit to 1 will enable a analog filter that filters out pulse width less than 50nsec on SDA and SCL lines.

I2CMRST Set this bit to 1 will reset the I2C Master Controller. All state machine and signal returns to their idle mode. Set this bit to 0 for normal operations.

The I^2C MCR register is used for setting control when it is written, and serve as the status when read. INFILEN is input pulse filtering control. When IFILEN is set, pulses shorter than 50 nsec on inputs of SDA and SCL are filtered out.

The START bit is used to generate START, or REPEAT START protocol. The STOP bit determines if the cycle will stop at the end of the data cycle or continue on to a burst. To generate a single read cycle, SA is written with the desired address, RS is set to 1, and I^2C MCR is written with ACK=0, STOP=1, START=1, RUN=1 to perform the operation and then STOP. When the operation is completed (or aborted due to errors), I^2C master generates an interrupt. The ACK bit must be set normally 1. This causes the controller to send an ACK automatically after each byte transaction. The ACK bit must be reset when set to 0 when the master is operated in receive mode and intend not to receive further data from the slave device.

The following table lists the permitted control bits combinations in master idle mode.

HS	RS	ACK	STOP	START	RUN	OPERATIONS
0	0	-	0	1	1	START condition followed by SEND. Master remains in TRANSMITTER mode
0	0	-	1	1	1	START condition followed by SEND and STOP
0	1	0	0	1	1	START condition followed by RECEICE operation with negative ACK. Master remains in RECEICER mode
0	1	0	1	1	1	START condition followed by RECEIVE and STOP
0	1	1	0	1	1	START condition followed by RECEIVE. Master remains in RECEIVER mode
0	1	1	1	1	1	Illegal command
1	0	0	0	0	1	Master Code sending and switching to HS mode

The following table lists the permitted control bits combinations in master TRANSMITTER mode.

HS	RS	ACK	STOP	START	RUN	OPERATIONS
0	-	-	0	0	1	SEND operation. Mater remains in TRANSMITTER mode
0	-	-	1	0	0	STOP condition
0	-	-	1	0	1	SEND followed by STOP condition
0	0	-	0	1	1	Repeated START condition followed by SEND. Master remains in TRANSMITTER mode
0	1	-	1	1	1	Repeated START condition followed by SEND and STOP condition
0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with negative ACK. Master remains in TRANSMITTER mode
0	1	0	1	1	1	Repeated START condition followed by SEND and STOP condition.

0	1	1	0	1	1	Repeated START condition followed by RECEIVE. Master remains in RECEIVER mode.
0	1	1	1	1	1	Illegal command

The following table lists the permitted control bits combinations in master RECEIVER mode.

HS	RS	ACK	STOP	START	RUN	OPERATIONS
0	-	0	0	0	1	RECEIVE operation with negative ACK. Mater remains in RECEIVE mode
0	-	-	1	0	0	STOP condition
0	-	0	1	0	1	RECEIVE followed by STOP condition
0	-	1	0	0	1	RECEIVE operation. Mater remains in RECEIVER mode
0	-	1	1	0	1	Illegal command
0	1	0	0	1	1	Repeated START condition followed by RECEIVE operation with negative ACK. Master remains in RECEIVER mode
0	1	0	1	1	1	Repeated START condition followed by RECEIVE and STOP conditions
0	1	0	1	1	1	Repeated START condition followed by RECEIVE. Master remains in RECEIVER mode
0	0	-	0	1	1	Repeated START condition followed by SEND. Master remains in TRANSMITTER mode.
0	0	-	1	1	1	Repeated START condition followed by SEND and STOP conditions.

All other control bits combinations not mentioned in the above three tables are NOP. In Master RECEIVER mode, STOP conditions should be generated only when after data negative ACK executed by Master, or address negative ACK executed by slave. Negative ACK here means SDA is pulled low during the acknowledge clock pulse.

I2CMCR when read reflect the status of the I^2C master controller.

IDLE this bit indicates that I^2C master is in the IDLE mode.

BUSY this bit indicates that I^2C master is receiving or transmitting data, and other status bits are not valid.

BUSBUSY this bit indicates that the external I^2C bus is busy and access to the bus is not possible. This bit is set/reset by START and STOP conditions.

ERROR this bit indicates that error occurred in the last operations. The errors include slave address was not acknowledged, or transmitted data was not acknowledged, or the master controller lost arbitration.

ADDRERR this bit indicates that the last operation slave address transmitted was not acknowledged.

DATAERR this bit indicates that the last operation data transmitted was not acknowledged.

ARBLOST this bit indicates that the last operation I^2C master controller lost the bus arbitration.

2.4 System Reset Register

This register is used for either MCU or host to issue a system-wide reset to CS6721. Writing to SYSRESET (0x75) location with data content of “55” will cause the system reset after 1024 clock cycles.

SYSRESET (0x75) System Reset Register WO (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	-	-	-	-	-	-	-	-
WRITE	-	-	-	-	-	-	-	-

The effects of reset register and WDT reset is the same. Both resets will load all register with default value, then execute boot ROM procedure that loads the application program into SRAM and pass the control to the application program.

2.5 Boot ROM Code and EEPROM Contents

The on-chip ROM integrated three application：1. Special application program by the user defined; 2. general purpose SFP/PON application program with DDM function. Romcode gets all data from the external EEPROM in this application; 3. general purpose SFP/EPON application program without the external EEPROM.

CS6721 has a 2K ROM for Boot and before code is executed, the ROMSEL (0x51) bit is tested first..

When ROMSEL=1, it means the commonly application of SFP/EPON without the external EEPROM, which includes: the setting of SDDAC through ADCIN2, adjustment of DCBBIAS by adjusting the resistance of MPD pin, temperature compensation of MODDAC through ADCIN1 and pin9, during this mode, DDM and open loop is invalid.

Unlike the situation above, when ROMSEL=0, the romcode will load Romheader from EEPROM first, and therefore determine which application be supported.

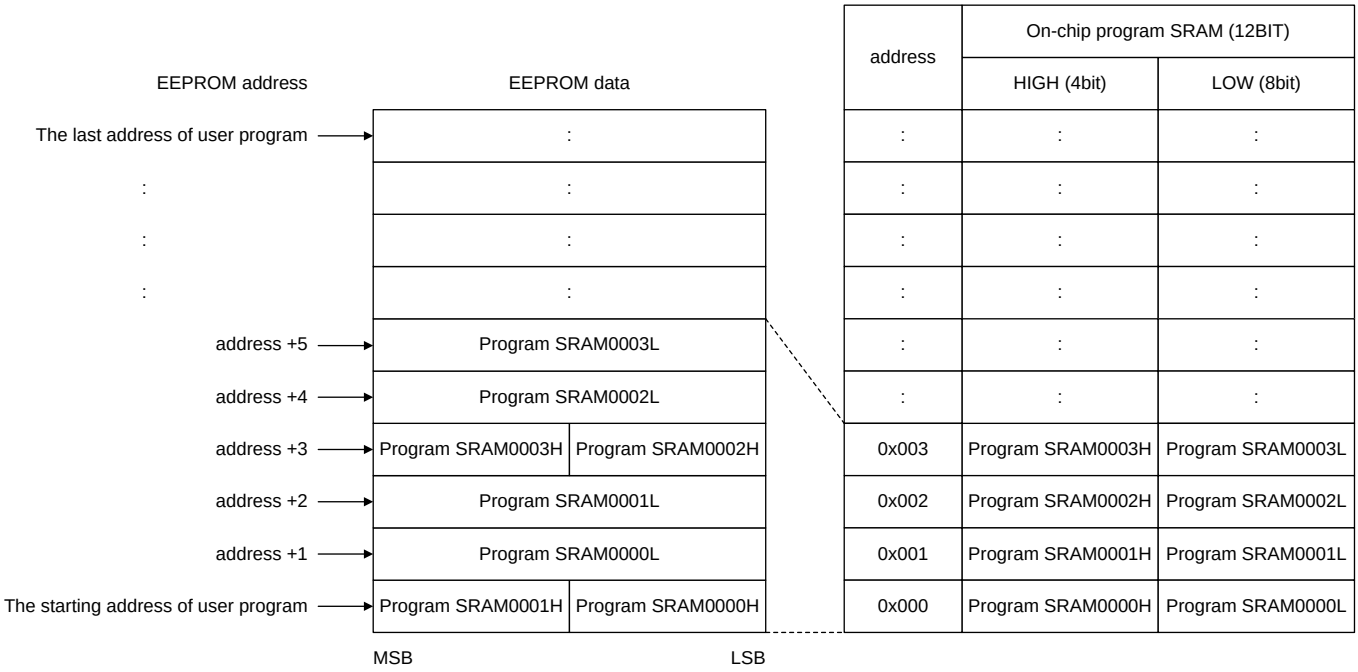
Romheader (stored in EEPROM)is a 48 bytes table which ranges from 0x0000-0x002F is described as below:

CS6721 RomHeader（0x0000）

ADRESS in EERROM		CONTENT	SIZE	DESCRPTION
0X0 (control byte)	bit7	Application Solution	1 bytes	bit7 = 0: uploads and execute the program of external EEPROM, bit0~bit6 was not concerned at this situation. bit7 = 1: executing the romcode, the last 16bytes of romheade（0020H ~ 002FH)can be used with other purpose
	bit6	Temperature Compensation of APD		bit7 = 1&& bit6 = 1: adjust the APD voltage through PIN9 DACOUT 0~1.8V bit7 = 1&& bit6 = 0: the voltage of APD is not adjustable
	bit5	Open/Close loop		bit7 = 1&& bit5 = 1: open loop of TX bit7 = 1&& bit5 = 0: close loop of TX
	bit4	Temperature Sensor Selection		bit7 = 1&& bit4 = 1: internal temperature sensor bit7 = 1&& bit4 = 0: external temperature sensor
	bit3	Host write to A0/A2		bit7 = 1&& bit3 = 1: allow host write the A0 A2,when the data updating of A0 A2 had been tested by romcode ,it will be stored in the EEPROM; bit7 = 1&& bit3 = 0: host is not allowed to write the A0 A2.
	bit2	DDM		bit7 = 1&& bit2 = 1: DDM available bit7 = 1&& bit3 = 0: DDM not available
	bit1	Voltage Protection		bit7 = 1&& bit2 = 1: shut off TX RX when voltage of VDDR is higher than 3.6;and TX RX are working properly when the voltage of VDDR is beyond 2.8 ~ 3.6V bit7 = 1&& bit3 = 0: TX RX are not shut off
	bit0	Rise/Fall of APD Compensation LUT		bit7 = 1&& bit0 = 1: rise of APD temperature compensation LUT bit7 = 1&& bit0 = 0: fall of APD temperature compensation LUT

CS6721 RomHeader（48Bytes）					
ADDRESS		**CONTENT**		**SIZE (bytes)**	**DESCRPTION**
0X0001		HIGH	The starting address of application program	2	
0X0002		LOW			
0X0003		HIGHT	Size of application program	2	Maximum:3KBytes
0X0004		LOW			
0X0005		The CRC of application program		2	
0X0006					
0X0007		HIGH	Starting address of DMI	2	
0X0008		LOW			
0X0009		HIGH	Size of DMI	2	
0X000A		LOW			
0X000B		HIGH	Starting address of SFP data	2	
0X000C		LOW			
0X000D		HIGH	SFP size	2	1≤ SFP size ≤512,The data size stored in SFP from A0 to A2
0X000E		LOW			
0X000F	bit7	Set MOD		1	bit7=0: configuration the MOD by ATC(see RomHeader 0x16 0x17)
					bit7=1: MOD compensation by LUT
0X0010		HIGH	Starting address of ADC temperature table	2	The data in temperature sensor table is the ADC of +85℃ and ADC D-value of each gap compared with the former
0X0011		LOW			
0X0012		Size of ADC temperature table		1	It represent the addressing space of temperature sensor,and the size can't be more than 127 with the situation of small EEPROM with DDM function
0X0013		Undefined		1	
0X0014		HIGH	Starting address of SD compensation table	2	
0X0015		LOW			
0X0016		K_{ratio}	Calculation of MOD	2	When 0x000F:BIT7=0，MODDAC = K_{ratio} X DCBDAC/256 +CONSTANT_C
0X0017		CONSTANT_C			
0X0016		HIGH	Starting address of MOD compensation table	2	When 0x000F:BIT7=1，0X16&0X17 are used individually to Store the high and low byte of MOD compensation table
0X0017		LOW			
0X0018		HIGH	Starting address of DCB compensation table	2	The starting address of MPD compensation table in the close loop
0X0019		LOW			
0X001A		HIGH	Starting address of APD compensation table	2	
0X001B		LOW			

0X001C	HIGH	Starting address of register configuration table	2	
0X001D	LOW			
0X001E	Size of register configuration table		1	
0X001F	CHECKSUM		1	Data CHECKSUM of EEPROM from 0X0000 ~ 0X001E
0X0020	HIGH	Title of application program	12	ASCII characters
0X002B	LOW			
0X002C	Version of application program		4	ASCII characters
0X002F				



If bit7 address 0 of Romheader is clear, the rom code will start first loading the application program user defined into the on-chip program SRAM. Note that each location of on-chip SRAM contains 12 bits. Therefore to fill two location of SRAM, three bytes of EEPROM are used. As an example, the program starting address is 0x1000, it mean 0x1000 contains the high nibbles of 0000 and 0001 on-chip program SRAM, and 0x1001 contains low byte of 0000, and 0x1002 contains low byte of 0001 as shown in the figure. After loading the whole application program, the boot code examines the 2-byte CRC to check the validity of the uploaded content. If successful, the boot code continues to load the 512 bytes from EEPROM to the 512 bytes of on-chip SFP RAM. For non-SFP applications, the copy operation still executes, and the application program can just ignore the copied contents, and treat the space above EEPROM as user defined storage. At the end of copying, the boot code transfers the CPU control to application program that is just uploaded from EEPROM.

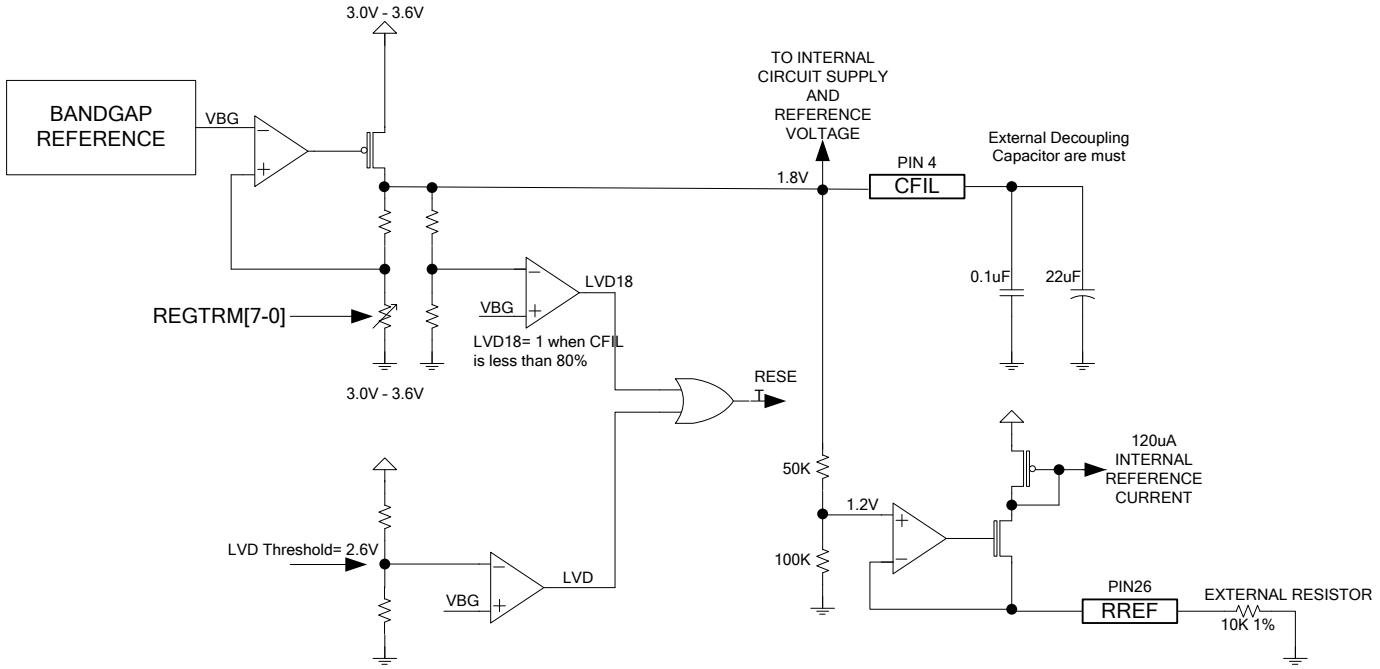
If bit7 address 0 of Romheader is set, the MCU will execute general purpose SFP/PON application program with DDM function. It will upload SFP data and configure registers according the registers configuration table and then implement DDM. In this application, a general SFP/PON module with DDM can be realized when used with a 2KB EEPROM.

3. Special System Analog Peripherals and Its Registers

This section describes the system analog peripherals including core supply voltage regulator, low supply voltage detection, and on-chip oscillator, ADC, and DAC.

3.1 On-Chip 1.8V Regulator

The on-chip regulator is used to provide 1.8V to internal core logic and analog circuit which is regulated from 3.3V supply. The on-chip regulator derive the 1.8V through the on-chip Band-gap, the on-chip regulator also provides a mechanism for power-on/off reset which force CS6721 into reset state if the regulator output is less than 80% of the target value or the supply voltage is less than 2.6V. The block diagram of the regulator and low-voltage supply detection are shown in the following circuit diagram.



Please note the regulator output is on pin 4 (CFIL) and external decoupling capacitors are necessary for low-noise operation. Because there are always chips to chips variations on the Bandgap voltage, and the 1.8V is used for internal reference, a register trimming is provided to fine trim the regulator output. In the calibration process, supply voltage (3.0V – 3.3V) is digitized by the ADC which has full-scale range of VDD18 (1.8V). Therefore, if VDD is known, then VDD18's true value can be derived, and a new trimming value can be programmed into REGTRM. VDD18 is used for internal reference detection as well as to set the precision reference current using external 10K resistor connected to RREF pin. Therefore, trimming VDD18 as precise as 1.8V is important for achieving precision module operations.

REGTRM (0x50) Regulator Trim Register W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	RTRIM7	RTRIM6	RTRIM5	RTRIM4	RTRIM3	RTRIM2	RTRIM1	RTRIM0
WRITE	RTRIM7	RTRIM6	RTRIM5	RTRIM4	RTRIM3	RTRIM2	RTRIM1	RTRIM0

REGTRM is defaulted to 0x00. Because of chips to chips variations, the native VDD18 may deviate from the precise 1.8V. The firmware can then load REGTRM with calibrated value to set the VDD18 as close to 1.8V as possible. After the new value is loaded, the regulator will be stable about 1msec later. The following table shows the relative trimming percentage of REGTRM versus the native value.

REGTRM[7:0](0x50h)	UP(%)	REGTRM[7:0](0x50h)	DOWN(%)
00	0(default)	00	0(default)
01	0.66%	10	-1.33%
02	1.39%	20	-2.54%

03	2.12%	30	-3.65%
04	2.95%	40	-4.72%
05	3.75%	50	-5.69%
06	4.60%	60	-6.63%
07	5.49%	70	-7.46%
08	6.54%	80	-8.29%
09	7.50%	90	-9.01%
0A	8.57%	A0	-9.72%
0B	9.63%	B0	-10.39%
0C	10.85%	C0	-11.02%
0D	12.05%	D0	-11.6%
0E	13.36%	E0	-12.15%
0F	14.69%	F0	-12.71%

For example, if the native VDD18 is measured as 1.75V, then it should be adjusted up by 2.85%. Thus REGTRM = 03 should be used. In general, it is preferred that VDD18 to be trimmed to +/- 1% of 1.8V because this voltage is also used for ADC reference and other reference levels.

There is a power on/off detection associated with the regulator. During power on or off transient, if CFIL falls below the 80% of the target value or supply voltage falls below 2.6V, the internal reset is forced on. This ensures that the CPU is put in reset (idle) state if the core voltage supply is not high enough. This ensures that if the core supply is not high enough, CPU program is halted and thus further improves the data integrity and system reliability.

It is also shown in the diagram, that 2/3 of VDD1.8V is used along with an external precision 10K resistor is used to provide an accurate reference current. This reference is used as the unit current amount for generating various current including DC bias current, modulation current for the laser. Because VDD1.8 can be trimmed through REGTRM, therefore accuracy of these outputs can be ensured.

The low supply voltage detection is to detect the level of external supply and provide warning to application software that the external supply is below marginal value. After detecting this warning the application software should stop critical task immediately and prepare for shut down or wait until the low supply condition is passed. The detection threshold of the supply voltage can be configured, and the status is read from LVDTSCFG register.

LVDTSCFG (0x51) Low Supply Detection/Temperature Sensor Configuration Register R/W 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	LVDST	ROMSEL	PW2MATCH	PW1MATCH	TSL1	TSL0	TCS1	TCS0
WRITE	-	-	-	-	TSL1	TSL0	TCS1	TCS0

LVDST This bit is read-only and reflects the low supply voltage detection result. LVDST =1 indicates that the supply is lower than 2.6V.

ROMSEL ROMSEL is read-only and is determined by bonding option
ROMSEL=1 indicates the normal application of SFP/EPON without EEPROM.
ROMSEL=0 indicates the following two aspects: the first is the download and executing of EEPROM program when bit7 of the first RomHeader byte is 0 . The second is the ROMCODE executing general purpose SFP/PON application program with DDM, during this mode,functions such as the temperature compensation of APD, open/close loop , internal or outside temperature sensor ,DDM and so on are selectable.

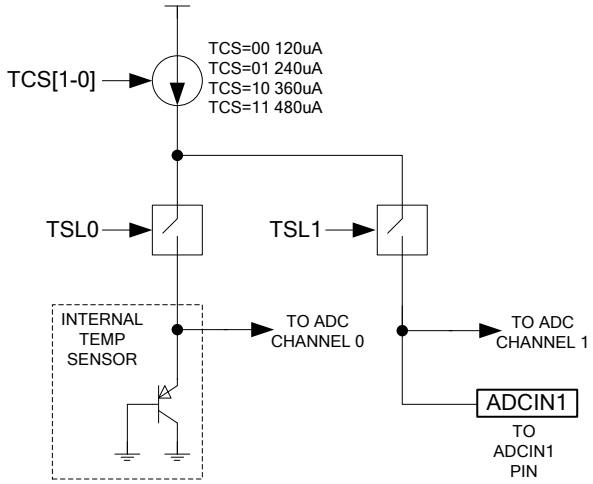
PW2MATCH The receiver data matches level 2 Password value.

PW1MATCH The receiver data matches level 1 Password value.

TSL1	Set this bit to 1 to connect the temperature sensor bias current to the ADCIN1 pin. If external temperature sensor is not used, or it does not require a bias current, this bit should be set to 0.
TSL0	Set this bit to 1 to connect the temperature sensor bias current to the internal temperature sensor.
TCS[1-0]	These two bits determine the bias current level for the temperature sensor. 00 = 120uA 01 = 240uA 10 = 360uA 11 = 480uA

3.2 Internal and Off-Chip Temperature Sensor

CS6721 has internal temperature sensor using a diode connected PNP transistor with a current source connected to it. The diode voltage is sent to channel 0 of the 12-bit ADC and can be digitized and used to determine the chip temperature from a look-up table stored in the external EEPROM. If off-chip temperature measurement is desired, the bias circuit can be used to connect to an external diode and ADC can be used. The following diagram shows the control of the temperature sensor connection. The configuration is done through LVDTSCFG register as described above.



There are chips to chips variations on the characteristics of internal PNP diodes that may result offset errors for ADC measuring of the temperature. However, the temperature dependency of the diode voltage is determined by silicon Band-gap. Therefore at calibration, the VDD18 is first calibrated so ADC's accuracy is obtained. Then knowing the current calibrated temperature, and a value obtained from internal temperature sensor digitized by ADC, a temperature look-up table can be established using band-gap calculation. This table can then be written into the external EEPROM by the calibration host through ISP. These details are described in the application notes of CS6721.

Internal On-Chip Oscillator

An internal multi-vibrator type oscillator is used to generate clock signal for MCU and its peripherals. The default oscillator frequency is 25MHz, and can be fine trimmed. The clock to the MCU and peripherals can be configured and the configurations are defined in OSCTRM register.

OSCTRM (0x52) Clock Configuration and OSC Trim Register R/W 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	CLKSL1	CLKSL0	OSCTEST	REFSEL	PEAKTC	SKEW2	SKEW1	SKEW0
WRITE	CLKSL1	CLKSL0	OSCTEST	REFSEL	PEAKTC	SKEW2	SKEW1	SKEW0

CLKSL[1-0] This two bits controls the pre-scaling of the system clock. The system clock frequency should be set as low as possible to minimize digital noise interference.
CLKSL = 00 SYSCLK = OSCCLK/2 (12.5MHz)
CLKSL = 01 SYSCLK = OSCCLK/4 (6.25MHz)
CLKSL = 10 SYSCLK = OSCCLK/8 (3.125MHz)
CLKSL = 11 SYSCLK = OSCCLK/16 (1.56MHz)

OSCTEST Set this bit to 1 will put OSCCLK/16 to be output on pin 9 (DAC). This bit is used only for manufacturing test and should be set to 0 for normal operations.

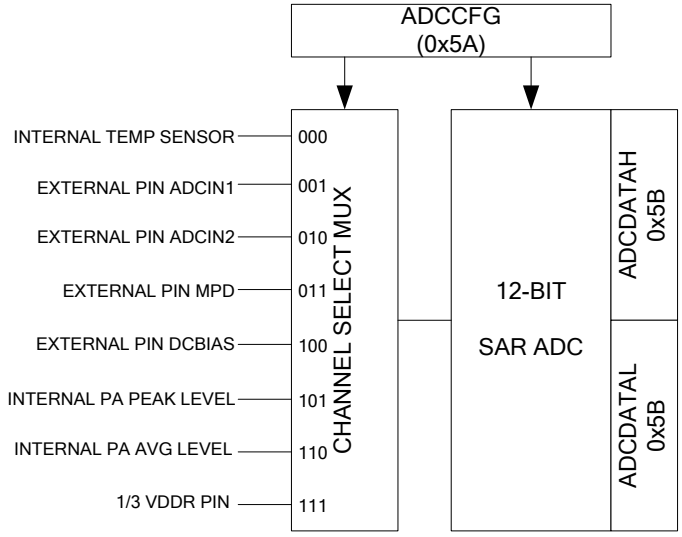
REFSEL Set this bit to 0 to use 2/3 VDD18 for the oscillator reference. Set this bit to 1 will use the Band-Gap reference for the oscillator. Because VDD18 is typically calibrated, therefore for normal operation, this bit should be set to 0.

PEAKTC This bit is used to control the peak detector time constant in the post amplifier. When this bit is 0, the time constant is set at about 30usec. When this bit is set to 1, the time constant is about 15usec. Default for normal operation should be 30usec.

SKEW[2-0] These bits fine trim the transmit edge skew. The adjustment ranges +/- 9 psec. Relative to the TXIP-TXIN rising edges, the following table shows the relation of the setting and cross-point
000 = No skew
001 = -5 psec
010 = -10 psec
011 = -15 psec
100 = +5 psec
101 = +10 psec
110 = +15 psec
111 = No skew

3.4 12-Bit SAR ADC and 10-Bit R2R DAC

CS6721 includes a 12-bit SAR ADC for performing analog measurement. Based on the measurement, various parameters of PA, LD driver as well as environment can be determined and thus compensated for a reliable fiber optics operation. The ADC uses VDD18 (CFIL) as its full-scale reference. For accurate measurement of ADC, VDD18 should be calibrated first. The ADC has 8 channel inputs and is shown in the following figure.



Typical usages of these channels are described below. ADCIN1 is typically connected to an external temperature sensor. ADCIN2 can be connected to PIN-TIA monitor output to determine the input optical power or a DC/DC converter output in case an APD high voltage is used. MPD pin level can be measured to determine if Laser

output failure. ADC can also be used to measure the voltage on DCBIAS pin to determine if there is valid laser bias for laser failure. PA peak detector level can be used for software SD control and for input power monitoring. 1/3 VDDR level is important measurement to calibrate the VDD18.

Because ADC is a SAR type converter, each conversion takes 14 cycles to resolve 12 bits. The clock to ADC can be pre-scaled. In general a slower ADC can yield more accurate result and less noise generated. The default ADC clock after reset is SYSCLK/8. The following register definitions describe the configuration and operation of the ADC.

ADCCFG (0x5A) ADC Configuration Register R/W 0x00011000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	ADCPD	CONV	ADPS2	ADPS1	ADPS0	CHSEL2	CHSEL1	CHSEL0
WRITE	ADCPD	CONV	ADPS2	ADPS1	ADPS0	CHSEL2	CHSEL1	CHSEL0

ADCPD — Set this bit to 1 will power down the ADC. Set this bit to 0 allows normal ADC operations. The ADC needs about 100usec to reach stable states for conversion after enable.

CONV — Set this bit to 1 will start ADC for continuous conversion. The result of the conversion result will be latched onto the ADCDATAH and ADCDATL.

ADPS[2-0] — ADC Clock rate scaling setting
000 = SYSCLK
001 = SYSCLK/2
010 = SYSCLK/4
011 = SYSCLK/8
100 = SYSCLK/16
101 = SYSCLK/32
110 = SYSCLK/64
111 = SYSCLK/128

CHSEL[2-0] — ADC channel select control.
000 = Internal Temperature Sensor
001 = External Pin ADCIN1
010 = External Pin ADCIN2
011 = External Pin MPD
100 = External Pin DCBIAS
101 = Internal Post Amplifier Peak Detector Peak Level
110 = Internal Post Amplifier Peak Detector Average Level
111 = External Pin VDDR * 1/3

ADCDATAH (0x5B) ADC Conversion Result High Byte Register RO 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	EOC	-	-	-	ADC11	ADC10	ADC9	ADC8
WRITE	DCBURST[7-0]							

EOC — This bit is set by ADC hardware to indicate a valid result is available on ADCDATAH and ADCDATAL. This bit is read-only, and is self cleared when ADCDATAL is read.

ADC[11-8] — This is high nibble of the ADC conversion result.

DCBURST[7-0] — This register is used to provide a sub-threshold current on laser through DCBIAS output during the burst-off duration. This can help the laser transition from off to on but may introduce optical power leakage during off time. This current is always on if set.

Note that EOC is set by the hardware when the conversion is complete and it is cleared when ADCDATAL (0x5C) is read by program. Before EOC is cleared the new conversion will not be updated into ADCDATA registers. Once EOC is cleared, new conversion result will be written. It is recommended that the program should always read the

high byte first to determine if the conversion is completed and result is valid, then followed by reading the low byte. This ensures that the data obtained are synchronized.

ADCDATAL (0x5C) ADC Conversion Result Low Byte Register RO 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
WRITE	FAILSELA	FAILSELB	COC2	COC1	COC0	BWC2	BWC1	BWC0

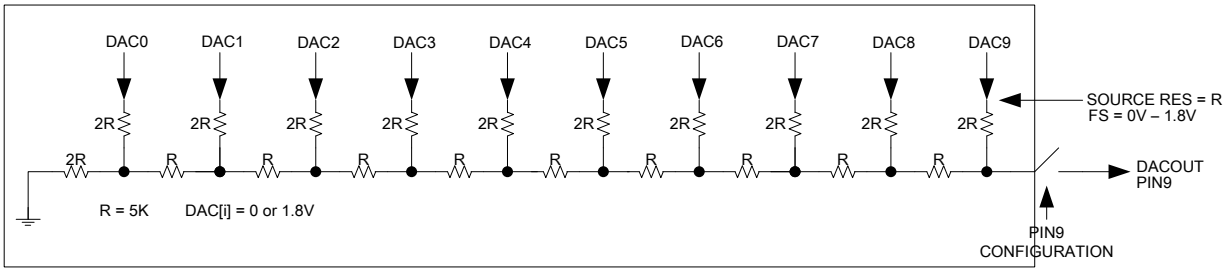
FAILSELA — Set this bit to 1 will enable MPDFAIL as a FAIL condition. Writing this bit 1 will also clear the latched MPDFAIL status if FAILLATEN=1. FAILSELA=0, MPDFAIL still operates the same but just will not affect the FAULT output.

FAILSELB — Set this bit to 1 will enable APCFAIL as a FAIL condition. Writing this bit 1 will also clear the latched APCFAIL status if FAILLATEN=1. FAILSELA=0, APCFAIL still operates the same but just will not affect the FAULT output.

COC[2-0] — These bits are used by Internal test.

BWC[2-0] — These bits are used by Internal test.

CS6721 also includes a 10-bit R2R DAC. The R2R DAC circuit implementation is shown in the following diagram.



Because the R2R network is driven by DAC[9-0] which is either 1.8V or 0V, and VDD18V is calibrated, so the output follow the calibrated precision of the VDD18V. The full-scale output of the DAC is from 0V to 1.8V. Please note the DAC output has a source impedance of approximately 10K therefore it should not be used to drive low resistive load. The DAC output is connected to PIN9 (DAC) under Pin 9 configuration register control PIN9CFG.FSEL.

DACDATAH (0x5D) DAC Data High Byte Register RW 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	SEL	MPDMREN (SEL=1) DACEN (SEL=0)	-	-	-	-	DACDATA[9]	DACDATA[8]
WRITE	SEL	MPDMREN (SEL=1) DACEN (SEL=0)	-	-	-	-	DACDATA[9]	DACDATA[8]

SEL — This bit defines whether DACDATA or MPDTHDATA will be operated on when access to 0x5E. If this bit is set, then the operation on 0x5E is referenced to MPDTHDATA[7-0]. If this bit is 0, then the operation on 0x5E is referenced to DACDATA[7-0].
This bit also controls whether MPDTHEN or DACEN is referenced in bit 6.

EN — Enable control bit. This bit is enable control for DAC and MPDTHD comparator depending on SEL bit setting. When SEL is 1, it is MPDMREN. When SEL is 0, it is DACEN.

DACDATA[9-8] — These are high order two bits of DAC data.

DACDATAL (0x5E) DAC Data Low Byte Register RW 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	DACDATA[7-0]							
WRITE	DACDATA[7-0]							

MPDTHDATA (0x5E) MPD Current Compare Threshold Register RW 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	MPDTHDATA[7-0]							
WRITE	MPDTHDATA[7-0]							

Because 0x5E serve as the address for both DACDATA[7-0] and MPDTHDATA[7-0], the operations of 0x5D and 0x5E need special attention and is described in more detail.

Writing DACDATA should start with writing 0x5D with SEL bit set to 0. For example, to write DAC value of “26A”, and enable DAC, write 0x5D with “42”, followed by writing 0x5E with “6A”.

Writing MPDTHDATA, should start with writing 0x5D with SEL bit set to 1. For example, to write MPDTHDATA of “6A”, write bit 7 (SEL) of 0x5D with “1”, then write bit 6(EN) of 0x5D with “1”, followed by writing 0x5E with “6A”. It is important that when operating on MPDTHDATA, the DACDATA[9-8] are not disturbed. Therefore, the program should first read out DACDATA[9-8], and then maintain the same value when writing into 0x5D.

The reading operation of 0x5D and 0x5E returns value depending on SEL bit too. For example, if reading 0x5D returns “01000010”, because MSB bit (SEL) is 0, then the value of bit 6 reflects DACEN.

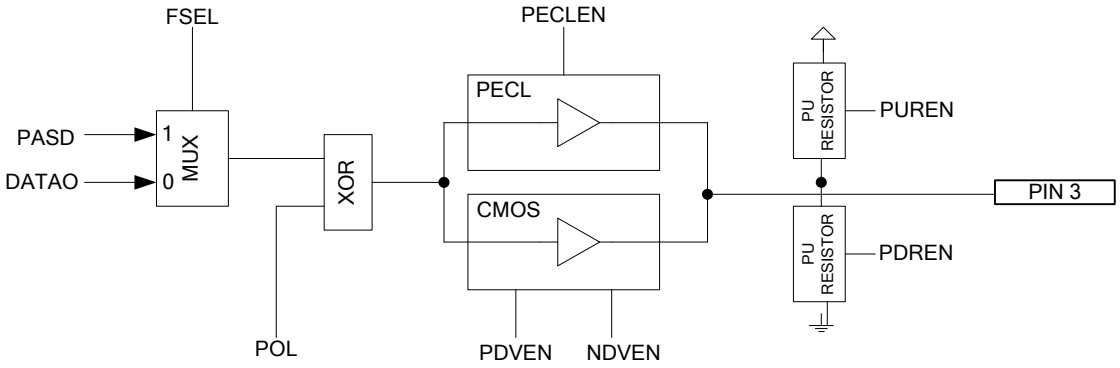
The MPDTHDDATA[7-0] control a internal current source .The current range of this current source is 0~1.92mA (later than E1), each step is 7.5uA. When the MPD current of the laser diode is lower than the current of the internal current source which is set by MPDTHDDATA[7-0], the bit 6 (MPDTHD) of 0x5F(ANASTATUS) will be set to 0. If MPD current of the laser diode is higher than the current of internal current source, bit 6 of 0x5F will be set to 1. MPDTHD can be used in two purposes, one for laser safety warning, and one for measuring the real actual laser output power.

4. Pin Configurations

To provide flexibilities for optical module design, the pin function of LOS (pin 3), DAC (pin 9), FAIL (pin 10), BENP (pin 15), and BENN (pin 16) can be configured by software. This includes the definition of the function and the polarity of the signal. The following sections describe the operations.

4.1 Pin 3 (LOS) Configurations

Pin 3 is normally used for LOS output. The following diagram shows possible pin 3 configurations uses PIN3CFG (©) register. Pin 3 can be configured as output only.



The PASD signal (1 meaning input power exceeds threshold) can be directly passed to Pin 3 output by setting FSEL = 1. Or software can write to DATAO bit of the pin3 configuration register and select FSEL = 0, this bit will be passed to Pin 3. The polarity of these signals can be inverted by setting POL = 1. There two types of output buffer, a CMOS output buffer with independently controlled P drive and N drive or a PECL output level is selected if PECLENB = 0 (for PECL mode, PDVEN should be set to 1 and NDVEN should be set to 0). By setting PDVEN and

NDVEN, either CMOS (PDVEN=NDVEN=1) output, or Open-Drain type (PDVEN=0, NDVEN=1) can be configured. For example, if negative polarity of LOS (LOS=low for loss of signal), CMOS open-drain output is intended, then PDVEN=0, NDVEN=1, PUREN=PDREN=PECL=0, POL=0, FSEL=1, DATAO=X. The default configuration of Pin 3 is CMOS Hi-Z (later than E1) and as PASD output.

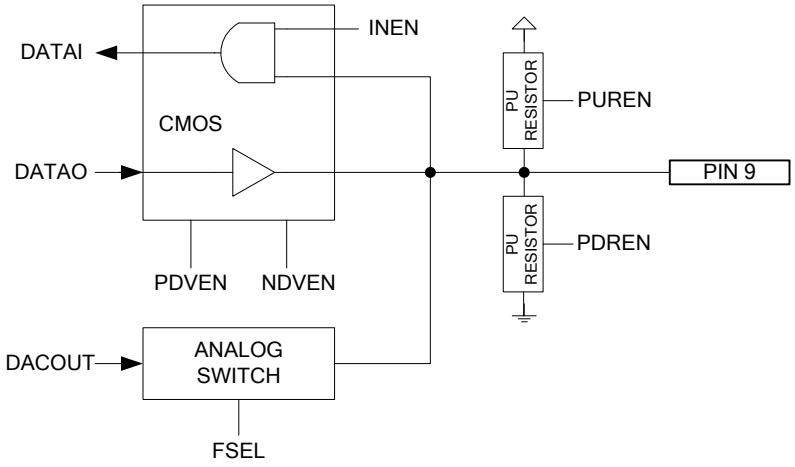
PIN3CFG (0x7A) Pin 3 LOS Configuration Register RW 0x00001010)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PDVEN	NDVEN	PUREN	PDREN	PECLENB	POL	FSEL	DATAO
WRITE	PDVEN	NDVEN	PUREN	PDREN	PECLENB	POL	FSEL	DATAO

PDVEN	Set this bit to enable the PMOS drive in the CMOS output driver
NDVEN	Set this bit to enable the NMOS drive in the CMOS output driver
PUREN	Set this bit to enable the on-chip weak pull-up resistor
PDREN	Set this bit to enable the on-chip weak pull-down resistor
PECLENB	Set this bit to disable the PECL driver. And clear this bit to 0 to enable PECL output. When PECL is selected, NDRIVE must be disabled. This bit default is disabled (Later than E1).
POL	Set this bit to reverse the output polarity
FSEL	Set this bit to pass the PASD status to the pin. Clear this bit to allow DATAO to pass to the pin.
DATAO	This bit is set or cleared by MCU and is under software control.

4.2 Pin 9 (DAC) Configurations

Pin 9 is normally used for R2R DAC output but it can also be configured for general-purpose digital IO pin. The following diagram shows possible pin 9 configurations uses PIN9CFG (0x7B) register. Pin 9 is also a test output for internal oscillator. When OSCTEST bit in OSCTRM register is set to 1, and PIN9CFG is configured as output pin, the 1/16th frequency of the IOSC is outputted on Pin 9. The default configuration Pin 9 is a general-purpose input.



PIN9CFG (0x7B) Pin 9 DAC Configuration Register RW 0x00001000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PDVEN	NDVEN	PUREN	PDREN	INEN	PIN23ST	FSEL	DATAI
WRITE	PDVEN	NDVEN	PUREN	PDREN	INEN	PIN23PDEN	FSEL	DATAO

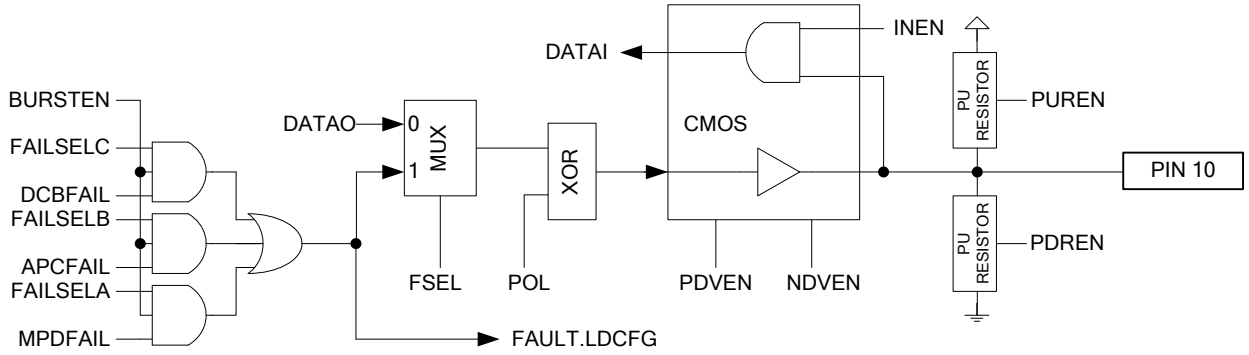
PDVEN	Set this bit to enable the PMOS drive in the CMOS output driver
NDVEN	Set this bit to enable the NMOS drive in the CMOS output driver
PUREN	Set this bit to enable the on-chip weak pull-up resistor
PDREN	Set this bit to enable the on-chip weak pull-down resistor

PIN23PDEN	PIN23PDEN=1 enables PIN23 input as TX power down. Pin23 is used as ADC channel 1 also can be used as TXVDD detection. When this pin falls below 1.3V, it will force transmit path to power down. When this pin is raised above 2.5V, it will enable the transmit path PIN23PDEN=0 disable PIN23 to control transmit power down.
PIN23ST	This reflects the status of PIN23 level. PIN23ST=0 if the level is less than 1.3V. PIN23ST=1, if the level is higher than 2.5V. This is with 1.2V hysteresis at center of 1.7V.
INEN	Set this bit to enable the CMOS input buffer. Clear this bit to disable the input buffer
FSEL	Set this bit to use this pin as DAC analog output. When using DAC function, CMOS output driver must be disabled and pull-up/pull-down resistors disabled too
DATAI	When this pin is configured as input pin, MCU can read this bit to obtain the pin status.
DATAO	When this pin is configured as output pin, MCU write this bit to control the output state.

4.3 Pin 10 (FAIL) Configurations

Pin 10 is normally used for FAIL output. Typical it is configured to reflect the status of hardware FAIL conditions, but it can also be configured for general-purpose digital IO pin. There are three hardware FAIL conditions and can be separately enabled to form the FAIL output. These include

The following diagram shows possible pin 10 configurations uses PIN10CFG (0x7C) register. The default configuration of Pin 10 is a general -purpose input.



PIN10CFG (0x7C) Pin 10 FAIL Configuration Register RW 0x00001000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PDVEN	NDVEN	PUREN	PDREN	INEN	POL	FSEL	DATAI
WRITE	PDVEN	NDVEN	PUREN	PDREN	INEN	POL	FSEL	DATAO

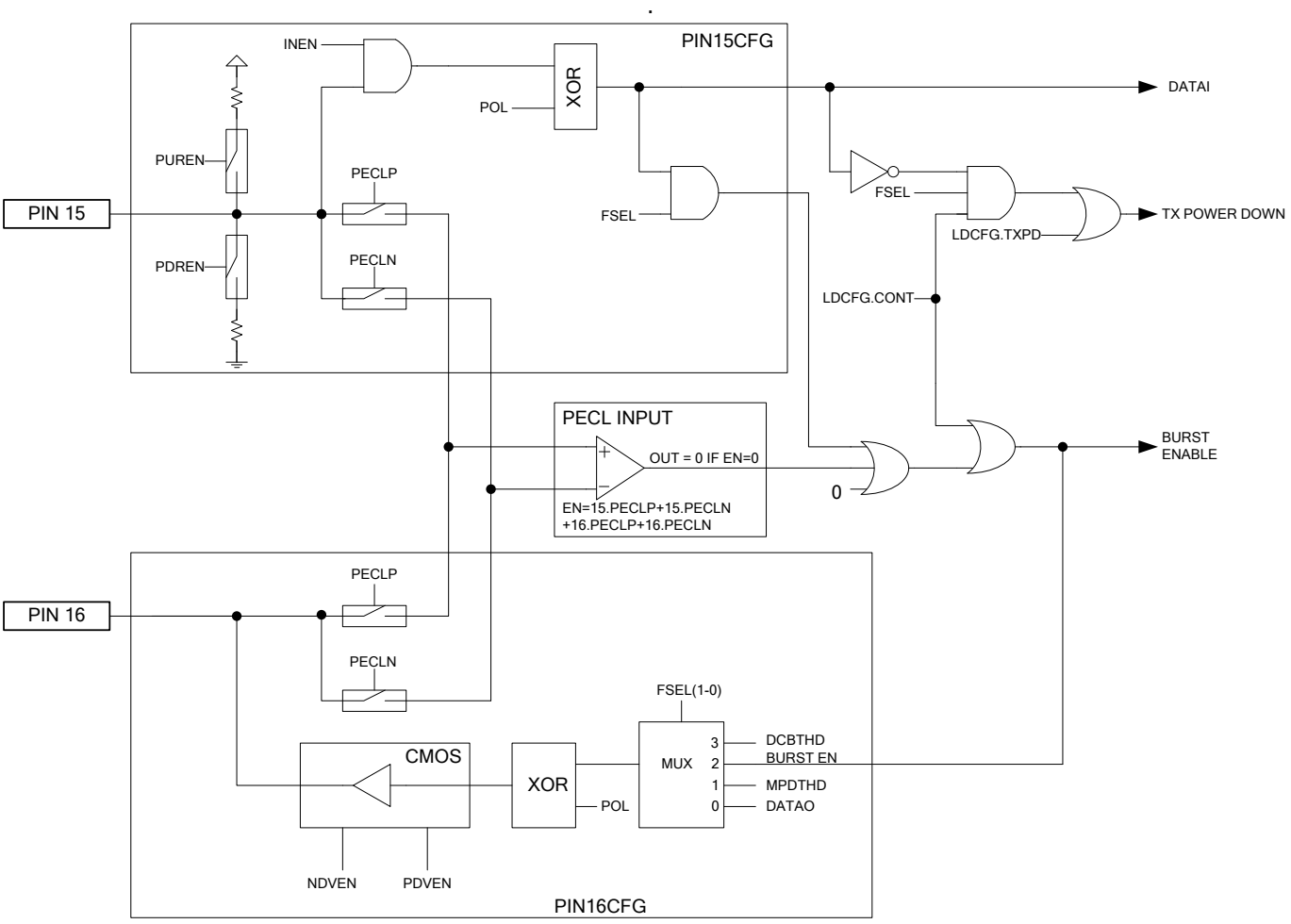
PDVEN	Set this bit to enable the PMOS drive in the CMOS output driver
NDVEN	Set this bit to enable the NMOS drive in the CMOS output driver
PUREN	Set this bit to enable the on-chip weak pull-up resistor
PDREN	Set this bit to enable the on-chip weak pull-down resistor
INEN	Set this bit to enable the CMOS input buffer. Clear this bit to disable the input buffer
POL	Set this bit to inverse the polarity of the output
FSEL	Set this bit to use this pin as FAIL status. Clear this bit to use software control of output.
DATAI	When this pin is configured as input pin, MCU can read this bit to obtain the pin status.
DATAO	When this pin is configured as output pin, MCU write this bit to control the output state.

4.4 Pin 15 and Pin 16 (BENP and BENN) Configurations

Pin 15 and Pin 16 has complicated configuration. Pin 15 and Pin 16 can be configured as either differential or single-ended fast PECL burst-enable control signal. Or Pin 15 can be configured as CMOS level burst-enable control, or a general purpose input. Pin 16 can be configured as a general purpose output, or the Laser Safety warning output. The internal BURST ENABLE is derived from these different configurations. If continuous mode of laser is required, setting LDCFG register's CONT bit will force BURST ENABLE to high. In this case, both BENP and BENN can be used for general-purpose I/O.

When Pin 15 or Pin 16 is configured as PECL input, either differential or single-ended, the input is biased to PECL threshold by the internal bias circuit. The PECL input buffer is powered down if none of these pins is PECL input. If both inputs are configured as GPI, then the CONT bit in LDCFG must be set to 1 so the internal burst enable signal is asserted for continuous mode operation. Otherwise the internal burst enable is de-asserted and the transmitter will not output.

The default configuration of Pin 15 is general-purpose CMOS input and typical usage of Pin 15 is either as TX_DISABLE or BURST_EN signals for fiber module. The differentiation between these two is done by CONT bit setting in LDCFG register. Please note that when used as TX_DISABLE, the asserted state will power down the transmit path. The transmit power down is also controlled by the TXPD bit in the LDCFG register. While used as BURST_EN, the transmit path is always enabled, and only the last stages of DCBIAS and MOD output are switched. When function as TX_DISABLE, it will also clear the latched FAIL flags.



PIN15CFG (0x7D) Pin 15 BENP Configuration Register RW 0x00001000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PECLP	PECLN	PUREN	PDREN	INEN	POL	FSEL	DATAI
WRITE	PECLP	PECLN	PUREN	PDREN	INEN	POL	FSEL	DCBDACF

PECLP	Set this bit to connect pin 15 to + input of PECL input buffer
PECLN	Set this bit to connect pin 15 to - input of PECL input buffer
PUREN	Set this bit to enable the on-chip weak pull-up resistor
PDREN	Set this bit to enable the on-chip weak pull-down resistor
INEN	Set this bit to enable the CMOS input buffer. Clear this bit to disable the input buffer.

POL	Set this bit to inverse the polarity of the input buffer.
FSEL	Set this bit to use CMOS inputs of pin 15 as the BURSTEN or TXDISABLE. If PECL is used, FSEL should be cleared to 0.
DATAI	When this pin is configured as CMOS input pin, MCU can read this bit to obtain the pin status.
DCBDACF	This bit is write-only. When APC=0, DCBDACF will set or clear the 0.5 LSB of DCBDAC output current allowing a finer resolutions of DCBDAC by software. When APC=1, this bit has no effect.

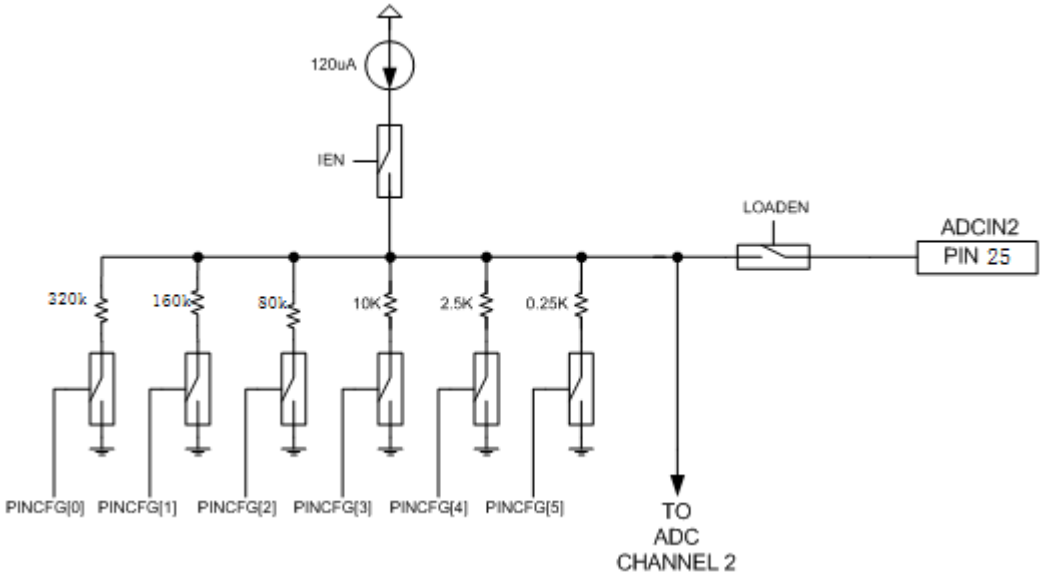
PIN16CFG (0x7E) Pin 16 BENN Configuration Register RW 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PECLP	PECLN	PDVEN	NDVEN	POL	FSEL1	FSEL0	-
WRITE	PECLP	PECLN	PDVEN	NDVEN	POL	FSEL1	FSEL0	DATAO

PELCP	Set this bit to connect pin 16 to + input of PECL input buffer
PECLN	Set this bit to connect pin 16 to - input of PECL input buffer
PDVEN	Set this bit to enable the PMOS drive in the CMOS output driver
NDVEN	Set this bit to enable the NMOS drive in the CMOS output driver
POL	POL controls the polarity of the output. Set this bit to 1 will inverse the output polarity
FSEL[1-0]	Select the function of the output. 00 = DATA OUTPUT 01 = MPDTHD, Laser Feedback Status output 10 = Burst Enable Status 11 = DCBTHD, Laser Drive Status output. This is set to 1 when DCBBIAS pin is higher than 2.4V and set to 0 when DCBBIAS is less than 2.4V. This can be used for light emitting indicator.
DATAO	When this pin is configured as CMOS output pin, MCU can write this bit to control the output.

4.5 Pin 25 (ADCIN2) Configurations

Pin 25 is connected to ADC's channel 2. It can be used for general ADC input measurements. In typical applications, this pin is used to connect to monitor output of PINTIA so input optical power can be measured. In typical applications, this requires a very large dynamic range for example from -40dBm to 0dBm. For a 1 A/W PIN, this corresponds to 0.1uA to 1mA. To achieve accurate measurement with such large dynamic range, an adjustable load is attached to Pin 25 to reduce the dynamic range required by ADC. This is shown in the following figure.



These resistors are built with on-chip unit resistors of 10K Ohm. A precision current reference of 120uA (generated from RREF external 10K Ohm) resistor can be switched on/off and can be used to calibrate the absolute value with these on-chip resistors. The control is through the following register. The default configuration of Pin 25 is no-connection.

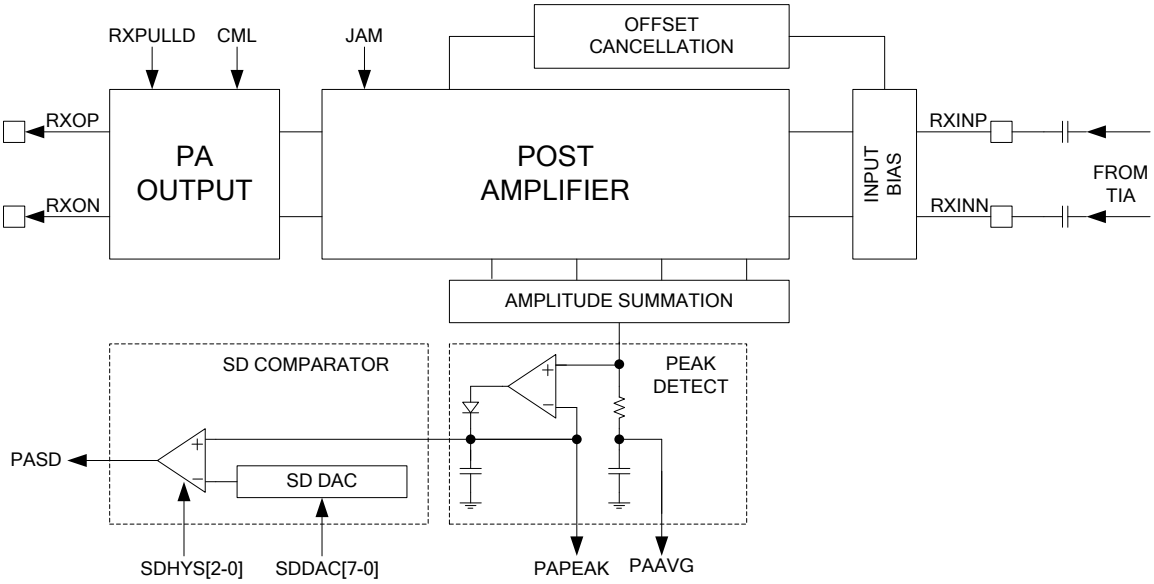
PIN25CFG (0x7F) Pin 25 Configuration Register RW 0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	LOADEN	IEN	CFG[5]	CFG[4]	CFG[3]	CFG[2]	CFG[1]	CFG[0]

WRITE	LOADEN	IEN	CFG[5]	CFG[4]	CFG[3]	CFG[2]	CFG[1]	CFG[0]

5. Post Amplifier and Receive Path

The post amplifier is a limiting amplifier that receives the AC coupled differential signals from PIN-TIA. The PA has 4 stages of amplifications offers more than 50dB gain from input to output. The input sensitivity is less than 2mV and typical bandwidth of 2GHz. Due to the high gain nature of the PA, on-chip offset compensations is required to cancel any offset that may saturate the gain stage. The offset cancellation circuit also provides DC bias to the input differential pins RXINP and RXINN through 10K resistor. Due to this internal bias, RXINP and RXINN must be AC coupled to PIN-TIA through capacitors. Note the lower 3-dB cut-off frequency is determined by the coupling capacitor and the internal bias resistor. The block diagram of the post amplifier is shown in the following figure.



The signal detect level is set by the register SDDAC[7-0], and the hysteresis of SD is set by the register SDHYS[2-0]. The relationship of the setting versus the SD level and hysteresis is shown in the following plots. SDDAC and SDHYS registers can be updated by MCU with temperature compensated value during normal operation. PA outputs the SD status on PASD signal which can be read by MCU on ANASTATUS register. PASD can be configured to pass directly onto LOS pin through PIN3CFG register. The polarity of the LOS state can also be configured using PIN3CFG. This configuration can be found in detail at the description of PIN3CFG register. The outputs of post amplifier are RXOP and RXON pins. The output can be configured with or without internal pull-down current sources. The detailed description on these configurations is in PACFG register.

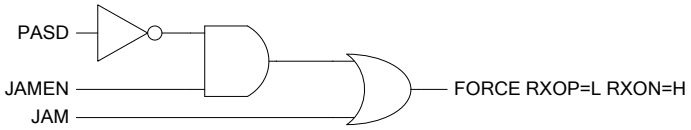
PACFG (0x53) PA configuration register R/W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PAPD	JAM	JAMEN	TEMPSEL	ASL	SDHYS[2]	SDHYS[1]	SDHYS[0]
WRITE	PAPD	JAM	JAMEN	TEMPSEL	ASL	SDHYS[2]	SDHYS[1]	SDHYS[0]

PAPD Receive Path Power Down. Set this bit to 1 will power down the receive circuits.

JAM This is software JAM control. Set this bit to 1 will force RXOP and RXON at a fix state of RXOP=L and RXON=H. Set this bit to 0 for normal receive operation.

JAMEN This is hardware JAM control enable. Set this bit to 1 use the PASD (0X5F) status to force RXOP=L and RXON=H. JAM and JAMEN function is shown in the following diagram.



TEMPSEL This bit is used to select which internal temperature is used. Setting this bit to 1 will select the positive temperature coefficient Bandgap reference. Setting this bit to 0 will select the internal PNP diode with negative temperature coefficient.

ASL Set this bit to 1 will reduce RXOP and RXON output amplitude by 25%. Set this bit to 0 will make RXOP and RXON as normal CML swing.

SDHYS[2-0] This three bits set the signal detect hysteresis level. Please note the hysteresis also depends on the SD level setting. Hysteresis is not very dependent on the temperature. The following table shows the relationship of SDHYS setting to the typical Hysteresis using typical ROSA. SDHYS[2] must be set to 0.

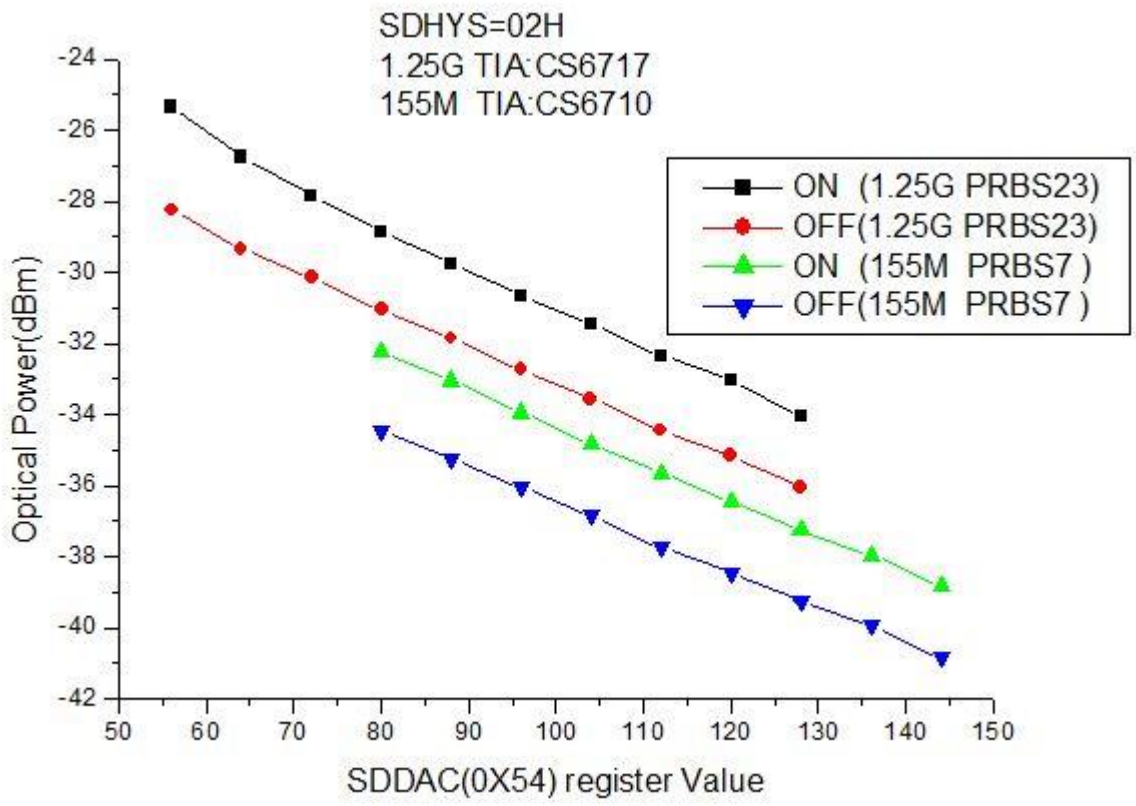
SDHYS[2-0]	Hysteresis (@-30dBm)
000	1.0dBm
001	1.5dBm
010	2.0dBm
011	2.7dBm

SDDAC (0x54) PA SD Level Setting

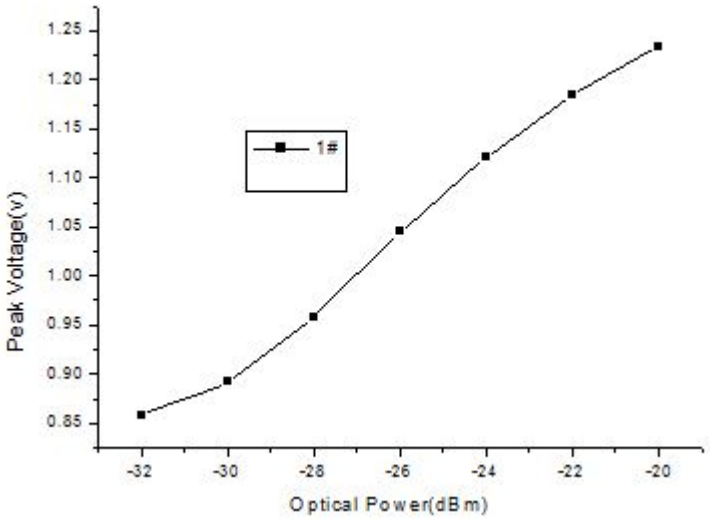
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	SDDAC7	SDDAC6	SDDAC5	SDDAC4	SDDAC3	SDDAC2	SDDAC1	SDDAC0
WRITE	SDDAC7	SDDAC6	SDDAC5	SDDAC4	SDDAC3	SDDAC2	SDDAC1	SDDAC0

This register set the signal detect level of the post amplifier.

The following two graphs show the typical SD level against SDDAC[7-0] setting using 0.9A/W 1.25G PIN-TIA of CS6717 with typical differential trans-impedance of 50KOhm with SDHYS[2-0] = 010, and a 155M PIN-TIA of CS6710 with typical differential trans-impedance of 100KOhm with SDHYS[2-0] = 010. In practical design, the proper SDDAC register setting will depend on the specific PIN-TIA used, and thus should be calibrated to its trans-impedance with temperature compensation during design phase.



PA also has one analog signal output, PAPEAK which can be fed into on-chip ADC. MCU can use this ADC reading to determine more precise signal detect level and combining another ADC input channel receiving PIN-TIA monitor current output, accurate optical input power can be calculated and flexible LOS status can be determined. It is also possible to use these two values to determine the input optical power level at low input range. A typical ADC reading converted to analog level using 0.9A/W PIN-TIA of m is shown in the following graph. From this graph, it can be seen that it presents a very accurate reading of input optical power at low power range.



6. LD Driver and Transmit Path

The LD driver is composed of several blocks that provide DC bias as well as modulation currents to the laser diode. The complete transmit path including both DC bias and modulation output is configured by LDCFG register.

LDCFG (0x55) LD Driver Configuration Register R/W (0x00100000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	TXPD	FAULT	CONT	MPDHYS2	MPDHYS1	MPDHYS0	DCBS1	DCBS0
WRITE	TXPD	FAILLATEN	CONT	MPDHYS2	MPDHYS0	MPDHYS0	DCBS1	DCBS0

TXPD — Set this bit to 0 for normal transmit path operation. Set this bit to 1 will power down the entire transmit path. Please note when CONT=1, the Pin 15 can function as TX_DISABLE, and it can also power down the transmit path.

FAULT — When read, this reflects the FAULT output status. The FAULT is the combinations of three fault conditions – DCBFAIL, MPDFAIL and APCFAIL (see PIN 5 Configuration description). Software can read this flag and update the corresponding I^2C SRAM for MSA requirement.

FAILLATEN — FAILLATEN=1 will cause DCBFAIL, MPDFAIL, APCFAIL to latch once it is asserted. If FAILLATEN=0, then these fail flags are not latched.

CONT — Set this bit to 1 for continuous mode operation. And set this bit to 0 for burst mode operation.

In continuous mode, Pin 15 can be configured as TX_DISABLE function. Whether it is positive asserted or negative asserted can be controlled by pin 15's polarity control. And the TX enable signal is just a hardware TXPD equivalent, when it is de-asserted, the entire transmit path is turned off and powered down.

MPDHYS[2-0] — These three bits controls the MPD comparators hysteresis. The hysteresis is reflected by the two MPD comparator output, MPDCMPU and MPDCMPD status bits.

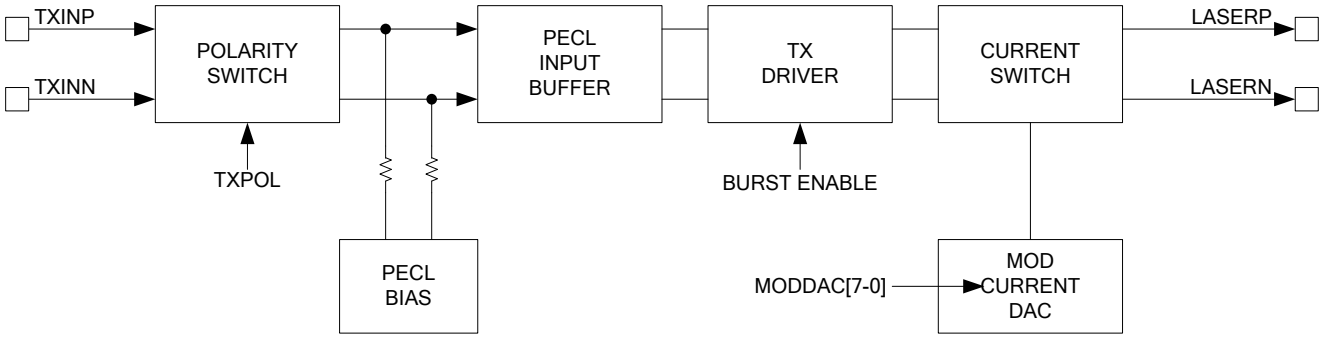
MPDHYS[2-0] = 000, HYS = 50mV
MPDHYS[2-0] = 001, HYS = 100mV
MPDHYS[2-0] = 010, HYS = 150mV
MPDHYS[2-0] = 011, HYS = 200mV
MPDHYS[2-0] = 100, HYS = 250mV
MPDHYS[2-0] = 101, HYS = 300mV
MPDHYS[2-0] = 110, HYS = 350mV
MPDHYS[2-0] = 111, HYS = 400mV

DCBS[1-0] — These two bits set the scaling factor of the DCB DAC output.

DCB[1-0] = 00 for DCBDAC full scale at 100mA.
DCB[1-0] = 01 for DCBDAC full scale at 75mA.
DCB[1-0] = 10 for DCBDAC full scale at 50mA.
DCB[1-0] = 11 for DCBDAC full scale at 25mA

6.1 Modulation Path

The modulation path provides the AC drive to the laser diode. It receives TXINP and TXINN inputs as differential PECL level. TXINP and TXINN are internal biased by PECL threshold. The polarity of TXINP and TXINN can be can be programmed by TXPOL setting. The outputs of PECL input buffer are sent to pre-driver of the modulation switch and provide a switched current source to LASERP and LASERN. The block diagram is shown as following.

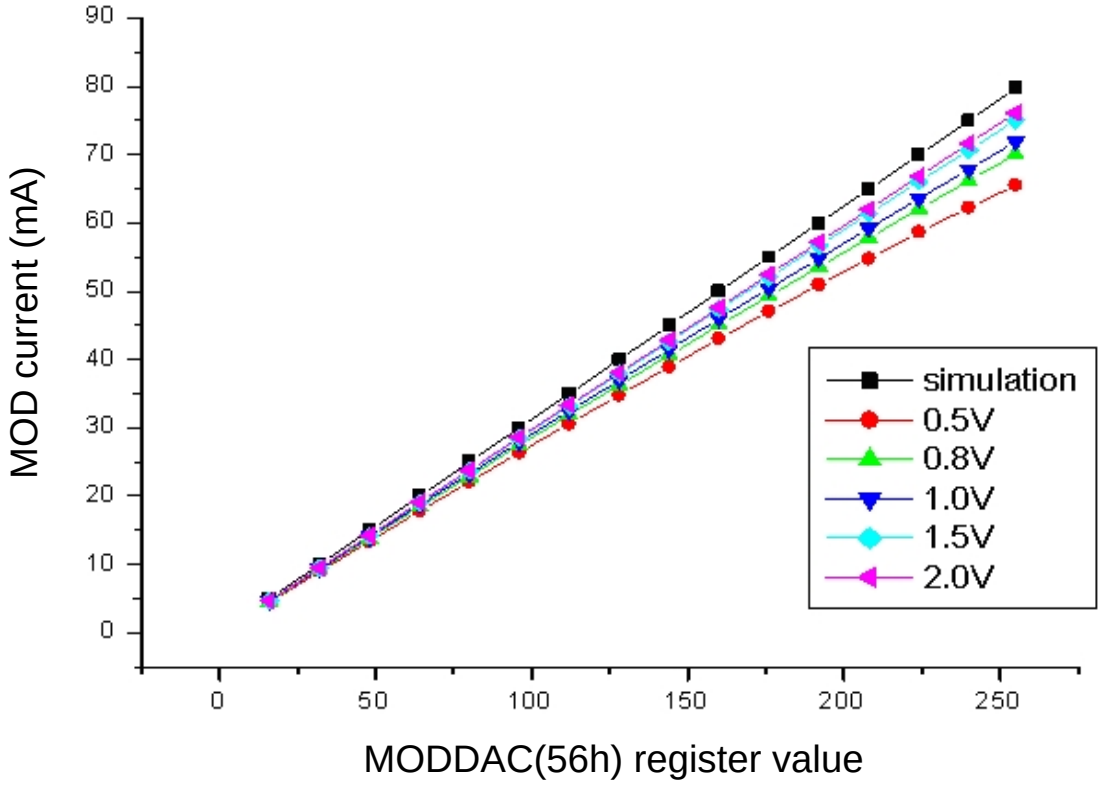


The modulation path is also controlled by the burst enable signal (see BENP and BENN pin description in the above section). When burst is on, the modulation path is turned on and LASERP and LASERN are driven by TXINP and TXINN signals. When burst enable is low, the modulation output forces LASERP to be connected to low (i.e. connected to the modulation current source), and disconnects LASERN. The modulation current level is set by MODDAC register as described in the following.

MODDAC (0x56) **Modulation Current Setting Register R/W (0x00000000)**

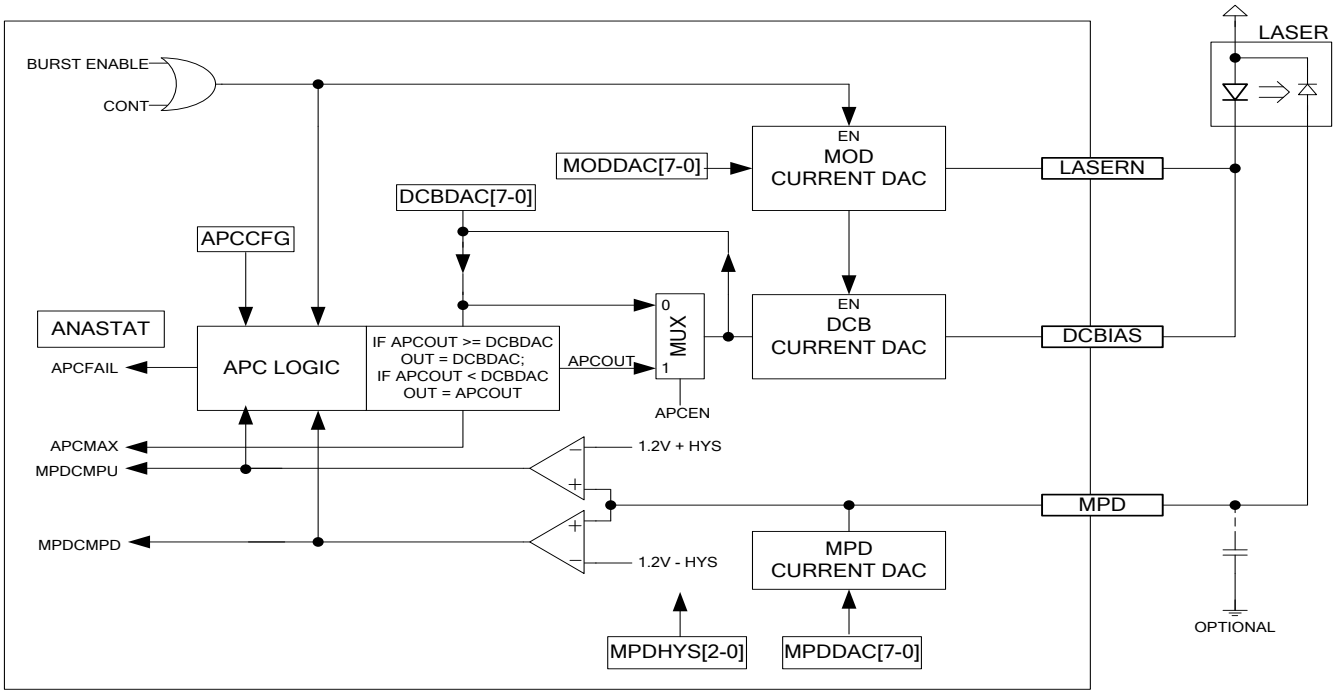
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	MODDAC[7-0]							
WRITE	MODDAC[7-0]							

The modulation programmable range is from 0mA to 80mA corresponding to MODDAC = 0 to MODDAC = 0xFF. Each step size of MODDAC is 0.3125mA. The relationship between MODDAC settings versus modulation output current is shown in the following graph. This graph also shows the output current dependence of the output voltage. It can be seen that the setting is relative linear if output voltage is maintained above 0.8V. This allows DC coupling of modulation current possible for most typical Laser Diodes.



6.2 DC Bias Path

The DC bias current of the laser is output on DCBIAS pin. The block diagram of the DC bias control is shown in the following diagram.



The simplest way for continuous mode laser operation (set CONT = 1 in LDCFG) is to use software open loop control by setting APCEN=0 (in the APCCFG register) which disable the APC logic. In this configuration, software has full control of DCBDAC. For power monitoring feedback control, the laser power monitoring is fed back to MPD pin. Software can set the MPDDAC to determine the target laser monitor current, and read the comparator output. CS6721 implemented two comparators on MPD pin with programmable thresholds. The space between the two thresholds is set by MPDHYS[2-0] in LDCFG. The compared status is read from ANASTATUS as MPDCMPU and MPDCMPD bits. The programmable thresholds of these two comparators can be used as hysteresis and thus prevent step oscillation in the feedback control loop.

DCBDAC (0x58) **DC BIAS Current Setting Register R/W (0x00000000) (DCBSEL=0)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	DCBOUT[7-0]							
WRITE	DCBDAC[7-0]							

DCBMAX (0x58) **DC BIAS MAX Current Setting Register W (0x00000000) (DCBSEL=1,MNSEL=1)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	DCBOUT[7-0]							
WRITE	DCBMAX[7-1]							MNSEL=1

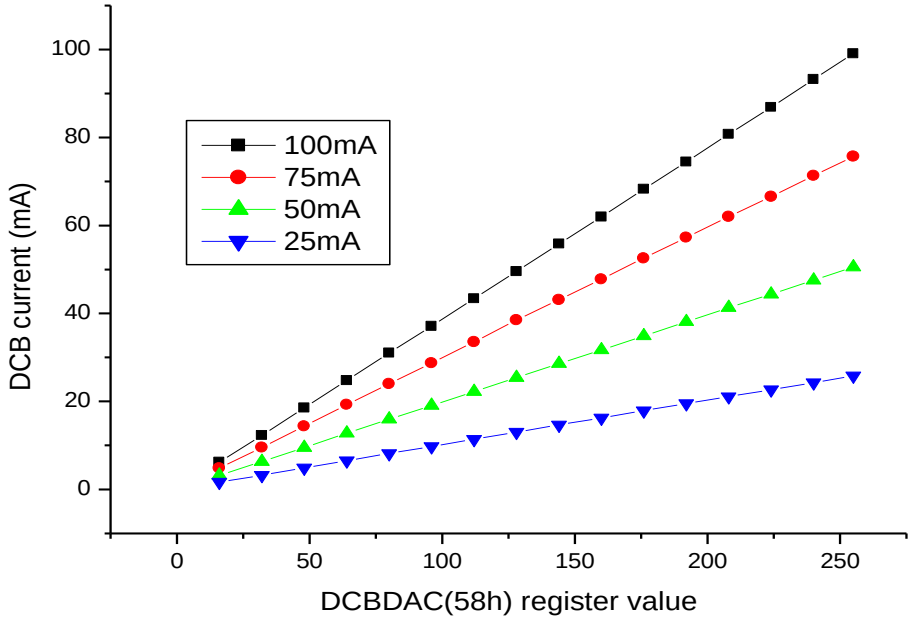
DCBMIN (0x58) **DC BIAS MIN Current Setting Register W (0x00000000) (DCBSEL=1, MNSEL=0)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	DCBOUT[7-0]							
WRITE	DCBMIN[7-1]							MNSEL=0

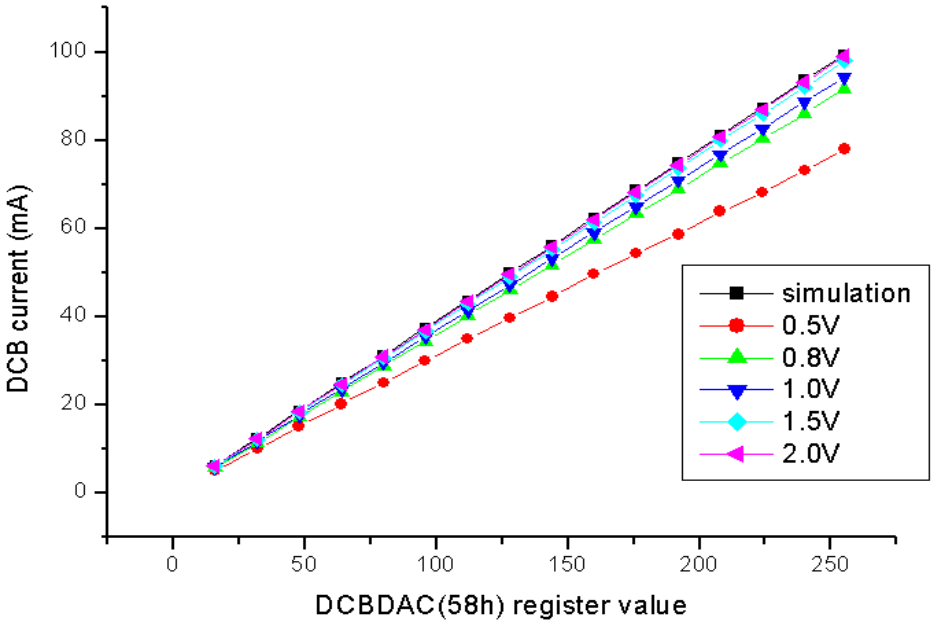
0x58 is a multi-function register address that when read out always obtain the present DCB DAC output current value. When written, it can write into DCBDAC, or DCBMIN or DCBMAX depending on DCBSEL and MNSEL setting.

If DCBSEL=0, then write into DCBDAC value. This is by setting DCBSEL(0x59) to 0. When DCBSEL=1, DCBDAC0 will be used to set DCBMAX (MNSEL=1) or DCBMIN (MNSEL=0).

Each LSB of DCBDAC is 0.39mA/DCBS[1-0] (defined in LDCFG), depending on DCBS setting, the full range can be set as 100mA, 75mA, 50mA, and 25mA. The relationship of DCBDAC and DCB output current is show in the following graph according to different DCBS setting.



The absolute DCB current output has slight dependence on the laser diode drop. The following graph shows the output current versus the output voltage. And it can be seen that as long as maintaining the output voltage higher than 0.8V, the current is relatively stable.



MPDDAC (0x57) **Monitor Photo Diode Current Setting Register R/W (0x00000000)**

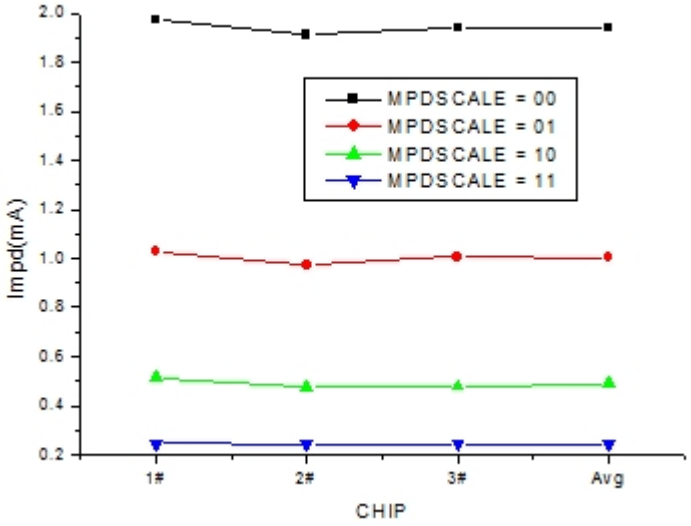
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	MPDDAC[7-0]							
WRITE	MPDDAC[7-0]							

MPDTXP (0x57) **Monitor Photo Diode Current Value Register RO (0x00000000)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	MPDTXP[7-0]							
WRITE	MPDDAC[7-0]							

0x57 is a multi-function register address. When written, it always writes into MPDDAC which is the setting of MPD feedback current for APC loop. When read, it read out either MPDDAC value or MPDTXP value depending on MPDSEL bit in APCCFG register.

MPDDAC controls the current source at MPD pin. When APC is enabled, the APC as a feedback loop will balance this current source with the monitor current from the laser diode. In reality, the close loop will force the MPDDAC current source to be equal to the monitor current by automatically adjusting the DCB output and thus maintaining a constant laser optical output power. The following graph shows the typical measurements on full range of the MPDDAC at different MPDSCALE (0x5F) setting.



MPDTXP is a read only register. It reflects the close approximation of the laser monitor feedback current. MPDTXP can be used in close loop configurations. Please note, although in closed loop application, the feedback monitor current will be approached to MPDDAC by the loop action, however, it dose not necessary equals to each other because of the loop time constant. This is especially true if the laser operates under burst-mode. MPDTXP approximate the feedback monitor current burst by burst when it burst-mode, and will also work under continuous mode. To use MPDTXP function, the **MPDMREN** bit in DACDATH (0x5D) must be turned on too as this bit controls the current replica circuit in MPD path.

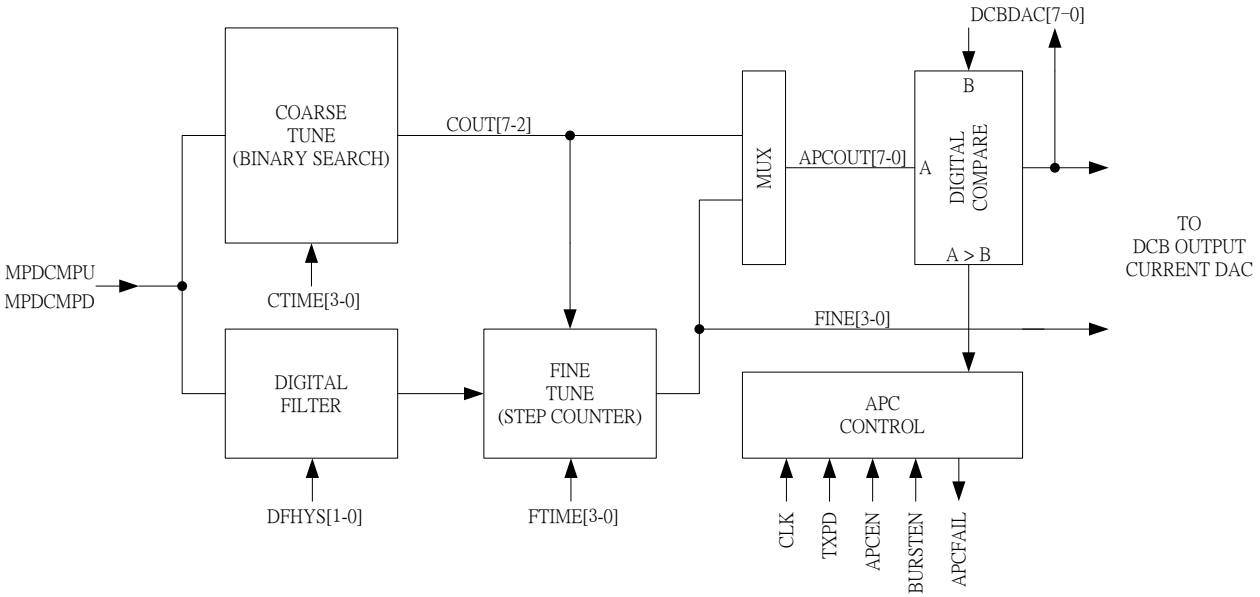
6.3 Automatic Power Control

The open-loop software control can only be used for continuous mode laser operation. For burst-mode driver, hardware APC logic must be selected as the power adjustment must be achieved in very short time at the initial burst-on time, and following fine adjustment needs to be done burst to burst basis to avoid power adjustment during transmission. For burst-mode applications such as PON, hardware APC must be used because the laser is not

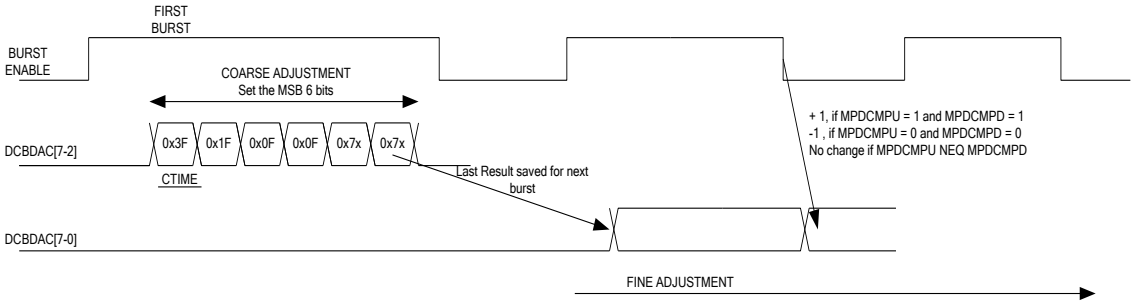
constantly on and the adjustment of laser DCB bias must be done during the burst on is described in detail as following block diagram.

CS6721 implementation includes hardware control logic (APC Hardware) that can be used for both continuous and burst mode operations. The software needs to perform the set up steps by

1. Set up related APC control parameters including LTIME[4-0] (0x59), DFHYS[1-0] (0x59), CTIME[3-0] (0x5F), and FTIME[3-0] (0x5F).
2. Then turn on transmit path (TXPD=0) and set APCEN=1
3. Set the DCB current scaling factors DCBS[1-0], and set the maximum DCB current by writing the maximum value to DCBDAC.
4. Set the monitor feedback current by writing MPDDAC, and MPD comparator hysteresis control MPDHYS[2-0]
5. Set the modulation current by writing to MODDAC
6. The APC hardware logic uses two stages of power control. One is coarse control which is carried out first and uses binary search to get the power setting to an approximation to the target value in 6 steps (each step is separated by CTIME). The coarse adjustment only changes the most significant 6-bit of DCBDAC. Once coarse adjustment is done, it enters into fine adjust mode. The fine adjustment is done periodically defined by FTIME, or at each burst end. When burst is turned on, the APC logic load the previous stored DCBDAC value and use it as the output current. Then wait for CTIME and start monitoring MPDCMPU and MPDCMPD. The MPDCMPU and MPDCMPD are fed into a signed 10-bit counter (loaded with 0x000) clocked by SYSCLK, and the counter is increment by 1 if MPDCMPU = 1 and MPDCMPD=1, or no change if MPDCMPU = 0 and MPDCMPD=1, or decrement by 1 if MPDCMPU = 0 and MPDCMPD=0. The counter value is checked at either the end of burst or FTIME expiration whichever occurs earlier against the MPDHYS setting. If the count value is larger than MPDHYS, the DCBDAC is incremented by 1, or if the count value is less than –MPDHYS, the DCBDAC is decrement by 1, or DCBDAC remains unchanged if the count value is within MPDHYS. The new DCBDAC is updated and is used for next burst on initial value. In general, FTIME is set longer than the maximum burst time. Therefore, the fine adjustment does not change during the burst on time. In stead the newly adjusted value of DCBDAC is applied at the next burst-on. This avoids changing of laser setting during actual transmission. The following diagram shows the detail functional block of APC hardware.



The following timing diagram shows a typical burst-mode operation of APC adjustment.



Using APC hardware, the laser power can approach to the final target within the first burst on time (6 CTIME). After the coarse adjustment is done, the fine adjustment occurs at the end of the burst each adjustment is 1/16 of LSB of the DCBDAC. The power setting of the laser never occurs during the laser on period if FTIME is set longer than the maximum burst time.

APCCFG (0x59) **APC Configuration Register R/W (0x00000000)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	APCEN	DCBSEL	DCBFAIL	BCEN	MPDSEL	LTSEL	DFHYS1	DFHYS0
WRITE	APCEN	DCBSEL	FAILSELC	BCEN	MPDSEL	LTSEL	DFHYS1	DFHYS0

APCEN Set this bit to 1 to allow hardware APC. Set this bit to 0 for open-loop or software control of laser power.

DCBSEL This bit defines whether DCBDAC or DCBMAX/DCBMIN will be operated on when access to 0x58. If this bit is set, then the writing 0x58 is referenced to DCBMAX[7-0]/DCBMIN[7-0]. If this bit is 0, then writing 0x58 is referenced to DCBDAC[7-0].

DCBFAIL This bit is the abnormal status of DCBIAS pin voltage. The DCBFAIL is asserted when DCBIAS pin has voltage lower then 1/6 VDDH or higher than ¾ VDDH. In general, this indicates some failure in the laser bias or failure in the laser diode. In burst-mode, DCBFAIL is sampled only during burst on durations.

If FAILLATEN=0, DCBFAIL is the real time status. If FAILLATEN=1, an assertion will cause DCBFAIL be latch 1. The latched DCBFAIL bit is cleared by any write “1” operation into FAILSELC bit. The latched DCBFAIL is also cleared by any assertion of TX Power Down conditions including assertion of TX_DISABLE pin or assertion of TXPD register bit.

FAILSELC Set this bit to 1 will enable DCBFAIL as a FAIL condition. Writing this bit 1 will also clear the latched DCBFAIL status if FAILLATEN=1. FAILSELC=0, DCBFAIL still operates the same but just will not affect the FAULT output.

BCEN Set this bit will open the burst pattern counter function that the counter result can be read in A0(130~134) or B0(130~134). Host read A0 or B0 ADDR=129 will clear counter. Clear this bit to 0 will close this function. This bit will close this backdoor.

MPDSEL This bit defines whether MPDDAC or MPDTXP will be read when access to 0x57. If this bit is set, then the reading 0x57 is referenced to MPDTXP[7-0]. If this bit is 0, then reading 0x57 is referenced to MPDDAC[7-0].

LTSEL This bit defines whether LTIME or CTIME/FTIME will be written on when access to 0x5F. If this bit is set, then the writing 0x5F is referenced to LTIME[4-0]. If this bit is 0, then writing 0x5F is referenced to CTIME[3-0] and FTIME[3-0].

DFHYS[1-0] DFHYS set the digital filter of MPDCMPU and MPDCMPD. MPDCMPU and MPDCMPD are fed into a 8-bit counter as a digital filter. The 10 bit counter is first preload 7F and counts up/down or unchanged depending on the input value of MPDCMPU and MPDCMPD. The final count value (at the burst-end) is then examined to see if the total deviation is larger than DFHYS to determine if to increment/decrement or maintain the DCBDAC value.

The value of DFHYS ranges from 1 to 4 for CONT=0. If CONT=1 (considering the larger loop time of continuous mode applications), the value is multiplied by 16 becomes 16, 32, 48, or 64.

6.4 Laser Power Monitoring and Safety Warning

CS6721 also include circuits to monitor actual Laser power and as well as provide safety warning. The detection is independent of APC, and track real time status of the Laser output through MPD pin.

The optical power of the Laser is monitored by the built-in monitor photo diode in the Laser package. The output of the monitor diode, a current source, is feedback to MPD pin of CS6721. This current is used for APC that obtain a power locked loop that maintain a constant optical output power. The current is also mirrored to two independent current sources (enabled by MPDMREN in DACDATAH register).

One current source is sent to MPDTXP circuit that converts to an 8-bit digital value of the feedback current. This value can be read by program through MPDTXP register.

The other current source is sent to MPDTHD comparator for safety warning. The comparator result can be read at MPDTHD bit of ANASTATUS (0x5F). If desired, the status can also be outputted directly on PIN 16 by configuration of PIN 16 functions. Please refer to PIN 16 configuration description. The threshold of the comparator is controlled by MPDTHDATA (0x5E).

In order for power monitoring and warning detection to function, MPDMREN located at DACDATAH (0x5D) must be set to 1. The programming method of MPDMREN and MPDTHDATA is described in the DACDATAH register section.

6.5 Analog Status

To allow ease of programming, the status of post amplifier and LD driver are grouped in ANASTATUS register.

ANASTATUS (0x5F) Configuration Register RO (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PASD	MPDTHD	APCHOLD	MPDFAIL	APCFAIL	BENABLE	MPDCMPU	MPDCMPD
WRITE	CTIME[3-0]				FTIME[3-0]			

ANASTATUS (0x5F) Configuration Register W (0x00000000)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	PASD	MPDTHD	APCHOLD	MPDFAIL	APCFAIL	BENABLE	MPDCMPU	MPDCMPD
WRITE	-	MPDSCALE[1-0]		LTIME[4-0]				

PASD — This bit reflects PA's SD status. PASD is 0 when the input power is lower than SDDAC setting. PASD is 1 when the input power is higher than SDDAC setting.

MPDTHD — This bit reflects the MPD current comparator output. This bit is 1 when the feedback current is larger than the threshold current defined in MPDTHDDAC. This bit is 0 when the feedback current is smaller than the threshold.

APCHOLD — This bit is set by the APC hardware to indicate the coarse adjust result. APCHOLD is set to 1 by hardware when APC completed the coarse adjustment.

MPDFAIL — This bit is set to 1 by hardware if MPD Pin voltage falls into abnormal range. When APC is stable, MPD pin typically should be at 1.4V locked state. MPDFAIL is asserted when MPD pin is higher than 90% VDDH or lower than 10%VDDH. Usually this indicates an OPEN or SHORT laser feedback loop. In burst-mode, MPDFAIL is sampled only during burst on durations.

If FAILLATEN=0, MPDFAIL is the real time status. If FAILLATEN=1, an assertion will cause MPDFAIL be latch 1. The latched MPDFAIL bit is cleared by any write "1" operation into FAILSELA bit in ADCDATL register. The latched MPDFAIL is also cleared by any assertion of TX Power Down conditions including assertion of TX_DISABLE pin or assertion of TXPD register bit.

APCFAIL	This bit is set to 1 by hardware if APC cannot converge into a stable loop. APCFAIL is asserted when the APC loop is adjusting DCBDAC and hits the higher bound of DCBMAX and lower bound of DCBMIN (assertion is made after 4 counts of consecutive hits and any reverse direction will clear the count). In burst-mode, APCFAIL is sampled only during burst on durations. If FAILLATEN=0, APCFAIL is the real time status. If FAILLATEN=1, an assertion will cause APCFAIL be latch 1. The latched APCFAIL bit is cleared by any write "1" operation into FAILSELB bit in ADCDATL register. The latched APCFAIL is also cleared by any assertion of TX Power Down conditions including assertion of TX_DISABLE pin or assertion of TXPD register bit.
BENABLE	This bit reflects current internal burst enable state. BENABLE = 1 means the burst is on while BENABLE = 0 means the burst is off. In continuous mode, BENABLE will always read as 1.
MPDCMPU	This bit reflects the MPD comparator output. MPDCMPU = 0 means the input photo diode current is larger than MPDDAC setting.
MPDCMPD	This bit reflects the MPD comparator output. MPDCMPD = 0 means the input photo diode current is larger than MPDDAC setting.
MPDSCALE1/0	These two bits to select MPDDAC/MPDTXP/MPDTHD full range. (00=2mA, 01=1mA, 10=500uA, 11=250uA)

This register when written also sets the time steps of coarse & fine adjustment (LTSEL=0), and the initial feedback loop stable time (LTSEL=1).

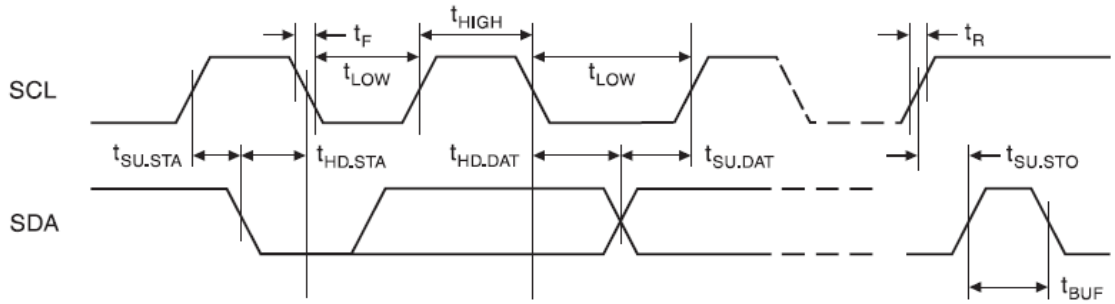
LTIME[4-0]	LTIMT[4-0] is used for delay compensation of the optical light feedback loop delay. The delay is (LTIME[4-0]) * T) where T is system clock period.
CTIME[3-0]	CTIME[3-0] is used for coarse time steps. The time between each step is (CTIME[3-0])+1) *T. Either CTIME expiration or burst end will update the coarse adjustment.
FTIME[3-0]	FTIME[3-0] is the time between each fine adjustment and is defined as (FTIME[3-0]) * 256T+T). Either FTIME expiration or burst end will update the fine adjustment.

The setting of these time constants depends on the operation modes of the module whether in continuous or burst-modes. Another two parameters will affect the time constants are DFHYS[1-0] in APCCFG, and MPDHYS[1-0] in LDCFG. DFHYS[1-0] is the setting for the digital filter of MPD comparator result, and MPDHYS[1-0] is the hysteresis setting of the two MPD comparators. For continuous mode, it is preferred that all these time constant to be large so a very stable loop can be obtained. For loop stability, a large decoupling capacitor must be added on MPD pin externally, and the time constants consisted by this capacitor should be the dominant pole of the loop. For burst mode, these time constants should be kept to minimum in the power up, so a fast acquisition of power can be obtained. Then FTIME should be set to longer than burst length for normal operation.

ELECTRICAL CHARACTERISTICS

I²C AC Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
fSCL	Clock Frequency	0	-	400	KHz	
tLOW	Clock Pulse Width Low	1.3	-	-	µs	
tHIGH	Clock Pulse Width High	0.6	-	-	µs	
tHD.STA	Start Hold Time	0.6	-	-	µs	
tSU.STA	Start Set-up Time	0.6	-	-	µs	
tHD.DAT	Data In Hold Time	0	-	0.9	µs	
tSU.DAT	Data In Set-up Time	100	-	-	ns	
tR	Rise Time of both HSDA and HSCL signals	-	-	300	ns	
tF	Fall Time of both HSDA and HSCL signals	-	-	300	ns	
tSU.STO	Stop Set-up Time	0.6	-	-	µs	
tBUF	Time the bus must be free before a new transmission can start	1.3	-	-	µs	



Absolute Maximum Ratings

SYMBOL	PARAMETER	RRATING	UNIT
VDD	Positive Power Supply	3.6	V
TA	Ambient Operating Temperature	-40 to 85	°C
TSTG	Storage Temperature	-65 to 150	°C

Recommend Operating Condition

SYMBOL	PARAMETER	RRATING	UNIT
VDD	Positive Power Supply	3.0 to 3.6	V
TA	Ambient Operating Temperature	-40 to 85	°C

DC/AC Electrical Characteristics VDD = 3.0V to 3.6V, TA = -40°C to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Power Supply Current						
IDD, VDDD	Supply Current Standby (RXPD=TXPD=1)	-	15	20	mA	1
IDD, VDDR	Supply Current Receive Only (RXPD=0, TXPD=1)	-	65	75	mA	2
IDD, VDDRO	Supply Current Transmit Only (RXPD=1, TXPD=0,	-	35	40	mA	3

	MODDAC=DCBDAC=00)					
IDD, VDDT	Supply Current Receive and Transmit Active (MODDAC=DCBDAC=00)	-	85	100	mA	4
Digital IO Characteristics						
VOH	IOH = 1mA	VDD-0.5	-	VDD	V	
VOL	IOL = 4mA	0	-	0.5	V	
IIN	Input Current	-50	0	50	uA	
Internal 1.8V Regulator						
V_{DD18}	Internal 1.8V regulator output	1.6	1.8	2.0	V	5

Note 1. Measured through VDDD pin at 12.5MHz clock rate.
2. Measured through VDDR pin.
3. Measured through VDDRO pin including load current of two external 120 Ohm pull down resistors.
4. Measured though VDDT pin at 10Mbps rate. Does not include any load current.
5. Internal regulator output on CFIL pin. This regulator can be trimmed by register setting.

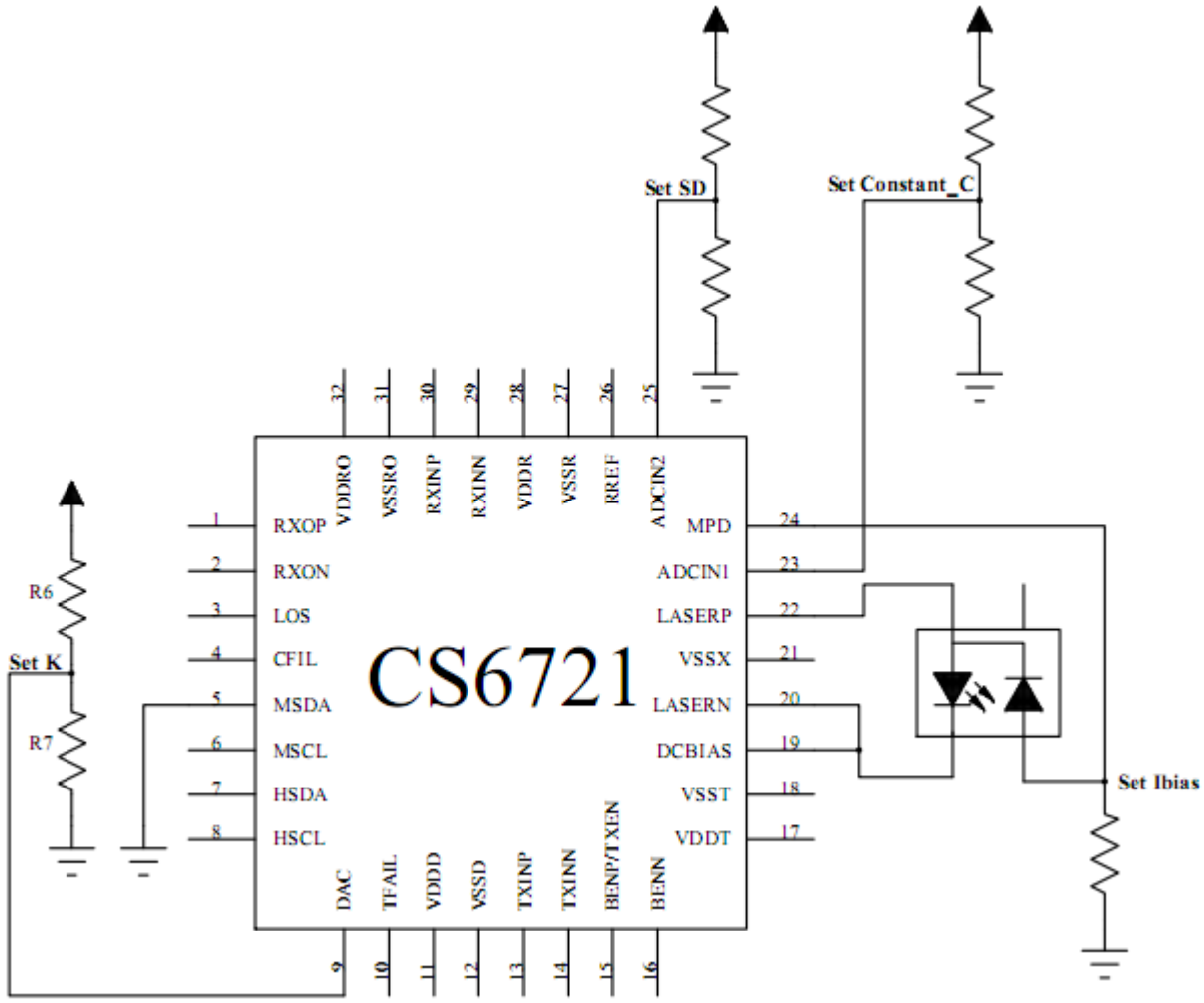
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Post Amplifier						
V, In	Input Sensitivity at 2.5Gbps	6	4	2	mV	Differential
V, Out	Differential Output Swing	640	800	960	mV	RXOP/RXON ASL=0
T, Rise/Fall	Output Rise/Fall Time	-	100	150	psec	
F, 3dB High	Bandwidth	1800	2000	2200	MHz	
F, 3dB Low	Low Cut-Off Frequency	-	50	100	KHz	
VIN, HYS	Hysteresis, Electrical	-	1.0	-	dB	HYS=00
LD Driver						
V, In, Swing	Differential Input Swing	600	1200	1800	mV	TXINP/TXINN
V, In, V_{CM}	PECL Input Common Voltage	Vcc-1.4	Vcc-1.3	Vcc-1.2	V	TXINP/TXINN
I, DCB	DCB Bias Current Range	1	40	100	mA	
I, MOD	MOD Current Range	4	35	80	mA	
T, Rise/Fall	Output Rise/Fall Time	50	80	120	nsec	Electrical
T, Ben	Burst Enable and Disable time	2	3	6	nsec	Electrical
V, Out	Minimum Output Voltage at DCB and LASERP, LASERN	0.8	1.0	-	V	
I, MPD	MPD Input Current Range	-	-	2.5	mA	
V, MPD	MPD Input Voltage	-	1.2	-	V	
Internal Oscillator						
F, OSC	Oscillator Frequency	15	25	35	MHz	
Analog To Digital Converter						
ADC, RES	Resolution	-	12	-	Bit	
ADC, Range	Input Full Scale	-	1.8	-	V	
ADC, INL1	Linearity Accuracy	-4	-	4	LSB	Note1
ADC, DNL1	Linearity Differential	-2	-	2	LSB	Note1
ADC, INL2	Linearity Accuracy	-10	-	10	LSB	Note2
ADC, DNL2	Linearity Differential	-4	-	4	LSB	Note2
ADC, CONV	Conversion Time		14T	-		T=80nsec

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Digital To Analog Converter						
DAC, RES	Resolution	-	10	-	Bit	
DAC, Range	Output Full Scale	-	1.8	-	V	
DAC, Source	Source Impedance	-	10K	-	Ohm	

Note 1: For VDD-0.4V to 0.4V range.
Note 2: For VDD toVDD-0.4V and 0.4V to 0V range

APPLICATION (NON-EEPROM) DIAGRAM

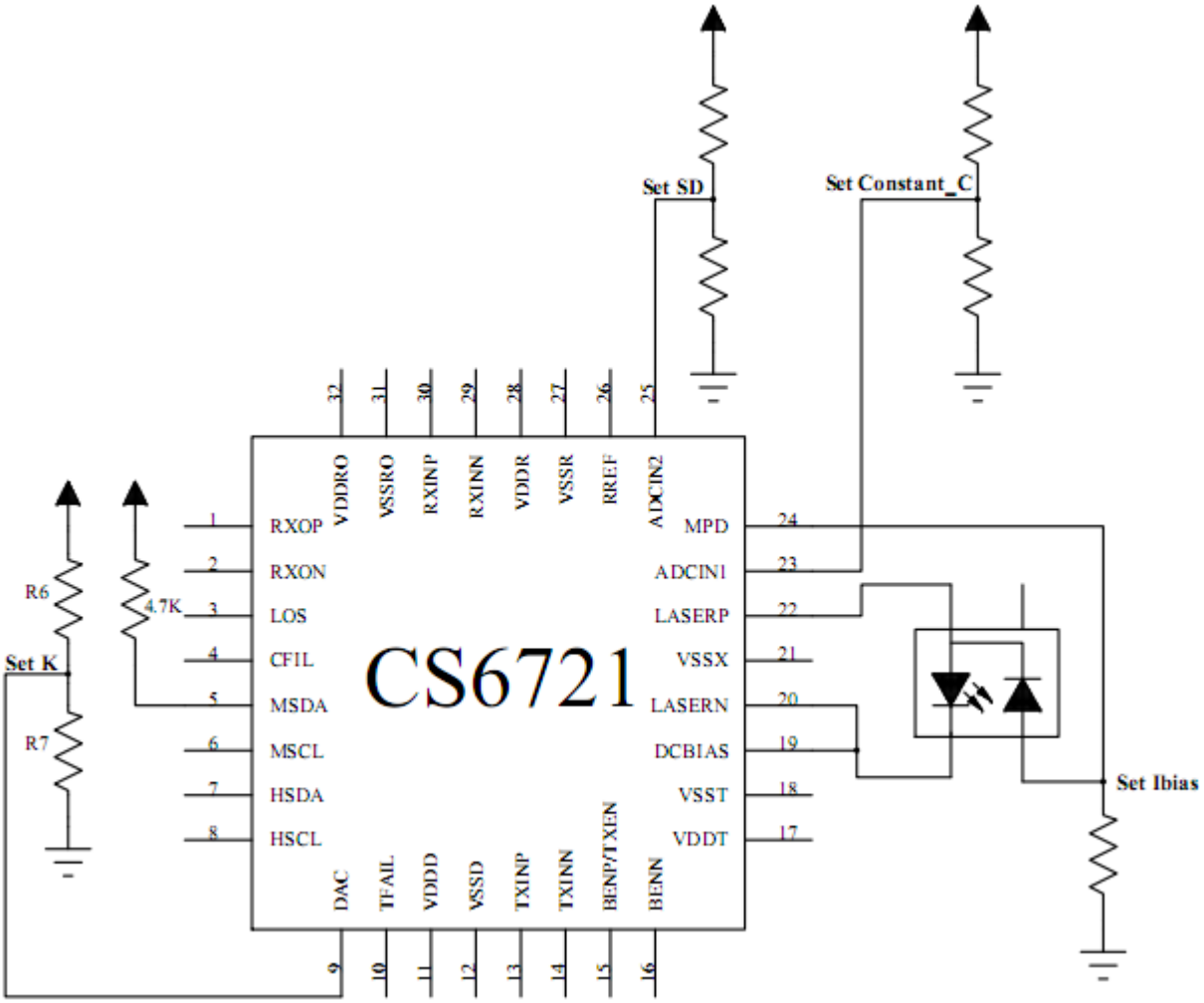
1. SFP Module Application without EEPROM (Romsel = 1): MSDA pin must be connected to GND.



MODDAC = K_{ratio}*DCBOUT/256 + Constant_C

	R6= NC R7=10K	R6=100K+ R7=NC	R6=39K R7=NC	R6=18K R7=NC	R6=13K R7=NC	R6≤4.7K R7=NC
K	0	144	112	96	80	48

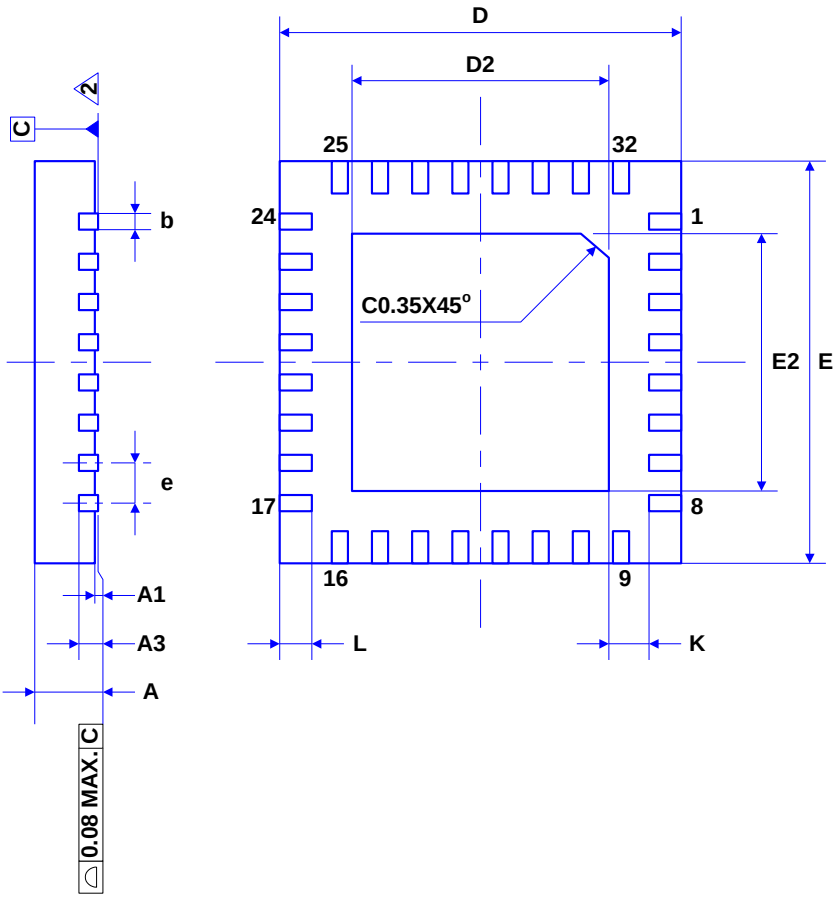
2. EPON Module Application without EEPROM(Romsel = 1)



MODDAC = K_{ratio}*DCBOUT/256 + Constant_C

	R6= NC R7=10K	R6=100K+ R7=NC	R6=39K R7=NC	R6=18K R7=NC	R6=13K R7=NC	R6≤4.7K R7=NC
K_{ratio}	0	144	112	96	80	48

PACKAGE OUTLINE
32-pin QFN



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e	0.50 BSC.		
L	0.35	0.40	0.45
K	0.20	-	-

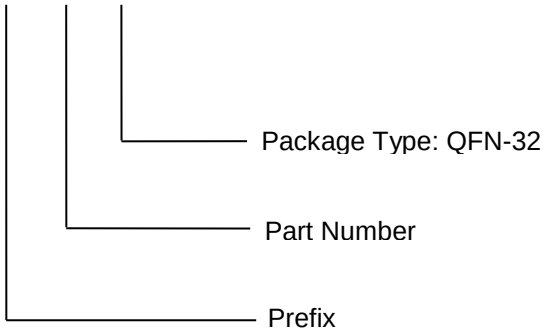
	Dimensions in Millimeters					
	D2			E2		
EXPOSED PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
2.7X2.7	2.60	2.70	2.80	2.60	2.70	2.80

Notes:
1. JEDEC Outline: N/A.
2. Dimension b applies to metal terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. The minimum “K” value of 0.20mm applies.
4. Bilateral co-planarity zone applies to the exposed heat sink slug as well as the terminals.

ORDERING INFORMATION

Prefix	Part Number	Package Type	Remark
CS	6721	W: 32-pin QFN	

Example: **CS 6721 W**



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