FUJITSU MICROELECTRONICS
DATA SHEET

DS04-27264-1E

ASSP for Power Management Applications (Rechargeable Battery)

DC/DC converter IC for Charging Li-ion battery

MB39A134

■ DESCRIPTION

The MB39A134 is a DC/DC converter IC for charging Li-ion battery, which is suitable for down conversion, and uses pulse width modulation (PWM) for controlling the charge voltage and current independently. This IC contains the build-in comparator for the voltage detection of the AC adapter independent from DC/DC converter control part, and selects the AC adapter or battery power automatically for voltage source supplying to the system.

MB39A134 provides a wide range of input voltage, low current consumption at standby, and high accuracy in charge current/voltage, which makes them suitable for a built-in charging device in products such as notebook PC.

■ FEATURES

- Support 2, 3 and 4 Cell Battery Pack
- Built-in two constant current control loops
- Built-in AC adapter detection function (ACOK pin)
- Charge voltage accuracy : ±0.7% (Ta = −10 °C to +85 °C)
- Built-in charging voltage control without external setting resistor (4.20 V/Cell or 4.10 V/Cell)
  Adjustable to charge voltage with external resistor
- Built-in two high accurate current detection amplifiers (±1%) (At input voltage difference 100 mV)
  (±5%) (At input voltage difference 20 mV)
  Input offset voltage : 0 mV (Current Amp1)
  : +3 mV (Current Amp2)
- Built-in Charging Current Control without external resistor (R_S = 20 mΩ : 2.85 A)
  Adjustable charging current with external resistor
- Setting of switching frequency using an external resistor
  (Frequency setting capacitor integrated) : 100 kHz to 2 MHz
- Built-in under voltage lockout protection
- In standby mode (Icc = 6 µA Typ) , only AC adapter detection function is operated
- Built-in VH regulator for reducing Qg loss of P-ch MOS FET
- Package : TSSOP-24

■ APPLICATIONS

- Built-in charger for Notebook PC
- Handy terminal device etc.

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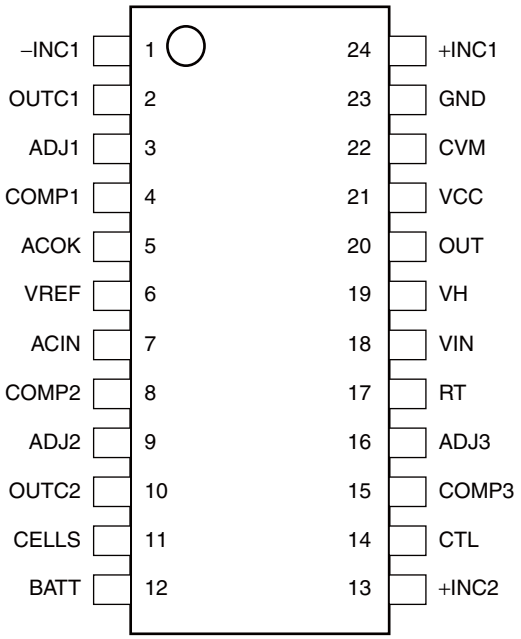
■ PIN ASSIGNMENT

(TOP VIEW)

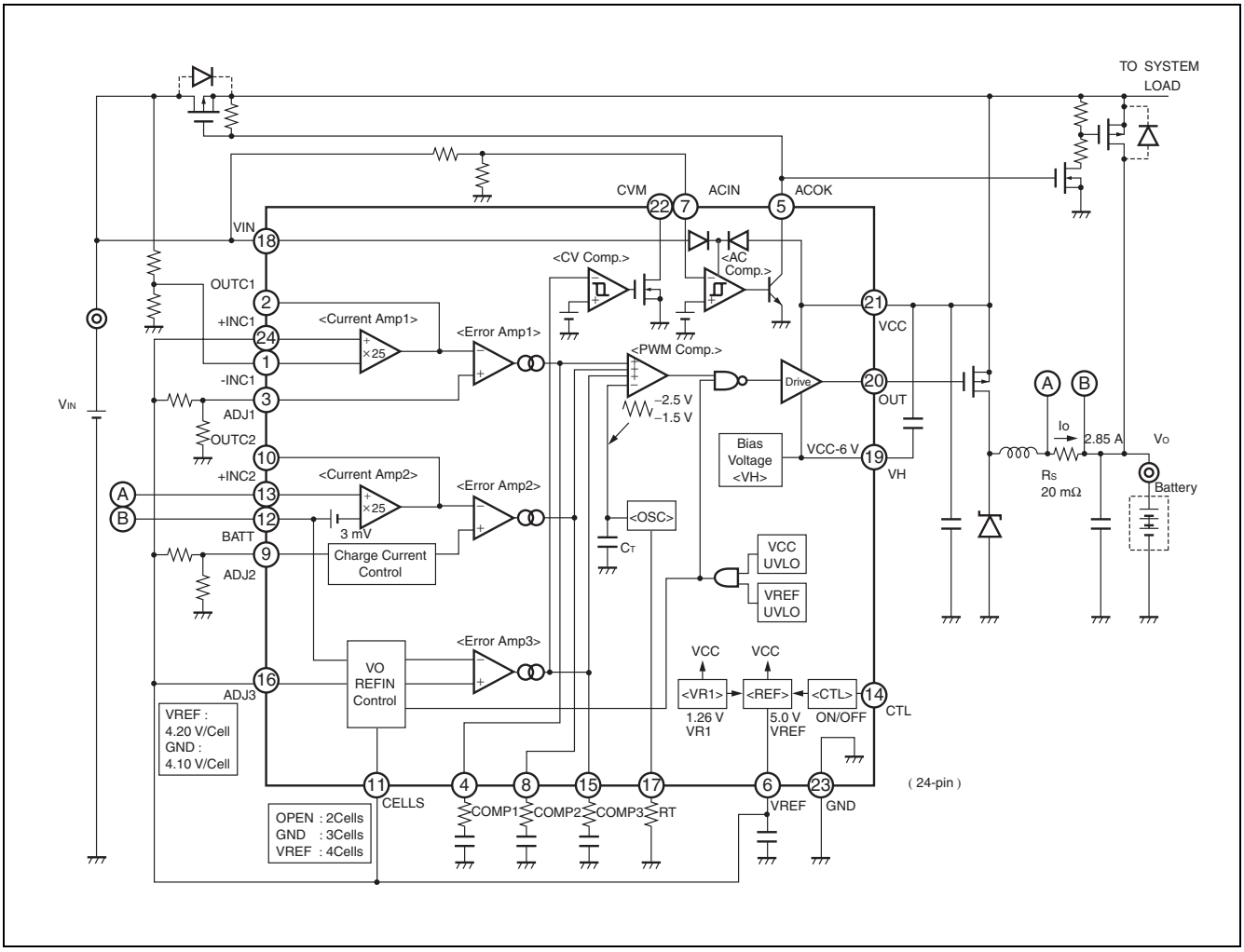


(FPT–24P–M08)

■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	-INC1	I	Current detection amplifier (Current Amp1) inverted input pin.
2	OUTC1	O	Current detection amplifier (Current Amp1) output pin.
3	ADJ1	I	Error amplifier (Error Amp1) non-inverted input pin.
4	COMP1	O	Error amplifier (Error Amp1) output pin.
5	ACOK	O	AC adapter voltage detection block (AC Comp.) output pin. ACIN = H : ACOK = Lo-Z, ACIN = L : ACOK = Hi-Z
6	VREF	O	Reference voltage output pin.
7	ACIN	I	AC adapter voltage detection block (AC Comp.) input pin.
8	COMP2	O	Error amplifier (Error Amp2) output pin.
9	ADJ2	I	Charge current control block setting input pin. ADJ2 pin “GND to 4.4 V” : Charge current control block output = ADJ2 pin voltage ADJ2 pin “4.6 V to VREF” : Charge current control block output = 1.5 V
10	OUTC2	O	Current detection amplifier (Current Amp2) output pin.
11	CELLS	I	Charge voltage setting switch pin (2 or 3 or 4 Cells). CELLS = VREF: 4 Cells, CELLS = GND: 3 Cells, CELLS = OPEN: 2 Cells
12	BATT	I	Current detection amplifier (Current Amp2) inverted input pin. Battery voltage input pin.
13	+INC2	I	Current detection amplifier (Current Amp2) non-inverted input pin.
14	CTL	I	Power supply control pin. Setting the CTL pin at “H” level places the DC/DC converter IC in the operating mode. Setting the CTL pin at “L” level places the DC/DC converter IC in the standby mode.
15	COMP3	O	Error amplifier (Error Amp3) output pin.
16	ADJ3	I	Charge voltage control block setting input pin. ADJ3 pin “GND to 0.2 V” : Charge voltage setting 4.10 V/Cell ADJ3 pin “0.4 V to 4.4 V” : Charge voltage setting 2 × V_{ADJ3} pin voltage/Cell ADJ3 pin “4.6 V to VREF” : Charge voltage setting 4.20 V/Cell
17	RT	—	Triangular wAVe oscillation frequency setting resistor connection pin.
18	VIN	—	Power supply pin for ACOK function block.
19	VH	O	Power supply pin for FET drive circuit (VH = VCC − 6 V)
20	OUT	O	External FET gate drive pin.
21	VCC	—	Power supply pin for reference voltage , control circuit, and output circuit.
22	CVM	O	Constant voltage control state detection block (CV Comp.) output pin.
23	GND	—	Ground pin.
24	+INC1	I	Current detection amplifier (Current Amp1) non-inverted input pin.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{VCC}	VCC, VIN pin	− 0.3	+ 28	V
		VCC, VIN pin, t ≤ 10 µs	− 0.3	+ 32	V
Output current	I_{OUT}	OUT pin	− 60	+ 60	mA
		Duty ≤ 5% (t = 1/fosc × Duty)	− 700	+ 700	mA
CLT pin input voltage	V_{CTL}	CTL pin	− 0.3	+ 28	V
Input voltage	V_{INE}	ADJ1, ADJ2, ADJ3, CELLS, ACIN pin	− 0.3	V_{VREF} + 0.3	V
	V_{INC}	-INC1, +INC1, BATT, +INC2 pin	− 0.3	+ 28	V
Permissible dissipation	P_D	Ta ≤ + 25 °C	—	1282*1,*2	mW
		Ta = + 85 °C	—	512*1,*2	mW
Storage temperature	T_{STG}	—	− 55	+ 125	°C

*1 : Power dissipation value between + 25 °C and + 85 °C is obtained by connecting these two points with straight line.

*2 : When IC is mounted on a 10 cm square epoxy double-sided.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VCC}	VCC, VIN pin	8	—	25	V
Reference voltage output current	I_{VREF}	—	−1	—	0	mA
VH pin output current	I_{VH}	—	0	—	30	mA
Input voltage	V_{INE}	ADJ1 pin	0	—	V_{VREF} − 1.5	V
		ADJ2 pin (internal reference voltage setting)	4.6	—	V_{VREF}	V
		ADJ2 pin (external voltage setting)	0	—	4.4	V
		ADJ3 pin (internal reference voltage setting)	0	—	0.2	V
			4.6		V_{VREF}	V
		ADJ3 pin (external voltage setting)	0.4	—	4.4	V
		CELLS pin	0	—	V_{VREF}	V
	V_{INC}	+INC1, +INC2, -INC1, BATT pin	0	—	V_{VCC}	V
ACIN pin input voltage	V_{ACIN}	—	0	—	5	V
ACOK pin output voltage	V_{ACOK}	—	0	—	25	V
ACOK pin output current	I_{ACOK}	—	0	—	1	mA
CTL pin input voltage	V_{CTL}	—	0	—	25	V
Output current	I_{OUT}	OUT pin	−45	—	+ 45	mA
		OUT pin Duty ≤ 5% (t = 1 / fosc × Duty)	−600	—	+ 600	mA
Switching frequency	f_{OSC}	—	100	500	2000	kHz
Timing resistor	R_{RT}	RT pin	8.2	33	180	kΩ
VH pin capacitor	C_{VH}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{VREF}	VREF pin	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	−30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = +25 °C, VCC pin = 19 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [REF]	Threshold voltage	V_{VREF1}	6	—	4.963	5.000	5.037	V
		V_{VREF2}	6	Ta = −10 °C to +85 °C	4.950	5.000	5.050	V
	Input stability	VREF Line	6	VCC pin = 8 V to 25 V	—	3	10	mV
	Load stability	VREF Load	6	VREF pin = 0 mA to −1 mA	—	1	10	mV
	Short-circuit output current	Ios	6	VREF pin = 1 V	−25	−12	−6	mA
Triangular Wave Oscillator Block [OSC]	Switching frequency	f_{OSC}	20	RT pin = 33 kΩ	450	500	550	kHz
	Frequency temperature variation	df/fdT	20	Ta = −30 °C to +85 °C	—	1*	—	%
Error Amplifier Block [Error Amp1]	Input offset voltage	V_{IO}	2, 3	COMP1 pin = 2 V	—	1	5	mV
	Input bias voltage	I_{ADJ1}	3	ADJ1 pin = 0 V	−100	—	—	nA
	Transcon-ductance	Gm	15	—	—	20*	—	µA/V
Error Amplifier Block [Error Amp2]	Threshold voltage	V_{TH1}	10	ADJ2 pin = VREF pin	—	1.5*	—	V
	Transcon-ductance	Gm	15	—	—	20*	—	µA/V
Error Amplifier Block [Error Amp3]	Threshold voltage accuracy	V_{TH1}	12	COMP3 pin = 2 V, Ta = +25 °C ADJ3 pin = VREF pin (4.20 V/Cell setting)	−0.5	0	+ 0.5	%
		V_{TH2}	12	COMP3 pin = 2 V, Ta = −10 °C to +85 °C, ADJ3 pin = VREF pin (4.20 V/Cell setting)	−0.7	0	+ 0.7	%
		V_{TH3}	12	COMP3 pin = 2 V, Ta = +25 °C ADJ3 pin = GND, (4.10 V/Cell setting)	−0.6	0	+ 0.6	%
		V_{TH4}	12	COMP3 pin = 2 V, Ta = − 10 °C to +85 °C ADJ3 pin = GND, (4.10 V/Cell setting)	−0.8	0	+ 0.8	%

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(Ta = +25 °C, VCC pin = 19 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Error Amplifier Block [Error Amp3]	Input current	I_{BATTH1}	12	ADJ3 pin = CELLS pin = VREF pin BATT pin = 16.8 V	—	25.2	38	µA
		I_{BATTL}	12	VCC pin = 0 V, BATT pin = 16.8 V	—	0	1	µA
	Transconductance	Gm	15	—	—	30*	—	µA/V
Current Detection Amplifier Block [Current Amp1, Current Amp2]	Input current	I_{+INCH}	13, 24	+INC1 pin = +INC2 pin = 3 V to VCC pin, ΔVin = −100 mV	—	20	30	µA
		I_{-INCH}	1	+INC1 pin = 3 V to VCC pin, ΔVin = −100 mV	—	0.1	0.2	µA
		I_{+INCL}	13, 24	+INC1 pin = +INC2 pin = 0.1 V, ΔVin = −100 mV	−225	−150	—	µA
		I_{-INCL}	1	+INC1 pin = +INC2 pin = 0.1 V, ΔVin = −100 mV	−255	−170	—	µA
	Input offset voltage	V_{OFF1}	2	+INC1 pin = 3 V to VCC pin	−1	0	1	mV
		V_{OFF2}	10	+INC2 pin = 3 V to VCC pin	2	3	4	mV
		V_{OFF3}	10	+INC2 pin = 0 V to 3 V	1	3	5	mV
	Common mode input voltage range	V_{CM}	2, 10	—	0	—	Vvcc	V
	Voltage gain	A_V	2, 10	+INC1 pin = +INC2 pin = 3 V to VCC pin, ΔVin = −100 mV	24.5	25.0	25.5	V/V
	Frequency band width	BW	2, 10	A_V = 0 dB	—	2*	—	MHz
	Output voltage	V_{OUTCH1}	2	—	4.7	4.9	—	V
		V_{OUTCH2}	10	—	4.5	4.7	—	V
		V_{OUTCL}	2, 10	—	50	75	100	mV
	Output source current	I_{SOURCE}	2, 10	OUTC1 pin = OUTC2 pin = 2 V	—	−2	−1	mA
	Output sink current	I_{SINK}	2, 10	OUTC1 pin = OUTC2 pin = 2 V	150	300	—	µA
PWM Comp. Block [PWM Comp.]	Threshold voltage	V_{TL}	20	Duty cycle = 0%	1.4	1.5	—	V
		V_{TH}	20	Duty cycle = 100%	—	2.5	2.6	V

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(Ta = +25 °C, VCC pin = 19 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min.	Typ.	Max.	
Output Block [OUT]	Output source current	I_{SOURCE}	20	OUT pin = 13 V, Duty ≤ 5% (t = 1/fosc × Duty)	—	–400*	—	mA
	Output sink current	I_{SINK}	20	OUT pin = 19V, Duty ≤ 5% (t = 1/fosc × Duty)	—	400*	—	mA
	Output ON resistance	R_{OH}	20	OUT pin = –45 mA	—	6.5	9.8	Ω
		R_{OL}	20	OUT pin = 45 mA	—	5.0	7.5	Ω
	Rise time	tr1	20	OUT pin = 3300 pF	—	50*	—	ns
	Fall time	tf1	20	OUT pin = 3300 pF	—	50*	—	ns
Control Block [CTL]	CTL input voltage	V_{ON}	14	IC operation mode	2	—	25	V
		V_{OFF}	14	IC standby mode	0	—	0.8	V
	Input current	I_{CTLH}	14	CTL pin = 5 V	—	100	150	µA
		I_{CTLL}	14	CTL pin = 0 V	—	0	1	µA
Bias Voltage Block [VH]	Output voltage	V_H	19	VCC pin = 8 V to 25 V, VH pin = 0 to 30 mA	V_{VCC}– 6.5	V_{VCC}– 6.0	V_{VCC}– 5.5	V
Under Voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	21	VCC pin = ↗	6.0	6.2	6.4	V
		V_{THL}	21	VCC pin = ↘	5.0	5.2	5.4	V
	Hysteresis width	V_H	21	VCC pin	—	1.0*	—	V
	Threshold voltage	V_{TLH}	6	VREF pin = ↗	2.6	2.8	3.0	V
		V_{THL}	6	VREF pin = ↘	2.4	2.6	2.8	V
	Hysteresis width	V_H	6	VREF pin	—	0.2	—	V
Over Temperature Detection	Detection temperature	T_{TH}	20	—	—	+ 150	—	°C
	Release temperature	T_{TL}	20	—	—	+ 125	—	°C
AC Adapter Voltage Detection Block [AC Comp.]	Threshold voltage	V_{TLH}	7	—	1.245	1.270	1.295	V
		V_{THL}	7	—	1.215	1.250	1.285	V
	Hysteresis width	V_H	7	—	—	20	—	mV
	ACOK pin output leak current	I_{LEAK}	5	ACOK pin = 25 V	—	0	1	µA
	ACOK pin output “L” level voltage	V_{ACOKL}	5	ACOK pin = 1 mA	—	0.9	1.1	V
	Current consumption	I_{VINL}	18	VIN pin = 19 V, ACIN pin = 0 V	—	0	1	µA
		I_{VINH}	18	VIN pin = 19 V, ACIN pin = 5 V	—	6	10	µA

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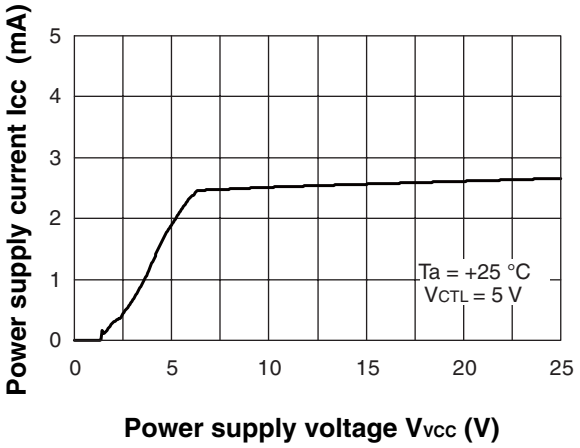
(Ta = +25 °C, VCC pin = 19 V, VREF pin = 0 mA)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min.	Typ.	Max.	
Charge Voltage Control Block [VO REFIN Control]	Input voltage	V_H	16	At 4.20 V/Cell	4.6	—	V_{VREF}	V
		V_{EXT}	16	At external setting	0.4	—	4.4	V
		V_L	16	At 4.10 V/Cell	0	—	0.2	V
	Threshold voltage	V_{TL}	16	—	0.21	0.3	0.39	V
		V_{TH}	16	—	4.41	4.5	4.59	V
	Input current	I_{IN}	16	ADJ3 pin	—	0	1	µA
	Input voltage	V_H	11	At 4 Cells	V_{VREF} – 0.4	—	V_{VREF}	V
		V_M	11	At 2 Cells	2.4	—	2.6	V
		V_L	11	At 3 Cells	0	—	0.3	V
	Input current	I_{INL}	11	CELLS = 0 V	–8.3	–5	—	µA
		I_{INH}	11	CELLS = I_{VREF}	—	5	8.3	µA
Charge Current Control Block [Charge Current Control]	Input voltage	V_H	9	At normal charge	4.6	—	V_{VREF}	V
		V_{EXT}	9	At external setting	0	—	4.4	V
	Threshold voltage	V_{TH}	9	—	4.41	4.50	4.59	V
	Input current	I_{IN}	9	ADJ2 pin	—	0	1	µA
General	Standby current	I_{CCS1}	18	VCC pin = 0 V, CTL pin = 0 V, ACIN pin = 5 V, VIN pin = 19 V	—	6	10	µA
		I_{CCS2}	21	VIN pin = 0 V, CTL pin = 0 V VCC pin = 19 V	—	0	1	µA
	Power supply current	I_{CC}	21	CTL pin = 5 V	—	2.7	4.0	mA

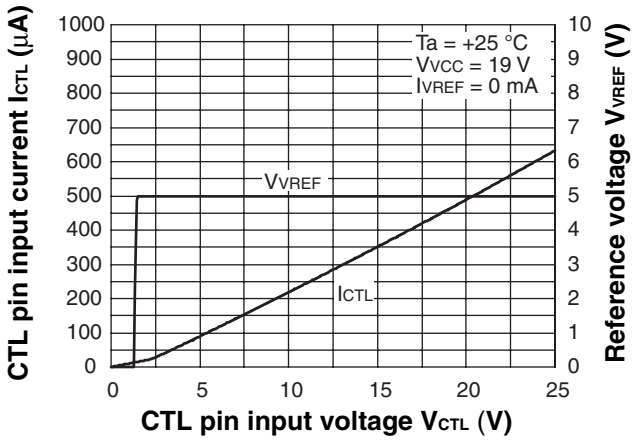
* : Normal design value

■ TYPICAL CHARACTERISTICS

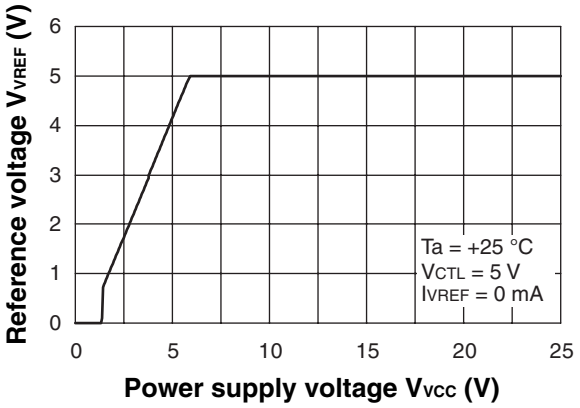
Power supply current vs. Power supply voltage



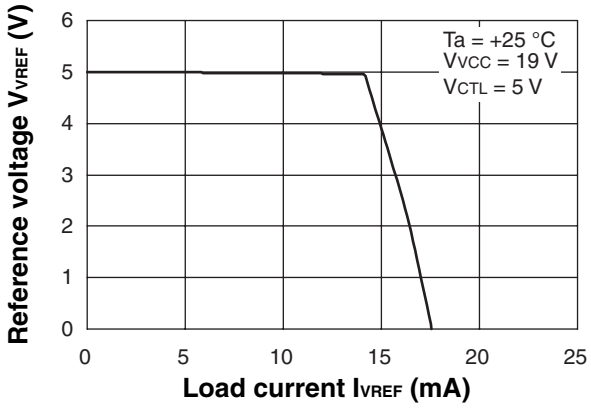
CTL pin input current, Reference voltage vs. CTL pin input voltage



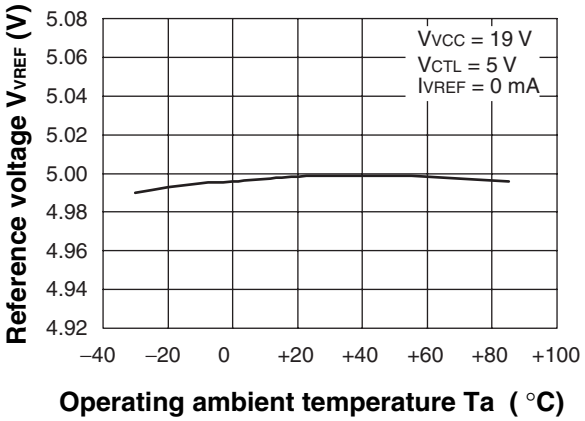
Reference voltage vs. Power supply voltage



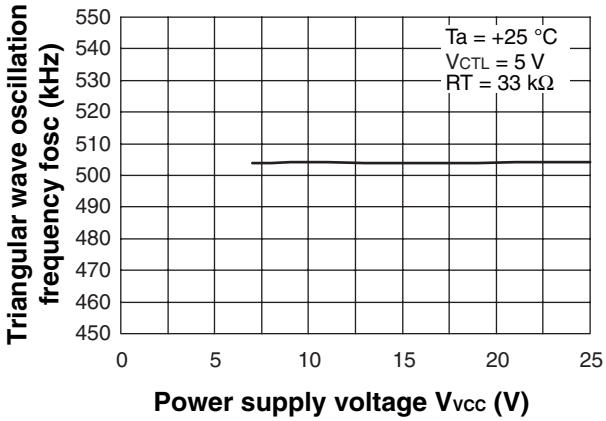
Reference voltage vs. Load current



Reference voltage vs. Operating ambient temperature



Triangular wave oscillation frequency vs. Power supply voltage



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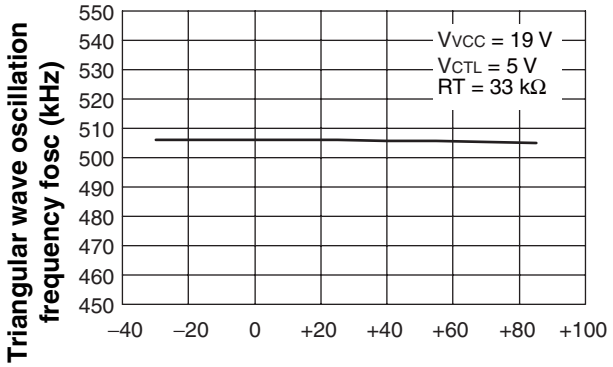
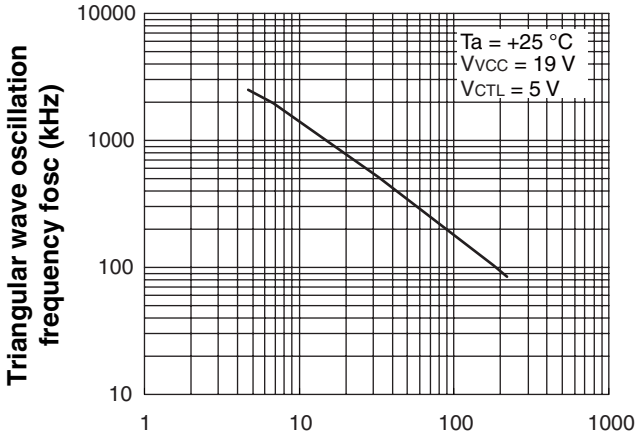
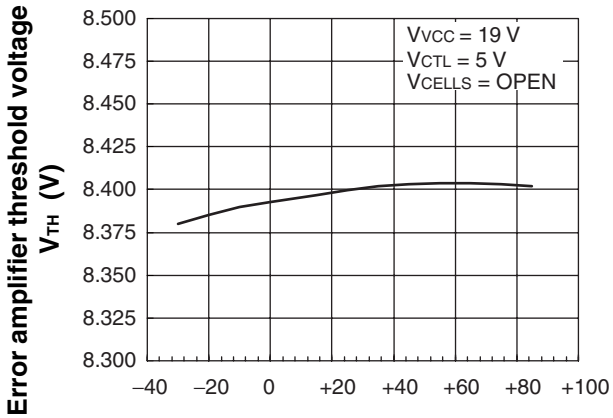
Triangular wave oscillation frequency vs. Operating ambient temperature



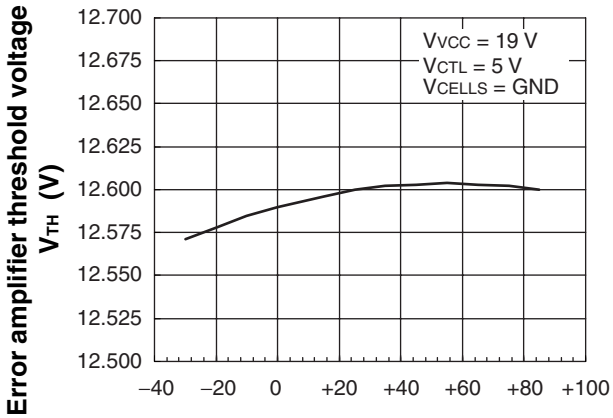
Triangular wave oscillation frequency vs. Timing resistor



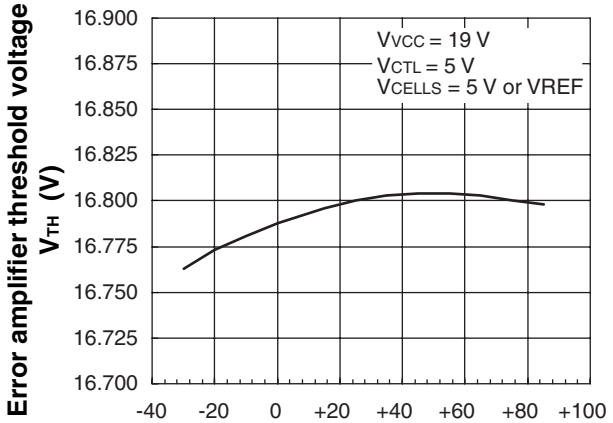
Error amplifier threshold voltage vs. Operating ambient temperature



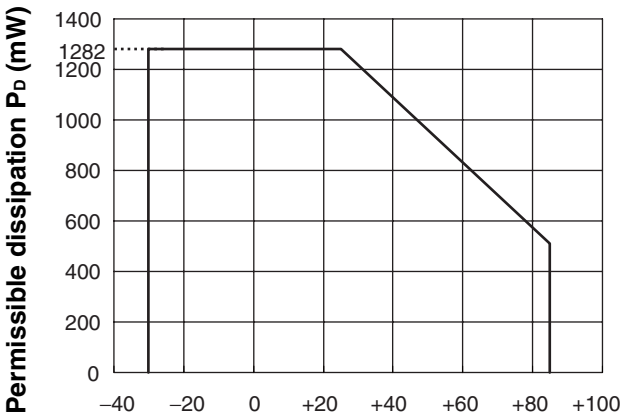
Error amplifier threshold voltage vs. Operating ambient temperature



Error amplifier threshold voltage vs. Operating ambient temperature



Permissible dissipation vs. Operating ambient temperature



■ FUNCTIONAL DESCRIPTION

MB39A134 is a DC/DC converter which uses pulse width modulation (PWM) for charging Li-ion battery and controls the charge voltage and current when charging the battery. It includes the charge control function for the battery and the AC adapter voltage detection function to stably supply the voltage from the AC adapter and the battery to the system.

- When controlling the charge voltage (constant voltage mode), the voltage entered in ADJ3 pin and CELLS pin can be used to set an arbitrary voltage. The error amplifier (Error Amp3) compares BATT pin voltage with the internal reference voltage to generate the PWM control signal for generating an arbitrary charge voltage.
- When controlling the charge current (constant current mode) , the current detection amplifier (Current Amp2) amplifies the voltage drop generated between both ends of the charge current sense resistance (R_S) to 25 times and outputs it through OUTC2 pin. The error amplifier (Error Amp2) compares the output voltage from the current detection amplifier (Current Amp2) with the voltage set at ADJ2 pin to generate the PWM control signal for executing the constant current charge.
- When controlling the AC adapter power, the current detection amplifier (Current Amp1) amplifies the difference between -INC1 pin voltage and +INC1 pin voltage (V_{VREF}) to 25 times and outputs it through OUTC1 pin when the output voltage of the AC adapter drops. The error amplifier (Error Amp1) compares the output voltage from the current detection amplifier (Current Amp1) with ADJ1 pin voltage to generate the PWM control signal for controlling the charge current so that AC adapter power can be kept constant.

The triangular wave voltage generated from the triangular wave oscillator is compared with the lowest potential of the output voltages from the error amplifier (Error Amp1, Error Amp2, and Error Amp3) and when the former is lower than the latter, the high side switching FET is set on.

In addition, AC Comp detects installation/removal of the AC adapter and its information is generated through ACOK pin.

1. DC/DC Converter Block

(1) Reference voltage block (REF)

The reference voltage circuit (REF) uses the voltage supplied from the VCC pin (pin 21) to generate a temperature compensated, stable voltage (5.0 V Typ) used as the reference supply voltage for the IC's internal circuitry.

This pin can also be used to obtain a load current to a maximum of 1 mA from the reference voltage VREF pin (pin 6) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator contains the built-in capacitor for frequency setting, and generates the triangular wave oscillation waveform by connecting the frequency setting resistor with the RT pin (pin 17) .

The triangular wave is input to the PWM comparator inside the IC.

Triangular wave oscillation frequency fosc

fosc (kHz) ≒ 17000 / RT (kΩ)

(3) Error amplifier block (Error Amp1)

This amplifier detects the output signal from the current detection amplifier (Current Amp 1) and outputs a PWM control signal.

In addition, it provides stable phase compensation to the system by connecting the resistor and the capacitor to COMP1 pin.

(4) Error amplifier block (Error Amp2)

This amplifier detects the output signal from the current detection amplifier (Current Amp2) , compares this to the output signal from the charge current control circuit, and outputs a PWM control signal to be used in controlling the charge current.

In addition, it provides stable phase compensation to the system by connecting the resistor and the capacitor to COMP2 pin.

(5) Error amplifier block (Error Amp3)

This error amplifier (Error Amp3) detects the DC/DC converter output voltage (battery charge voltage) , compares this to the output signal from the VO REFIN Control circuit, and outputs the PWM control signal. Arbitrary output voltage from 2 Cell to 4 Cell can be set by connecting an external resistor for setting charge voltage to ADJ3 pin (pin 16) . In addition, it provides stable phase compensation to the system by connecting the resistor and the capacitor to COMP3 pin.

(6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) amplifies the voltage difference between +INC1 pin (pin 24) and -INC1 pin (pin 1) 25 times and the signal is output to the following error amplifier (Error Amp1) .

(7) Current detection amplifier block (Current Amp2)

The current detection amplifier (Current Amp2) detects a voltage drop on the both ends of the output sense resistor (R_S) due to the flow of the charge current, using the +INC2 pin (pin 13) and BATT pin (pin 12) . The signal amplified to 25 times is output to the following error amplifier (Error Amp2) .

(8) PWM comparator block (PWM Comp.)

The PWM comparator circuit (PWM Comp.) is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1 to Error Amp3) depending on their output voltage.

The PWM comparator circuit compares the triangular wave voltage generated by the triangular wave oscillator with the error amplifier output voltage and turns on the external output transistor (MOS FET) , during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

(9) Output block (OUT)

The output circuit uses a totem-pole configuration capable of driving an external P-ch MOS FET.

The output “L” level sets the output amplitude to 6 V (Typ) using the voltage generated by the bias voltage block (VH) .

This results in increasing conversion efficiency and suppressing the withstand voltage of the connected external transistor (MOSFET) even in a wide range of input voltages.

(10) Power supply control block (CTL)

Setting the CTL pin (pin 14) to “L” level places the IC in the standby mode. During the standby mode, only AC adapter detection function is operated. (The supply current is 6 μA at typical in the standby mode.)

CTL function table

CTL	Power	AC adapter detection
L	OFF (Standby)	ON (Active)
H	ON (Active)	ON (Active)

(11) Bias voltage block (VH)

The bias voltage circuit outputs V_{CC} – 6 V (Typ) as the minimum potential of the output circuit. In the standby mode, this circuit outputs the potential equal to V_{CC}.

2. Protection Functions

(1) Under voltage lockout protection circuit block (UVLO)

The transient state or a momentary decrease in supply voltage or internal reference voltage (VREF pin) , which occurs when the power supply (VCC pin) is turned on, may cause malfunctions in the control IC, resulting in breakdown or deterioration of the system.

To prevent such malfunction, the under voltage lockout protection circuit detects internal reference voltage drop and fixes the OUT pin (pin 20) to the “H” level. The system restores when the power supply and the internal reference reaches less than the threshold voltage of the lockout protection circuit at the low voltage level.

Protection circuit (UVLO) operation function table

When UVLO is operating (VCC or VREF voltage is lower than UVLO threshold voltage.)

pin	OUT
Status	H

(2) Over temperature detection

The circuit protects an IC from heat-destruction. If the temperature at the joint part reaches +150 °C, the circuit changes the level of OUT pin to “H”, and stops the voltage output.

In addition, if the temperature at the joint part drops to +125 °C, the output restarts again.

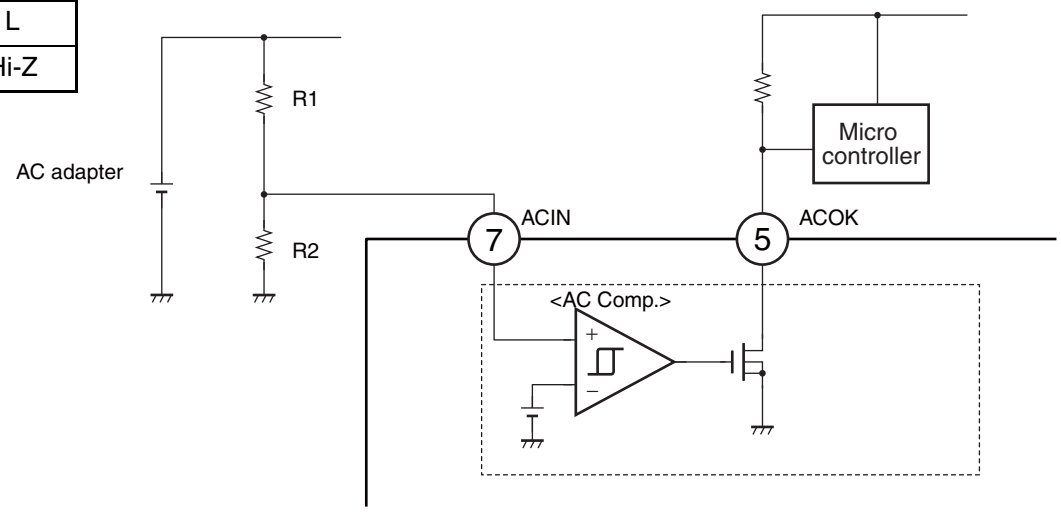
Therefore, make sure to design the DC/DC power supply system so that the over heating protection does not start frequently.

3. Detection Functions

AC adapter voltage detection block (AC Comp.)

The AC adapter voltage detection block (AC Comp.) detects that ACIN pin voltage is below 1.25 V (Typ) and sets ACOK pin in the AC adapter voltage detection block to Hi-Z. In addition, a higher voltage from either VCC pin or VIN pin is supplied as the IC power supply.

ACIN	ACOK
H	L
L	Hi-Z



AC adapter detection voltage setting

V_{IN} = Low to High

Vth = (R1 + R2) / R2 × 1.27 V

V_{IN} = High to Low

Vth = (R1 + R2) / R2 × 1.25 V

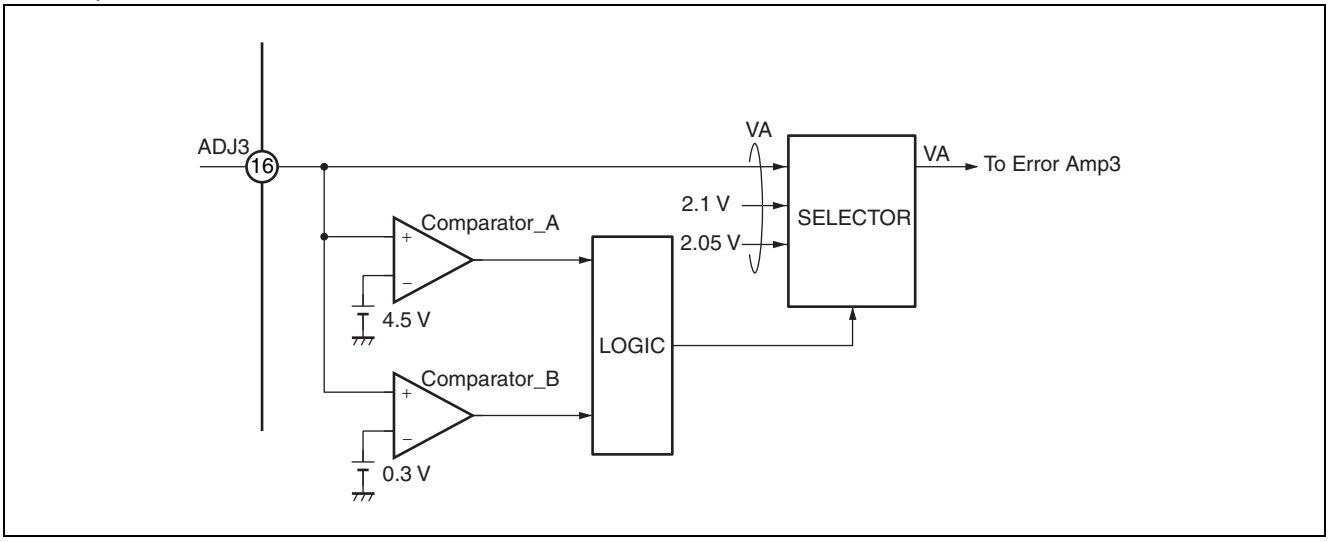
4. Setting the Charge Voltage

The charge voltage (DC/DC output) is set by the input voltage to ADJ3 pin (pin 16) and CELLS pin (pin 11) . The ADJ3 pin (pin 16) can set charge voltage per cell. An arbitrary charge voltage is set when external resistor is set. It doesn't need external resistor when ADJ3 pin (pin 16) is input to VREF level or GND level by internal high accurate reference voltage. The CELLS pin (pin 11) can set the series battery number when the pin is input VREF, OPEN or GND level.

The setting of ADJ3 pin (pin 16), CELLS pin (pin 11) and charge voltage (DC/DC output) is shown below.

ADJ3 Input Voltage	CELLS	Charge Voltage	Note
VREF pin (ADJ3 ≥ 4.6 V)	OPEN	8.4 V	2 Cell × 4.20 V/Cell
	GND	12.6 V	3 Cell × 4.20 V/Cell
	VREF	16.8 V	4 Cell × 4.20 V/Cell
GND pin (ADJ3 ≤ 0.2 V)	OPEN	8.2 V	2 Cell × 4.10 V/Cell
	GND	12.3 V	3 Cell × 4.10 V/Cell
	VREF	16.4 V	4 Cell × 4.10 V/Cell
External voltage setting (ADJ3 = 0.4 V to 4.4 V)	OPEN	4 × ADJ3 pin voltage	2 Cell × 2 × ADJ3 pin voltage/Cell
	GND	6 × ADJ3 pin voltage	3 Cell × 2 × ADJ3 pin voltage/Cell
	VREF	8 × ADJ3 pin voltage	4 Cell × 2 × ADJ3 pin voltage/Cell

• ADJ3 pin internal circuit



5. Setting the Charge Current

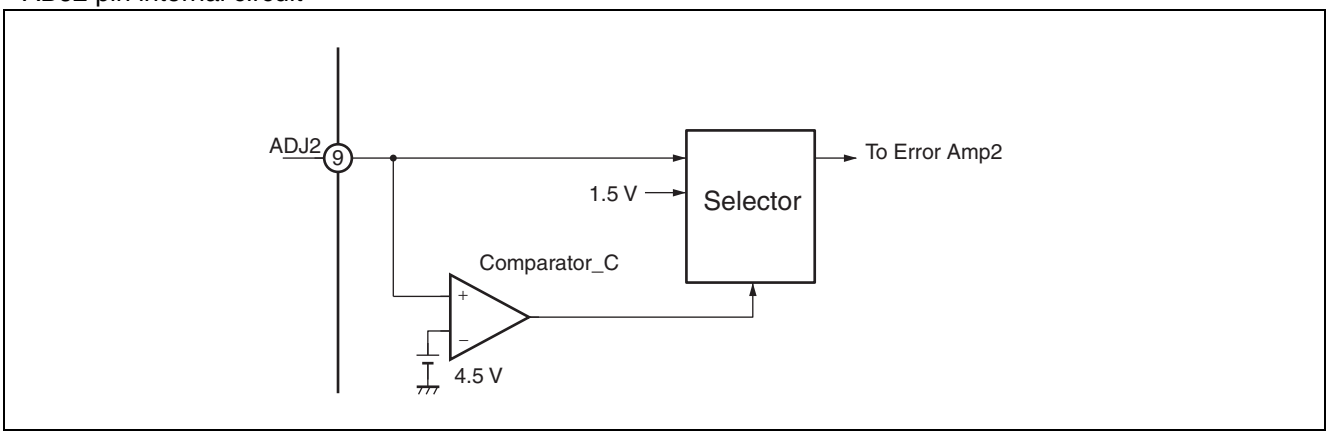
The Error amplifier block (Error Amp2) compares the output voltage of charge current control block set by ADJ2 pin (pin 9) with the output signal from the current detection amplifier (current Amp2) , and outputs a PWM control signal to be used in controlling the maximum charge current for battery. When the current overflows the rated value, the current will be constantly charged to the rated value, and the charge voltage will drop.

Battery charge current setting voltage : ADJ2

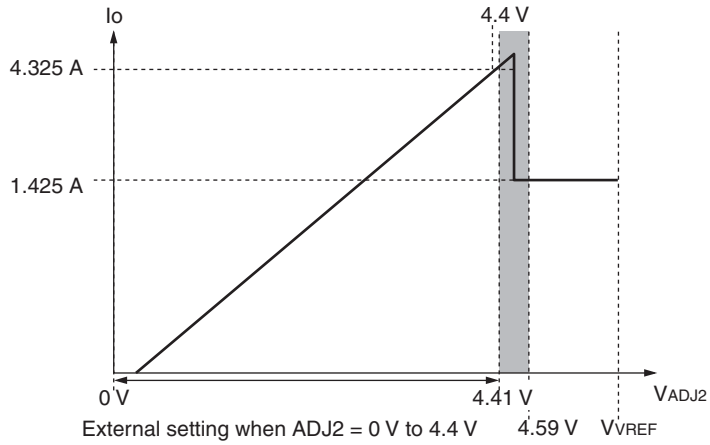
$$\text{Upper limit of charge current Io} = \frac{\text{Charge current control block output voltage voltage (V)} - 0.075}{\text{Current detection amplifier block voltage gain (25.0 V/V Typ)} \times \text{sense resistor } R_S\ (\Omega)}$$

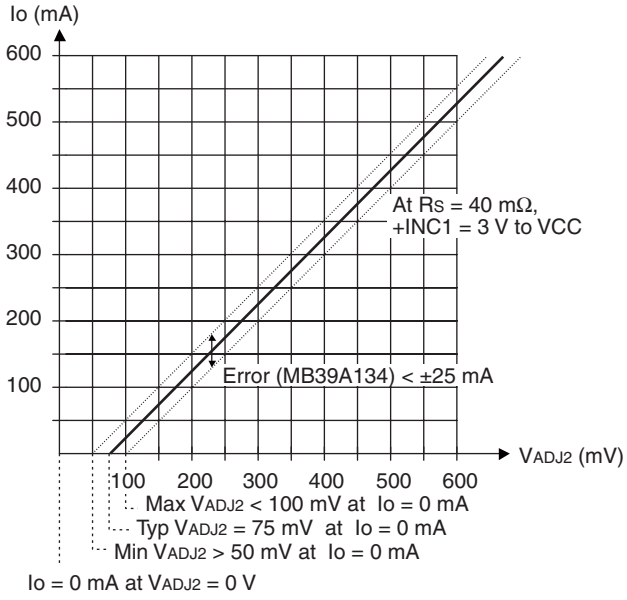
ADJ2 Input Voltage	Charge Current Control Block Output Voltage	Charge Current		
		R_S = 40 mΩ	**R_S = 20 mΩ**	**R_S = 15 mΩ**
VREF (ADJ2 > 4.6 V)	1.5 V	1.425 A	2.85 A	3.79 A
External Voltage Setting (ADJ2 = GND to 4.4 V)	V_{ADJ2} (V)	V_{ADJ2}-0.075 (A)	2 × (V_{ADJ2}-0.075) (A)	2.66 × (V_{ADJ2}-0.075) (A)

• ADJ2 pin internal circuit



• Example of charge current setting (R_S = 40 mΩ)





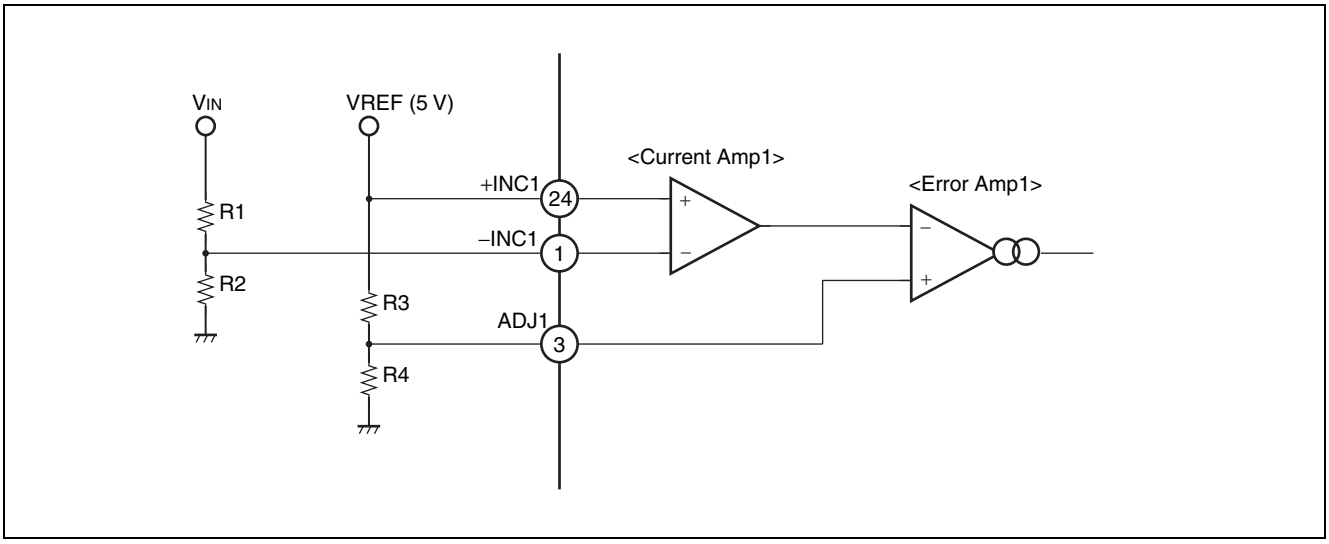
6. Setting Dynamically-Controlled-Charging

By connecting as shown in the example of the figure below, the AC adopter voltage (V_{IN}) drops and becomes the calculated Vth, and then, the dynamically-controlled charging loop reduce the charge current to keep a settled power level.

AC adopter voltage in dynamically controlled charging mode:

$$Vth = VREF \times \left(1 - \frac{1}{A_V} \times \frac{R4}{R3 + R4}\right) \times \frac{R1 + R2}{R2}$$

VREF : Reference voltage (5.0 V Typ) A_V : Current detection amplifier block voltage gain (25.0 V/V Typ)



■ TRANSIT RESPONSE WHEN A LOAD CHANGES SUDDENLY

The constant voltage control loop and the constant current control loop are independent each other and when a load changes suddenly, these two control loops switch over each other.

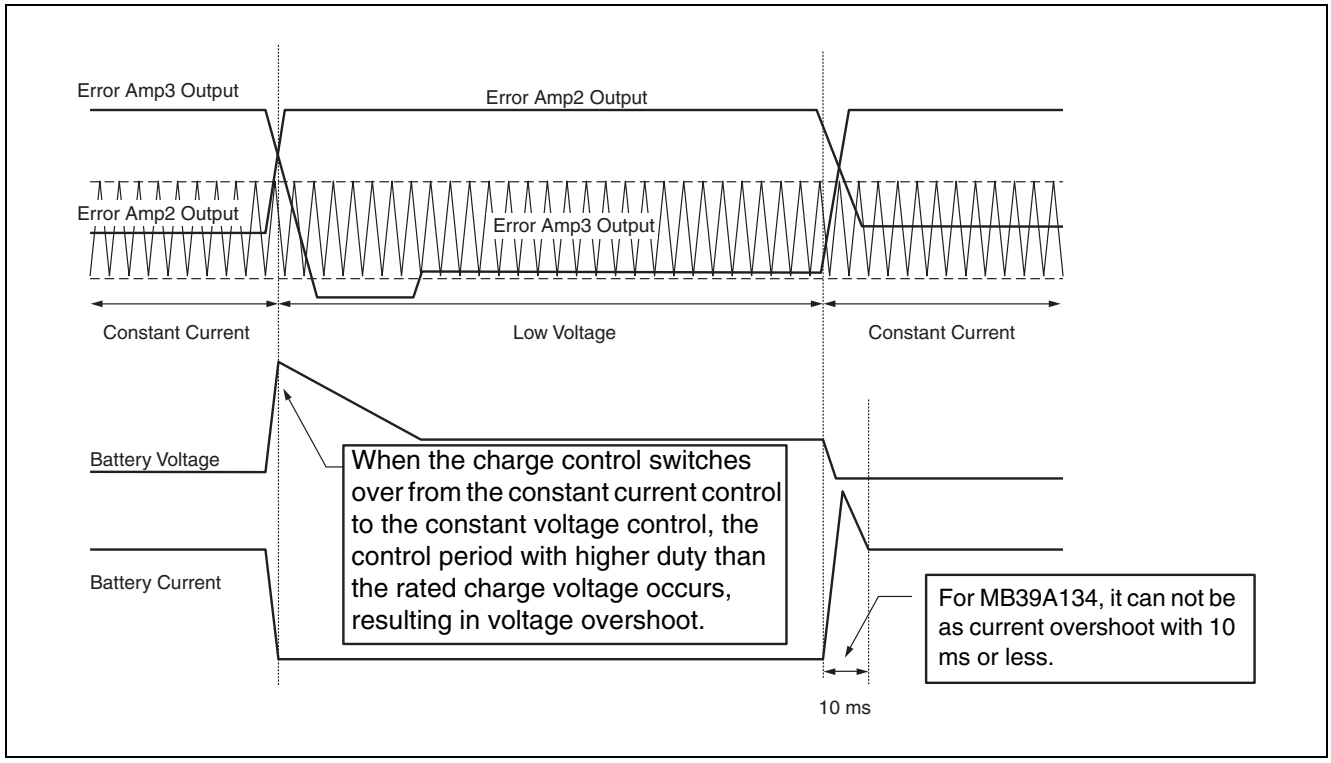
Overshoot of the battery voltage and current is generated by the delay in the control loop when changing the mode.

The delay time is determined by the phase compensation components values.

When the constant current control switches over to the constant voltage control when removing the battery, the control period with higher duty than the rated charge voltage occurs, resulting in voltage overshoot. In such a period, since the battery is removed, no excessive voltage should be applied to the battery.

When the constant voltage control switches over to the constant current control when installing the battery, the control period with higher duty than the rated charge current occurs, resulting in current overshoot.

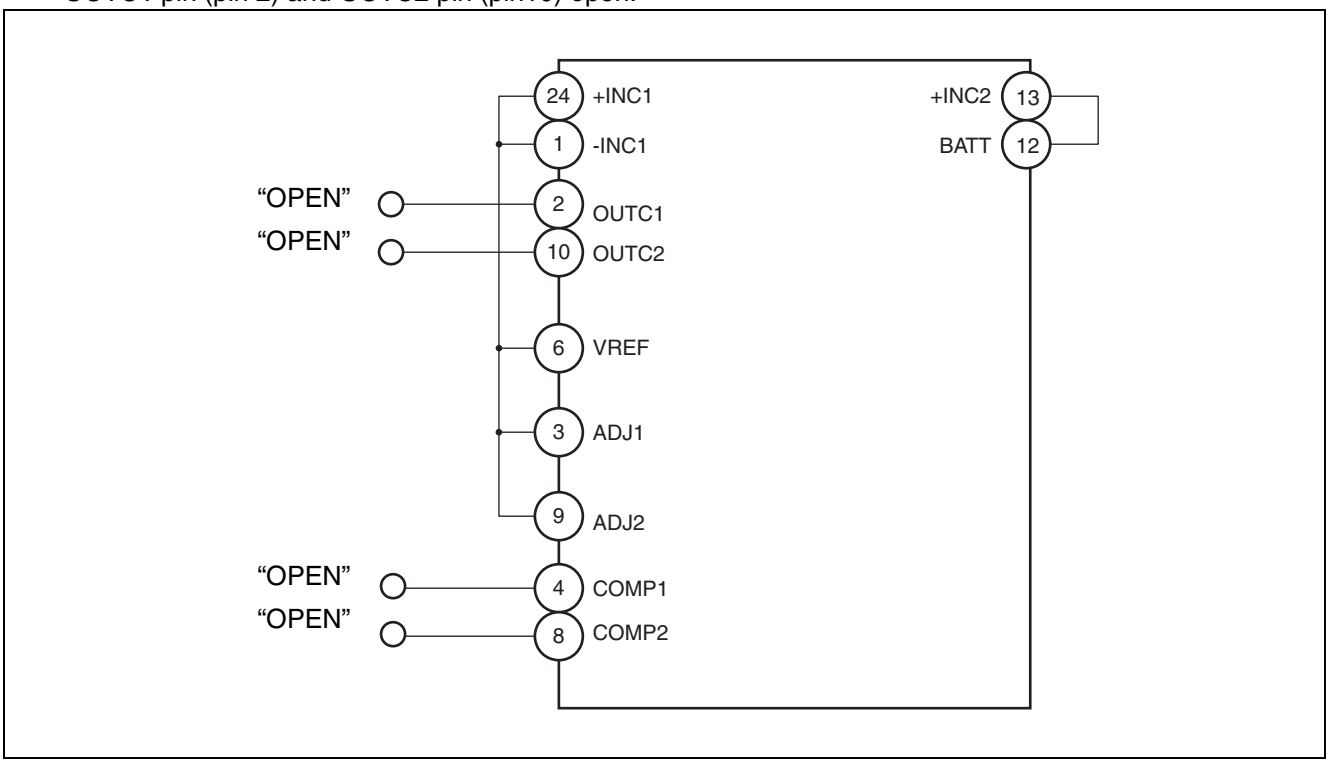
For MB39A134, it can not be as current overshoot with 10 ms or less.



■ CONNECTION WITHOUT USING THE Current Amp1, Current Amp2 AND THE Error Amp1, Error Amp2

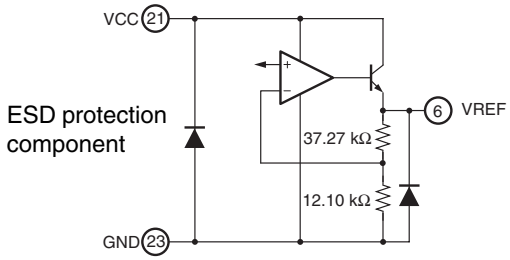
When Current Amp1, 2 or Error Amp1, 2 are not used, please connect it as follows.

- +INC1 pin (pin 24), -INC1 pin (pin 1), ADJ1 pin (pin 3), and ADJ2 pin (pin 9) are connected with the VREF pin.
- +INC2 pin (pin 13) is connected with the pin BATT pin (pin 12).
- OUTC1 pin (pin 2) and OUTC2 pin (pin10) open.

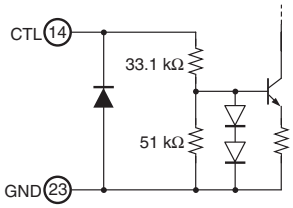


■ INPUT/OUTPUT PIN EQUIVALENT CIRCUIT DIAGRAM

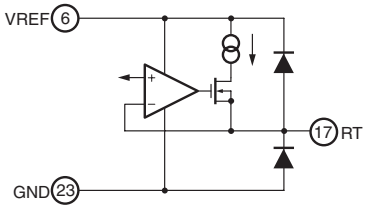
<Reference voltage block>



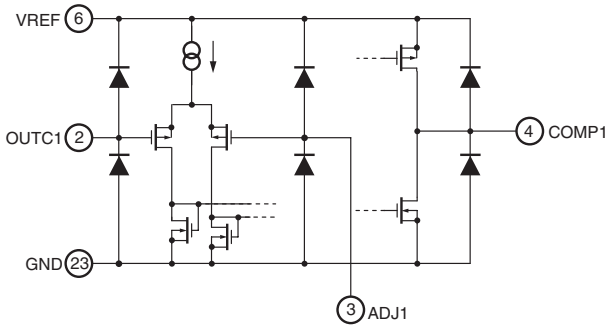
<Control bloc>



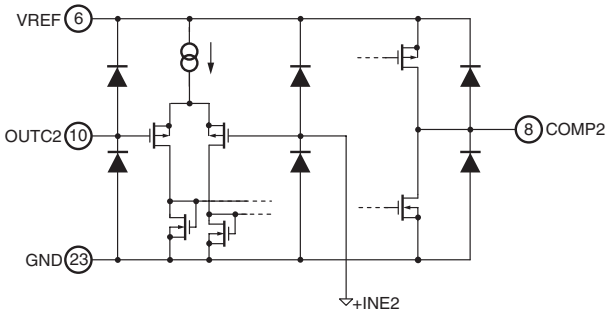
<Triangular wave oscillator block>



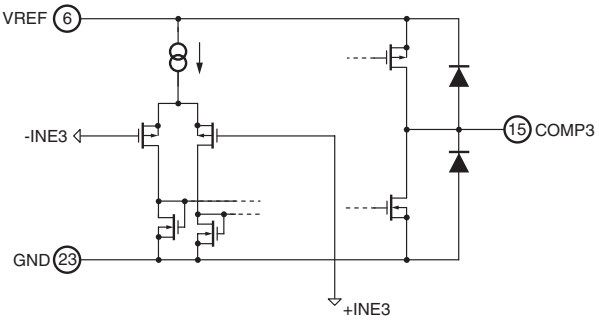
<Error amplifier block (Error Amp1) >



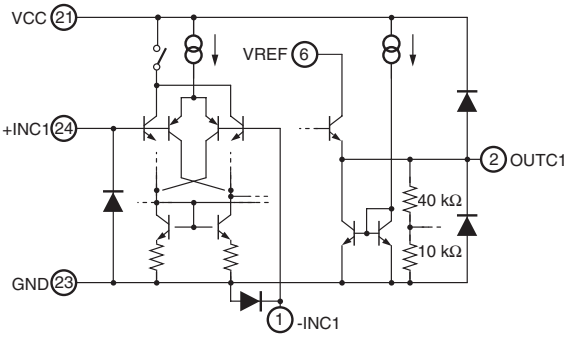
<Error amplifier block (Error Amp2) >



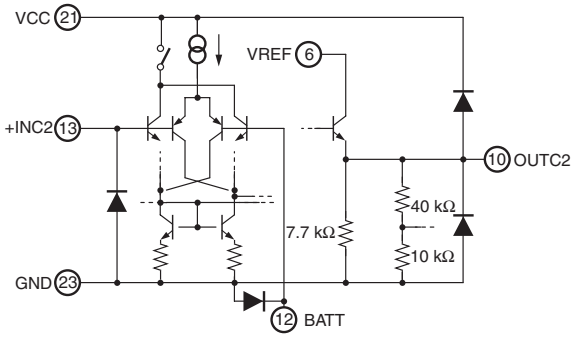
<Error amplifier block (Error Amp3) >



<Current detection amplifier block (Current Amp1) >



<Current detection amplifier block (Current Amp2) >



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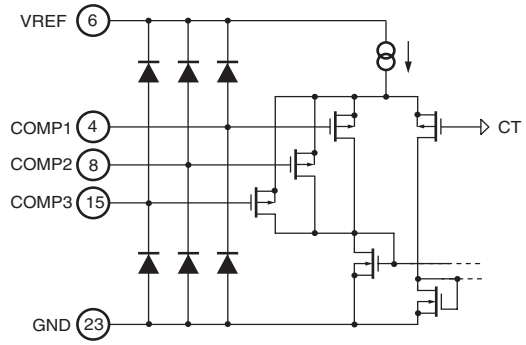
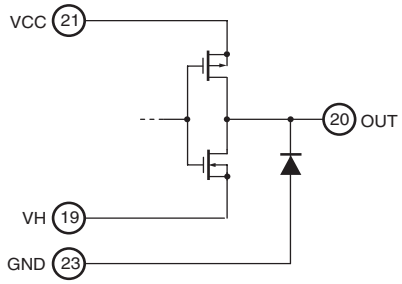
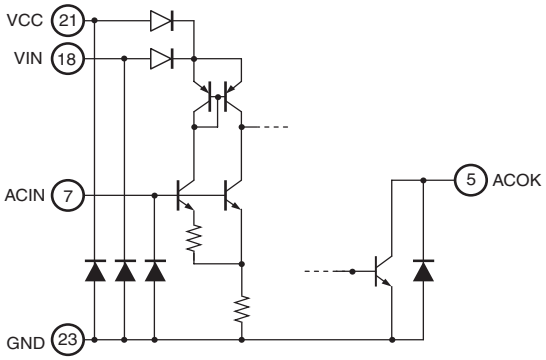
<PWM comparator block>



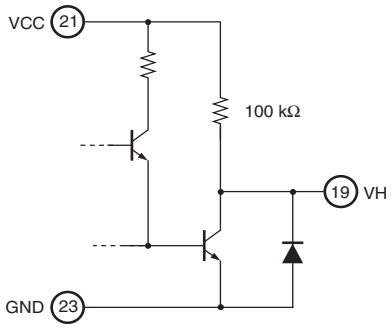
<Output block>



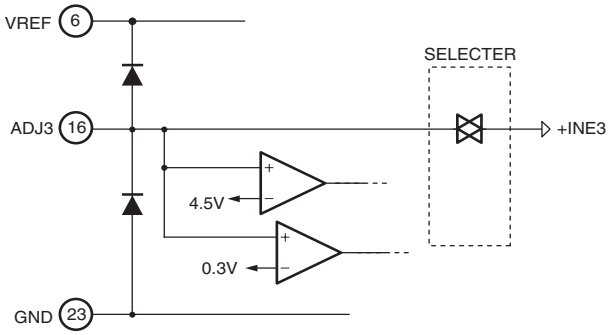
<AC adapter detection block>



<Bias voltage block>



<Charge voltage setting block>



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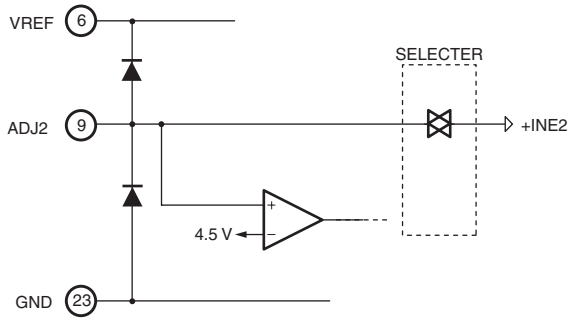
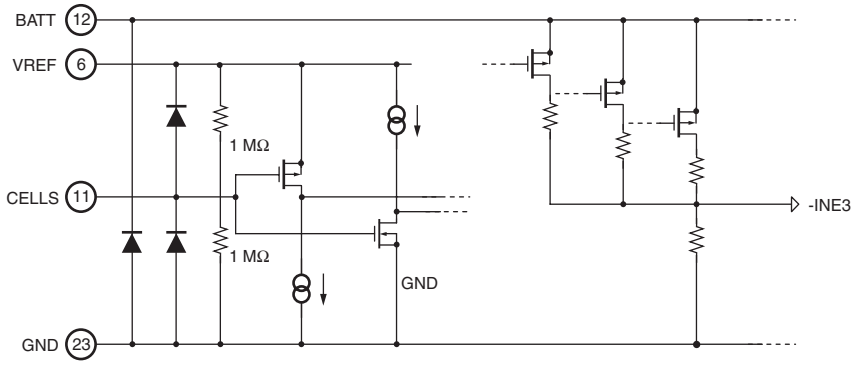
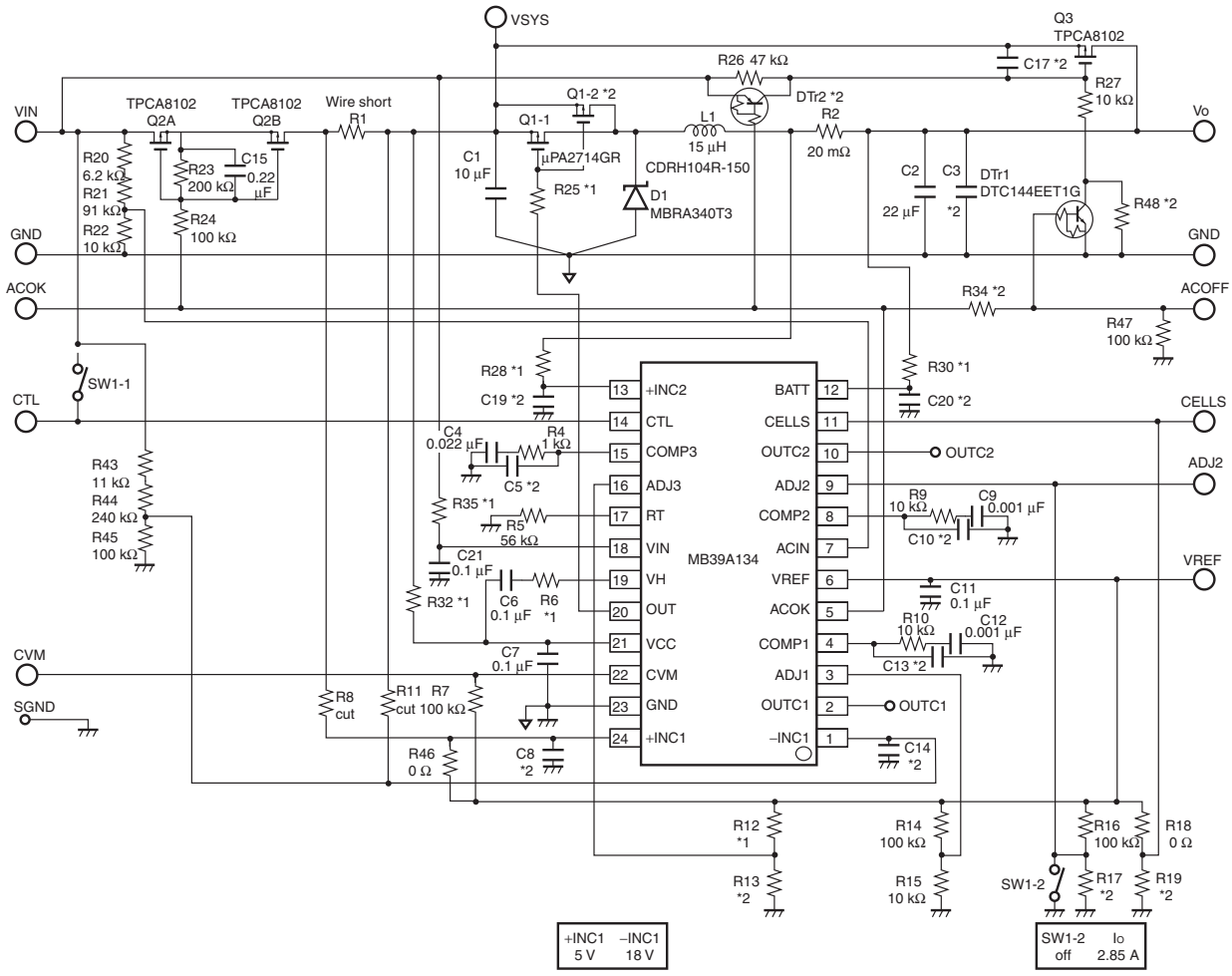
<Charge current setting block>



<Cell switch block>



■ TYPICAL APPLICATION CIRCUIT



*1 Patterm short
*2 Not mounted

Place R12 = 0 Ω for output 4.2 V/Cell.
Place R13 = 0 Ω for output 4.1 V/Cell.

Place R18 = 0 Ω for 4 Cells operation.
Place R19 = 0 Ω for 3 Cells operation.
Open R18 & R19 2 Cells operation.

■ PARTS LIST

Com-ponent	Item	Specification	Vendor	Package	Parts No.	Remarks
M1	IC	MB39A134	FML	TSSOP-24	—	
Q1-1	P-ch FET	VDS = − 20 V, ID = 7 A (Max)	NEC	SOP-8	μPA2714GR	
Q1-2	P-ch FET	—	—	—	—	Not mounted
Q2A	P-ch FET	VDS = − 30 V, ID = 40 A (Max)	TOSHIBA	SOP Advance	TPCA8102	
Q2B	P-ch FET	VDS = − 30 V, ID = 40 A (Max)	TOSHIBA	SOP Advance	TPCA8102	
Q3	P-ch FET	VDS = − 30 V, ID = 40 A (Max)	TOSHIBA	SOP Advance	TPCA8102	
DTr1	Transistor	VCEO = 50 V	ON Semi	SC-75	DTC144EET1G	
DTr2	Transistor	—	—	—	—	Not mounted
D1	Diode	VF = 0.45 V (Max) at IF = 3 A	ON Semi	RMDS	MBRA340T3	
L1	Inductor	15 μH 50 mW Irms = 3.1 A	SUMIDA	SMD	CDRH104R-150	
C1	Ceramic Capacitor	10 μF (25 V)	TDK	3225	C3225X5R1E106K	
C2	Ceramic Capacitor	22 μF (25 V)	TDK	3225	C3225JC1E226M	
C3	—	—	—	—	—	Not mounted
C4	Ceramic Capacitor	0.022 μF (50 V)	TDK	1608	C1608JB1H223K	
C5	—	—	—	—	—	Not mounted
C6	Ceramic Capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C7	Ceramic Capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C8	—	—	—	—	—	Not mounted
C9	Ceramic Capacitor	0.001 μF (50 V)	TDK	1608	C1608JB1H102J	
C10	—	—	—	—	—	Not mounted
C11	Ceramic Capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C12	Ceramic Capacitor	0.001 μF (50 V)	TDK	1608	C1608JB1H102J	
C13	—	—	—	—	—	Not mounted
C14	—	—	—	—	—	Not mounted
C15	Ceramic Capacitor	0.22 μF (25 V)	TDK	1608	C1608JB1H224K	
C17	Ceramic Capacitor	—	—	—	—	Not mounted
C19	—	—	—	—	—	Not mounted
C20	—	—	—	—	—	Not mounted
C21	Ceramic Capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	

(Continued)

Com-ponent	Item	Specification	Vendor	Package	Parts No.	Remarks
R1	Resistor	0	Mac-Eight	SMD	MJP-0.2	Wire short
R2	Resistor	20 mΩ	KOA	SL1	SL1TTE20L0D	
R4	Resistor	1 kΩ	SSM	1608	RR0816P102D	
R5	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R6	—	—	—	—	—	Pattern short
R7	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R8	—	—	—	—	—	Pattern cut
R9	Resistor	10 kΩ	SSM	1608	RR0816P103D	
R10	Resistor	10 kΩ	SSM	1608	RR0816P103D	
R11	—	—	—	—	—	Pattern cut
R12	—	—	—	—	—	Pattern short
R13	—	—	—	—	—	Not mounted
R14	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R15	Resistor	10 kΩ	SSM	1608	RR0816P103D	
R16	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R17	—	—	—	—	—	Not mounted
R18	Resistor	0 Ω	KOA	1608	RK73Z1J	
R19	—	—	—	—	—	Not mounted
R20	Resistor	6.2 kΩ	SSM	1608	RR0816P622D	
R21	Resistor	91 kΩ	SSM	1608	RR0816P913D	
R22	Resistor	10 kΩ	SSM	1608	RR0816P103D	
R23	Resistor	200 kΩ	SSM	1608	RR0816P204D	
R24	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R25	—	—	—	—	—	Pattern short
R26	Resistor	47 kΩ	SSM	1608	RR0816P473D	
R27	Resistor	10 kΩ	SSM	1608	RR0816P103D	
R28	—	—	—	—	—	Pattern short
R30	—	—	—	—	—	Pattern short
R32	—	—	—	—	—	Pattern short
R34	Resistor	—	—	—	—	Not mounted
R35	—	—	—	—	—	Pattern short
R43	Resistor	11 kΩ	SSM	1608	RR0816P113D	
R44	Resistor	240 kΩ	SSM	1608	RR0816P244D	
R45	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R46	Resistor	0 Ω	KOA	1608	RK73Z1J	

(Continued)

(Continued)

Compo-nent	Item	Specification	Vendor	Package	Parts No.	Remarks
R47	Resistor	100 kΩ	SSM	1608	RR0816P104D	
R48	Resistor	—	—	—	—	Not mounted
SW1	DIP SW	SW	MATSUKYU	SMD	DMS-2H	
PIN	Wiring Pin	WT-2-1	Mac-Eight	—	WT-2-1	11-pin

Note : These components are recommended based on the operating tests authorized.

FML : Fujitsu Microelectronics Limited
NEC : NEC Corporation
TOSHIBA : TOSHIBA Corporation
ON Semi : ON Semiconductor Corporation
SUMIDA : SUMIDA Corporation
TDK : TDK Corporation
Mac-Eight : Mac-Eight Co.,Ltd
KOA : KOA Corporation
SSM : SUSUMU Co.,Ltd
MATSUKYU : Matsukyu Co.,Ltd

■ APPLICATION NOTE

• Selecting inductor

The inductance value should be selected, as a reference, so that the peak-to-peal value of the inductor ripple current is 50% or less of the maximum charge current. In such a case, the inductance value can be obtained as follows :

$$L \geq \frac{V_{IN} - V_O}{LOR \times I_{OMAX}} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

L : Inductance value [H]

I_{OMAX} : Max. charge current [A]

LOR : Peak-to-peak value of inductor ripple current - max. charge current ratio (0.5)

V_{IN} : Switching system power supply voltage [V]

V_O : Charge voltage [V]

fosc : Switching frequency [Hz]

The minimum charge current value (critical current value) without backward inductor current can be obtained as follow :

$$I_{OC} = \frac{V_O}{2 \times L} \times \frac{V_{IN} - V_O}{V_{IN} \times f_{OSC}}$$

I_{OC} : Critical current [A]

L : Inductance value [H]

V_{IN} : Switching system power supply voltage [V]

V_O : Charge voltage [V]

fosc : Switching frequency [Hz]

To judge that the current passing through the inductor is below a rated value, it is necessary to obtain a maximum current value passing through the inductor. The maximum inductor current value can be obtained as follows :

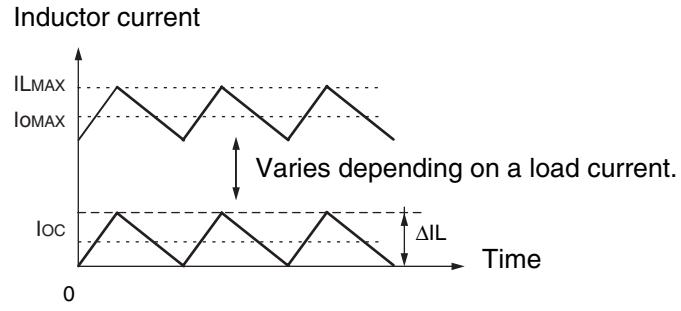
$$I_{LMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

I_{LMAX} : Max. inductor current [A]

I_{OMAX} : Max. charge current [A]

ΔIL : Peak-to-peak value of inductor ripple current [A]

$$\Delta IL \geq \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$



• Selecting SWFET

If MB39A134 is used for the charger for a notebook PC, MOSFET with the 30V range can be normally used for SWFET since the output voltage from the AC adapter (which is the input voltage to it) is 25V or less.

To judge that the current passing through SWFET is below a rated value, it is necessary to obtain a maximum current value passing through SWFET. The maximum SWFET current value can be obtained as follows :

$$I_{DMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

I_{DMAX} : Max. SWFET drain current [A]

I_{OMAX} : Max. charge current [A]

ΔIL : Peak-to-peak value of inductor ripple current [A]

Furthermore, to judge that permissible SWFET loss is below a rated value, it is necessary to obtain the SWFET loss.
To reduce SWFET loss as much as possible, select a SWFET making sure that the continuity loss becomes equal to the switching loss as a reference.

The SWFET continuity loss is obtained by the following formula:

$$P_{Ron} = \frac{V_O}{V_{IN}} \times I_O^2 \times Ron$$

P_{Ron} : SWFET continuity loss [W]

I_O : Charge current [A]

V_{IN} : Switching system power supply voltage [V]

V_O : Charge voltage [V]

Ron : SWFET on resistance [Ω]

Rough SWFET switching loss can be obtained as follows :

$$P_{SW} = \frac{1}{2} \times V_{IN} \times IL_{MIN} \times fosc \times Tr + \frac{1}{2} \times V_{IN} \times IL_{MAX} \times fosc \times Tf$$

P_{SW} : SWFET switching loss [W]

$IL_{MIN} = Iomax - \Delta IL / 2$: Lower value of inductor current [A]

$IL_{MAX} = Iomax + \Delta IL / 2$: Upper value of inductor current [A]

V_{IN} : Switching system power supply voltage [V]

fosc : Switching frequency [Hz]

Tr : SWFET turn-on time [s]

Tf : SWFET turn-off time [s]

- Selecting flyback diode

Select the shot-key barrier diode (SBD) with a small forward voltage as much as possible.

To judge that the current passing through the flyback diode is below a rated value, it is necessary to obtain a peak current value passing through the flyback diode. The maximum current value of the flyback diode can be obtained as follows :

$$If \geq Io_{MAX} + \frac{\Delta IL}{2}$$

I_f : Forward current [A]

Io_{MAX} : Max. charge current [A]

ΔIL : Peak-to-peak value of inductor ripple current [A]

Furthermore, to judge that permissible SBD loss is below a rated value, it is necessary to obtain the SBD loss. The SBD loss can be obtained as follows :

$$P_{SBD} = Io_{MAX} \times (1 - \frac{V_O}{V_{IN}}) \times Vf$$

P_{SBD} : SBD loss [W]

Io_{MAX} : Max. charge current [A]

V_{IN} : Switching system power supply voltage [V]

V_O : Charge voltage [V]

Vf : Forward voltage [V]

• Selecting output capacitor

It is necessary to use the capacitor with sufficient withstand against the surge current which generates when installing/removing a battery. Since the output ripple voltage is large when ESR is large, the capacitor with low ESR should be used to reduce the output ripple voltage. Generally, a ceramic capacitor is used for the output capacitor.

A minimum capacitor required considering the switching ripple voltage can be obtained as follows :

$$Co \geq \frac{1}{2\pi \times fosc \times \left(\frac{\Delta V_O}{\Delta IL} - ESR \right)}$$

Co : Output capacitor [F]

ESR : Serial resistance of output capacitor [Ω]

ΔV_O : Switching ripple voltage [V]

ΔIL : Peak-to-peak value of inductor ripple current [A]

fosc : Switching frequency [Hz]

Since overshoot occurs in a DC/DC output voltage when removing a battery being charged, it is necessary to secure sufficient voltage resistant tolerance. Generally, the capacitor with a rated withstanding voltage over a maximum input voltage is used.

In addition, use the capacitor with sufficient acceptable ripple current tolerance. The acceptable ripple current required can be obtained as follows:

$$Irms \geq \frac{\Delta IL}{2\sqrt{3}}$$

Irms : Acceptable ripple current (effective value) [A]

ΔIL : Peak-to-peak value of inductor ripple current [A]

• Selecting input capacitor

Select the input capacitor with ESR as small as possible. A ceramic capacitor is recommended. When a larger capacity of capacitor than ceramic capacitors should be used, use the polymer capacitor with low ESR or the tantalum capacitor.

The DC/DC switching operation causes the ripple voltage with the power supply voltage. Use the acceptable ripple voltage to examine the lower value of the input capacitor. The ripple voltage of the power supply can be simply obtained as follows :

$$\Delta V_{IN} = \frac{I_{OMAX}}{C_{IN}} \times \frac{V_O}{V_{IN} \times f_{OSC}} + ESR \times \left(I_{OMAX} + \frac{\Delta IL}{2}\right)$$

ΔV_{IN} : Peak-to-peak value of switching system power supply ripple voltage [V]

I_{OMAX} : Maximum charge current [A]

C_{IN} : Input capacitor [F]

V_{IN} : Switching system power supply voltage [V]

V_O : Charge voltage [V]

f_{OSC} : Switching frequency [Hz]

ESR : Series resistance component of input capacitor [Ω]

ΔIL : Peak-to-peak value of inductor ripple current [A]

The ripple voltage of the power supply can be decreased by raising the switching frequency besides using the capacitor.
The capacitor has the features in the frequency, temperature and bias voltage, so that the effect capacitance can be extremely small depending on the use conditions.

Please choose the one of having the enough margin for the input voltage and ripple current to ratings of the capacitor.

The acceptable ripple current is given by the following formula.

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}}$$

Irms : Acceptable ripple current (effective value) [A]

I_{OMAX} : Maximum charge current [A]

V_{IN} : Switching system power supply voltage [V]

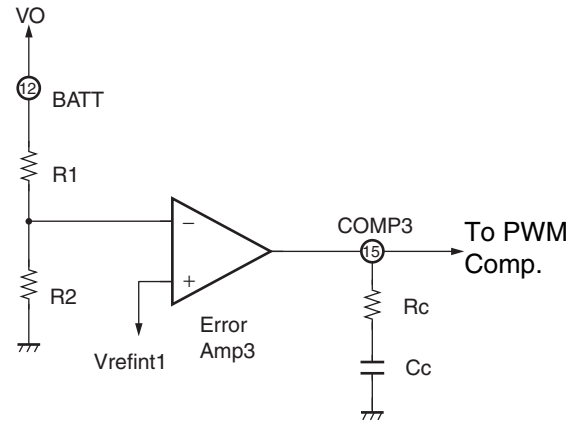
V_O : Charge voltage [V]

• Designing phase compensation circuit

(1) Constant voltage (CV) mode phase compensation circuit

If a capacitor with low ESR is used for the output capacitor, such as a ceramic capacitor, oscillation can be generated more easily since a phase delay by LC resonant frequency is close to +180 °C. In this case, the phase is compensated by connecting the phase advancing circuit with 1pole-1zero to the output pin (COMP3) of the error amplifier 3 (gm amplifier) .

1pole-1zero phase compensation circuit



As a reference, Rc (Ω) and Cc (F) of the phase advancing circuit can be obtained as follows :

$$Rc \fallingdotseq \frac{Io}{190 \times 10^{-6} \times V_{IN}} \times \sqrt{\frac{L}{Co}}$$

$$Cc \fallingdotseq \frac{\sqrt{L \times Co}}{Rc}$$

Io : Charge current [A]

V_{IN} : Switching system power supply voltage [V]

L : Inductance value of inductor [H]

Co : Output capacitor value [F]

Vo : Charge voltage [V]

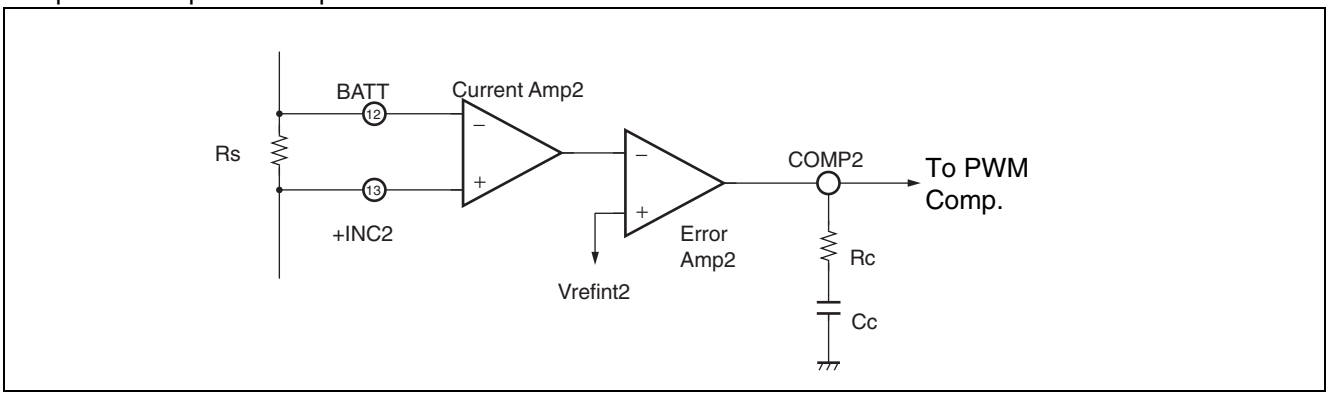
In addition, the crossover frequency fco [Hz] at this time can be obtained as follows :

$$f_{CO} \fallingdotseq 1 \times 10^{-5} \times \frac{V_{IN}}{Vo \times Cc}$$

(2) Constant current (CC) mode phase compensation circuit

Since the output capacitor impedance has a small influence to the loop response characteristics in this mode, the phase compensation circuit with 1pole-1zero is normally connected to the output pin (COMP2) of the error amplifier 2 (gm amplifier) .

1pole-1zero phase compensation circuit



As a standard, Rc (Ω) and Cc (F) of the phase advancing circuit can be obtained as follows :

$$Rc \fallingdotseq 1.2 \times 10^4 \times \frac{f_{CO} \times L}{Rs \times V_{IN}}$$

$$Cc \fallingdotseq \frac{\sqrt{L \times Co}}{Rc}$$

Rs : Resistance value of charge current detection [Ω]

V_{IN} : Switching system power supply voltage [V]

L : Inductance value [H]

Co : Output capacitance value [F]

f_{CO} : Crossover frequency [Hz]

- Acceptable loss and thermal design

  In most of the cases, it is not necessary for this IC to examine an acceptable loss and thermal design because of its high efficiency, however, it is necessary to examine them in usage under a high power supply voltage, high switching frequency, high load, or high temperature.

  The IC's internal loss (P_{IC}) can be obtained as follows :

  $$P_{IC} = V_{CC} \times (I_{CC} + Q_g \times f_{OSC})$$

  P_{IC} : IC's Internal loss [W]

  V_{CC} : Power supply voltage (V_{IN}) [V]

  I_{CC} : Power supply current [A] (4.0 mA Max)

  Q_g : Total amount of charges of all SWFETs [C] (when Vgs = 6 V)

  f_{OSC} : Switching frequency [Hz]

  The temperature at the joint part (Tj) can be obtained as follows :

  $$Tj = Ta + \theta ja \times P_{IC}$$

  Tj : Joint part temperature [°C]

  Ta : Ambient temperature [°C]

  θja : TSSOP-24 package thermal resistance (78 °C / W)

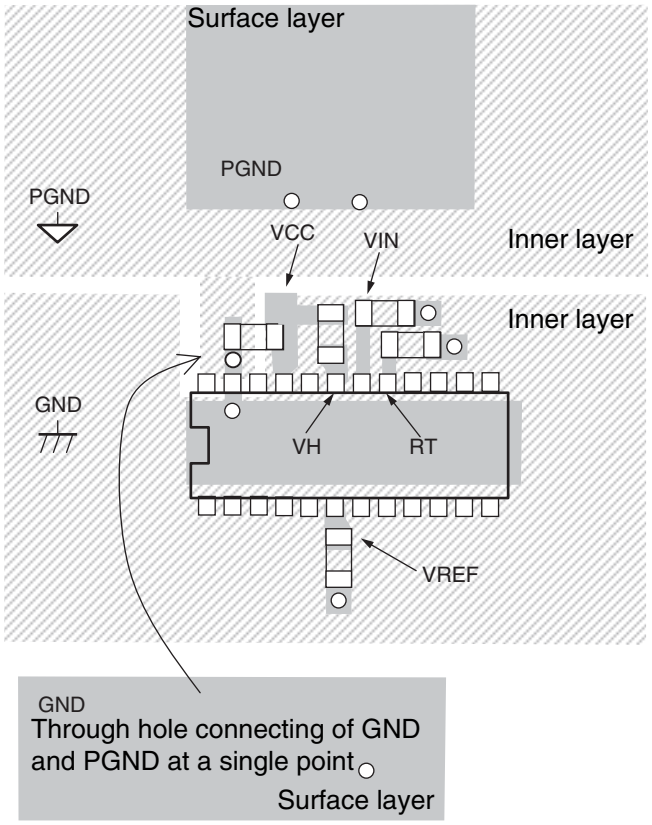
  P_{IC} : IC's internal loss [W]

- The board layout

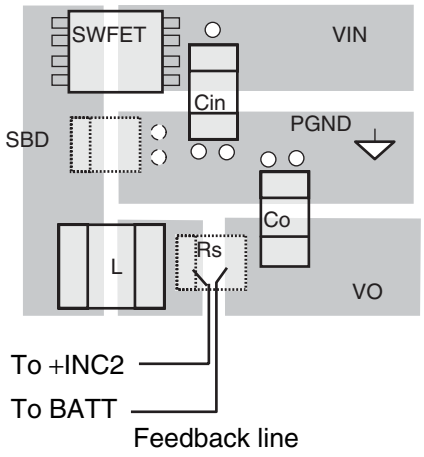
  When designing the layout, consider the points listed below.

  - Connect on the surface layer as much as possible the input capacitor (C_{IN}) , SWFET, SBD, inductor (L) , sense resistance (Rs) , and the output capacitor (Co) , and avoid connecting them via the through hole.
  - Design to make the current loop as small as possible with a special care for the loop configured by the input capacitor (C_{IN}) , SWFET, and SBD.
  - Connect GND pins of the input capacitor (C_{IN}) , SBD, and the output capacitor (Co) to GNDs on the inner layer via the through holes by making them close to the pins.
  - A large current flows momentarily at the net of OUT pin connecting to SWFET gate. Use the wiring width of about 0.8 mm as a standard to make wiring as shortly as possible.
  - Place bypass capacitors connecting to VCC, VIN, VREF, and VH pins and fosc setting resistance connecting to RT pin on the positions close to the pins as much as possible.
    In addition, GND pins of the VCC, VIN, and VREF bypass capacitors and fosc setting resistance should be connected so that they are close to GND pin on the IC as much as possible.
    (Make the through holes just close to GND pin of the IC and GND pin of the bypass capacitor fosc setting resistance to reinforce connection to inner GNDs.)
  - Since nets of −INC1, +INCx, BATT, COMPx, and RT pins are sensitive to noise, make wiring for them as shortly as possible, and keep them away from SW system parts as much as possible.
  - Since nets of +INC2 and BATT are extremely sensitive to noise, make Kelvin connection (remote sensing) making them as closely as possible each other, and keep them away from SW system parts as much as possible.
  - Set a solid area for GND on the IC mounting surface as much as possible. Connect the control system GND with PGND at a single point so that any large current path does not pass.

GND wiring example



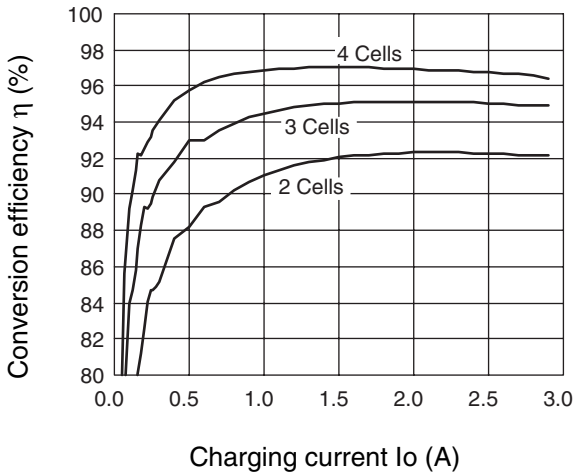
SW system part arrangement example



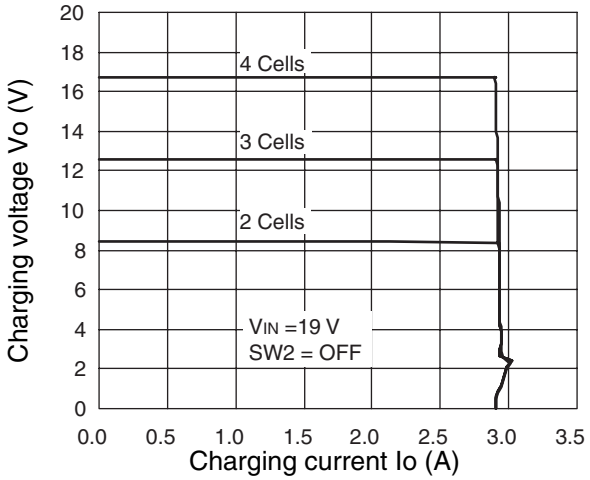
■ REFERENCE DATA

Unless explained specially, the measurement conditions are V_{IN} = 19 V, I_O = 2.85 A, Li+ battery 4 Cell, and Ta = + 25 °C.

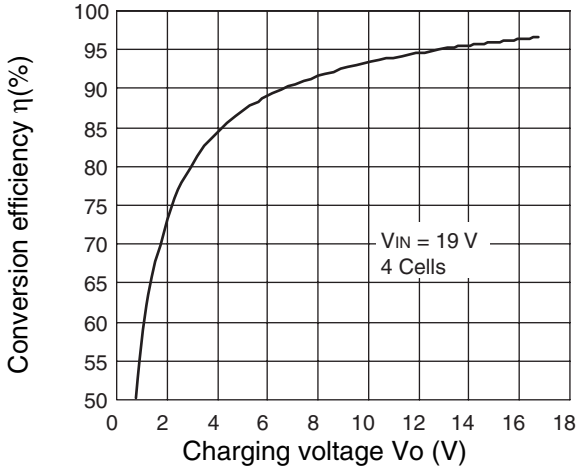
Conversion efficiency vs. Charging current
(Constant voltage mode)



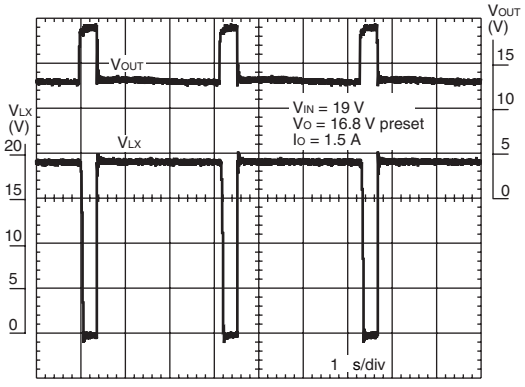
Charging voltage vs. Charging current



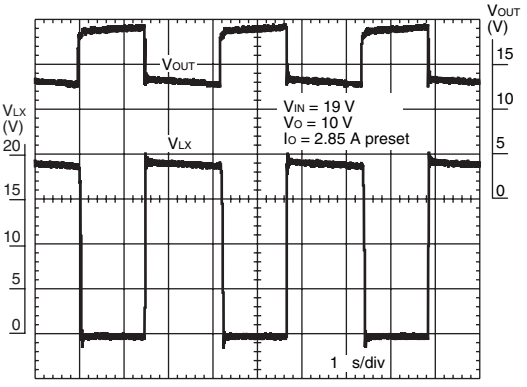
Conversion efficiency vs. Charging voltage
(Constant current mode)



Switching waveform
(Constant voltage mode)



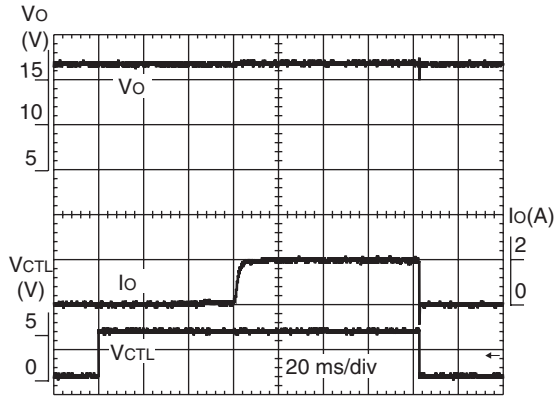
Switching waveform
(Constant current mode)



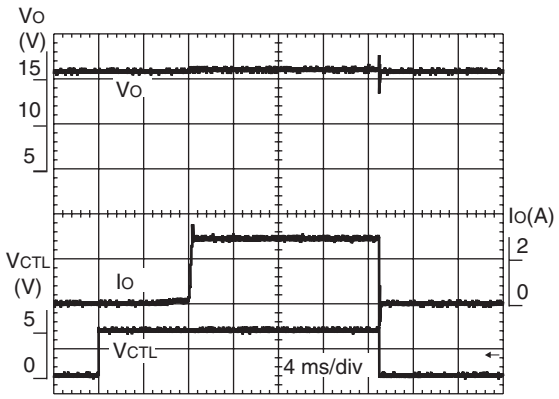
(Continued)

(Continued)

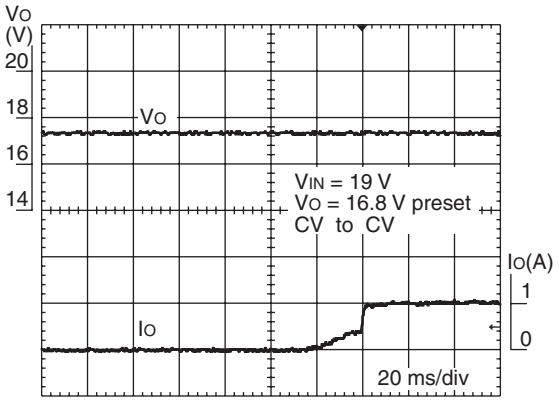
Start and stop
(Constant voltage mode)



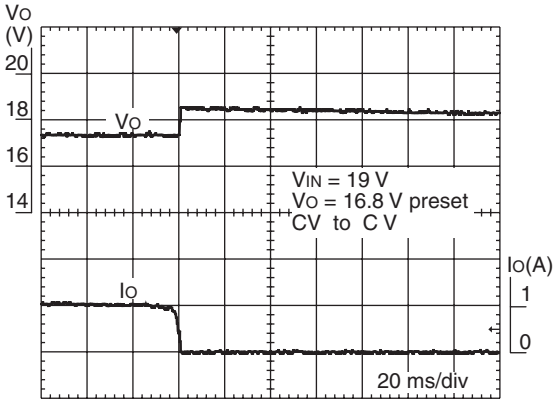
Start and stop
(Constant current mode)



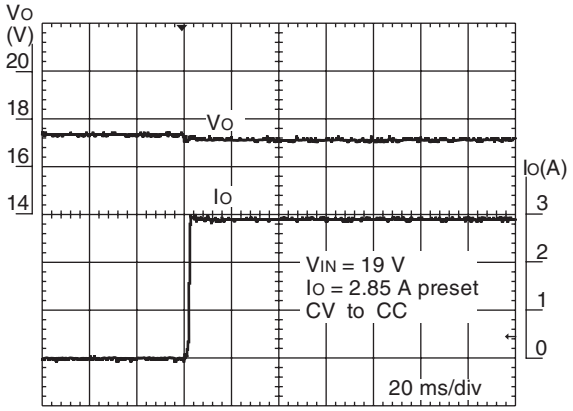
Load-step response
(Constant voltage mode)
Battery insertion



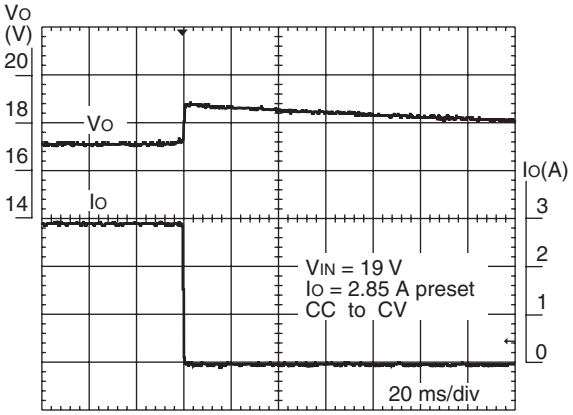
Load-step response
(Constant voltage mode)
Battery removal



Load-step operation response
(Constant current mode)
Battery insertion



Load-step operation response
(Constant current mode)
Battery removal



■ USAGE PRECAUTION

1. Do not configure the IC over the maximum ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to be normally operated within the recommended usage conditions. Usage outside of these conditions can have a bad effect on the reliability of the LSI.

2. Use the devices within recommended operating conditions

The recommended operating conditions are the recommended values that guarantee the normal operations of LSI.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed circuit board ground lines should be set up with consideration for common impedance

4. Take appropriate measures against static electricity

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1MΩ in series between body and ground.

5. Do not apply negative voltages

The use of negative voltages below −0.3 V may cause the parasitic transistor to be activated on LSI lines, which can cause malfunctions.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A134PFT-❑❑❑E1	24-pin plastic TSSOP (FPT-24P-M08)	Lead Free version

■ EV BOARD ORDERING INFORMATION

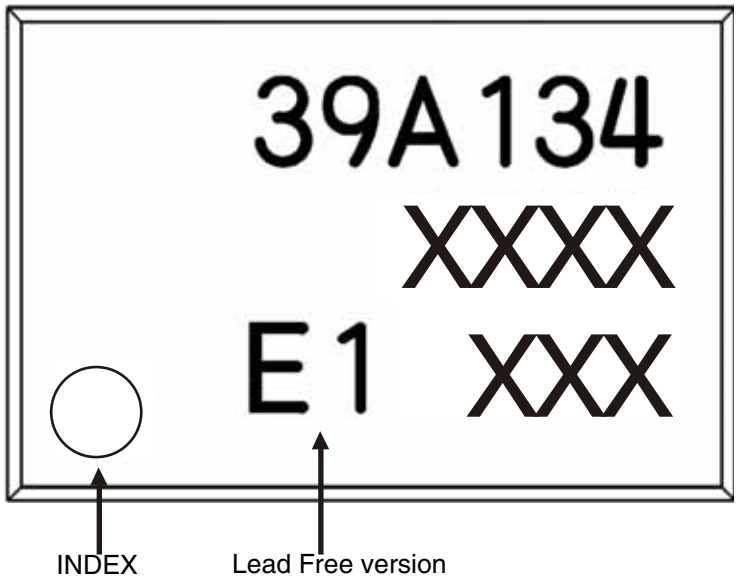
EV board part No.	EV board version No.	Remarks
MB39A134EVB-01D	MB39A134EVB-01 Rev1.0	TSSOP-24

■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

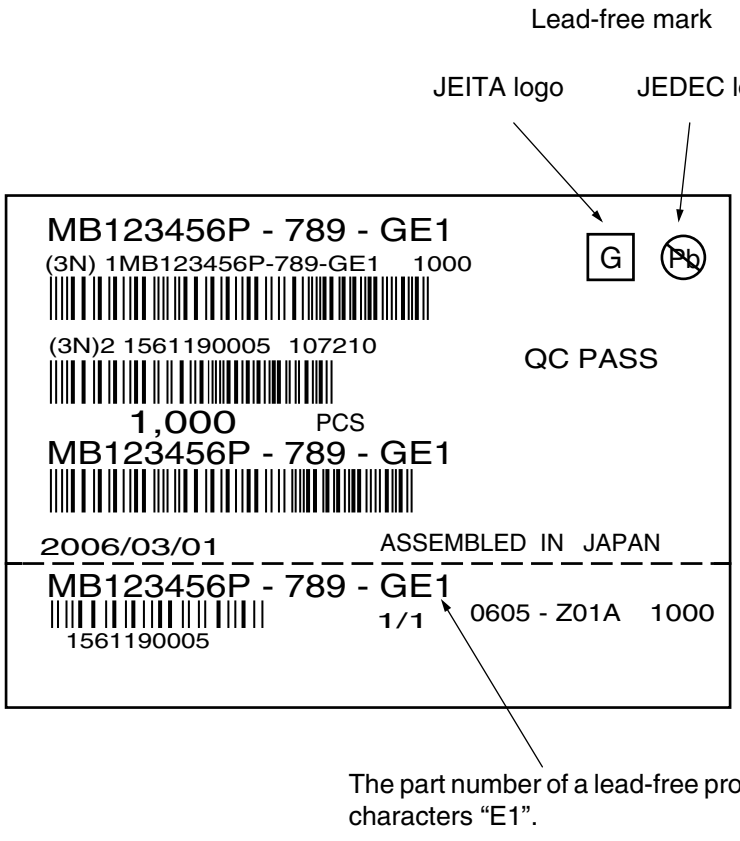
The LSI products of Fujitsu microelectronics with “E1” are compliant with RoHS Directive , and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB) , and polybrominated diphenyl ethers (PBDE) .

A products whose part number has trailing characters “E1” is RoHS compliant.

■ MARKING FORMAT (LEAD FREE VERSION)



■ LABELING SAMPLE (LEAD FREE VERSION)

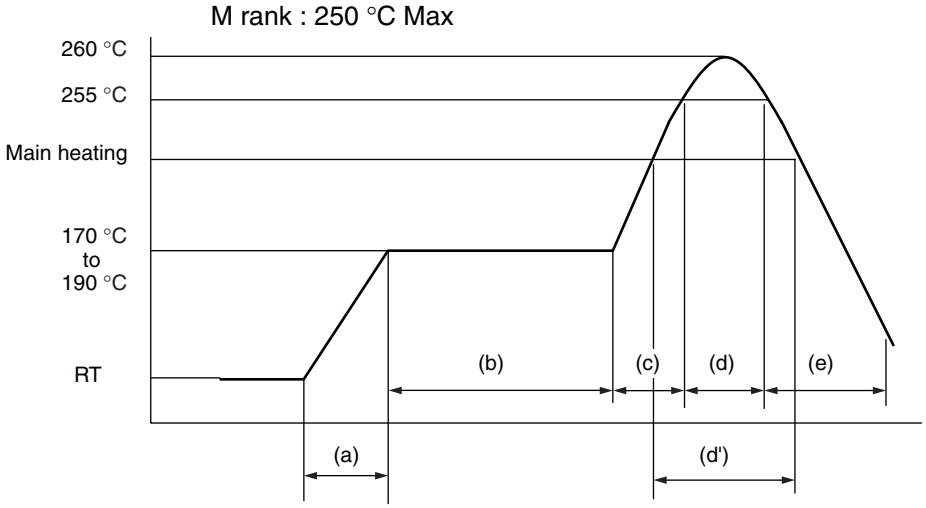


■ MB39A134PFT-❑❑❑E1
RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

Item	Condition	
Mounting Method	IR (infrared reflow) , Manual soldering (partial heating method)	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after Manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please process within 8 days after baking (125 °C, 24H)
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Mounting Conditions]

(1) IR (infrared reflow)



"H" level : 260 °C Max
(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60 s to 180 s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Peak temperature : Temperature 260 °C Max; 255 °C or more, 10 s or less
(d') Main Heating : Temperature 230 °C or more, 40 s or less
or
Temperature 225 °C or more, 60 s or less
or
Temperature 220 °C or more, 80 s or less
(e) Cooling : Natural cooling or forced cooling

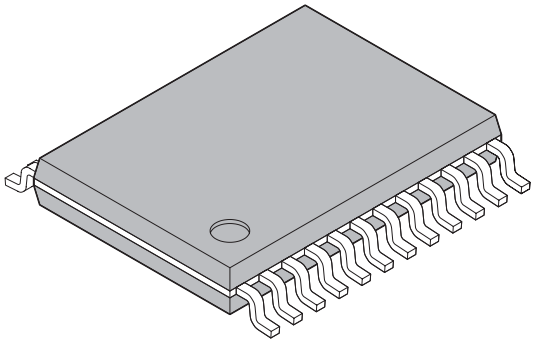
Note : Temperature : the top of the package body

(2) Manual soldering (partial heating method)

Conditions : Temperature 400 °C Max

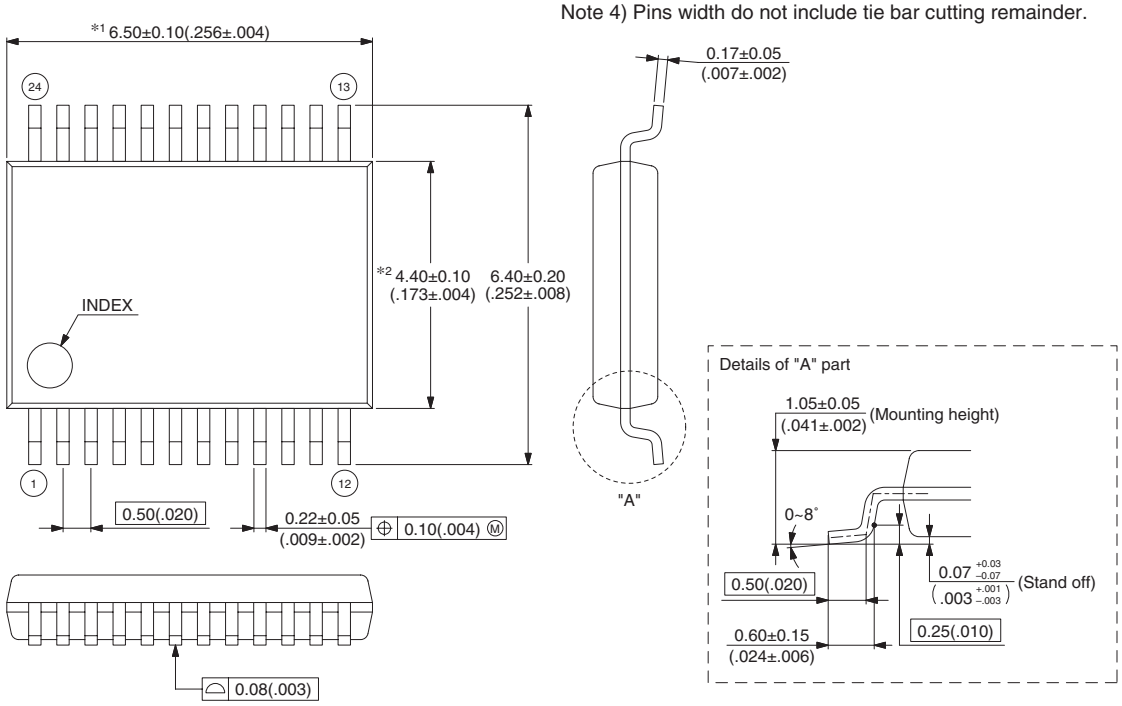
Times : 5 s max/pin

■ PACKAGE DIMENSION

24-pin plastic TSSOP		
	Lead pitch	0.50 mm
	Package width × package length	4.4 × 6.5 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.10 mm MAX
	Weight	0.08 g
(FPT-24P-M08)	Code (Reference)	P-TSSOP24-4.4×6.5-0.50

24-pin plastic TSSOP
(FPT-24P-M08)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

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http://cn.fujitsu.com/fmc/tw

Edited Strategic Business Development Dept.