T507&T507-H Datasheet

High-performance Quad-core 64-bit Intelligent Cockpit Processor

Revision 1.4

September 13, 2021

Revision History

Revision	Date	Description
1.0	Dec.31, 2019	Initial release version
1.1	Apr.24, 2020	Update the voltage range of VCC_LVDS in section 5.2.
1.2	Sep.30, 2020	Modify the ball name of N18 to USB_TEST in section 7.1.
1.3	Jun.25, 2021	1. Add the description of CPU cache. 2. Delete HDMI for T507, T517 3. Add T507 CX00H0YZ information Modify RGMII and RMII timing
1.4	September 13, 2021	1. Modify T507 CX00H0YZ to T507-H 2. Modify to a version only for T507 and T507-H 3. Update features

Declaration

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About This Document

Purpose

The document describes features of each module, pin/signal characteristics, voltage range, interface timing, thermal and package, and packing of T507/T507-H. For details about register descriptions of each module, see the ***Allwinner_T507&T507-H_User_Manual***.

CAUTION

The document defines two devices: T507 and T507-H. Unless other stated, their contents are consistent.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
WARNING	A warning means that injury or death is possible if the instructions are not obeyed.
CAUTION	A caution means that damage to equipment is possible.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical Conventions

The expressions of data capacity, frequency, and data rate are described as follows.

Type	Symbol	Value
Data capacity	1K	1024
	1M	1,048,576
	1G	1,073,741,824
Frequency, data rate	1k	1000
	1M	1,000,000
	1G	1,000,000,000

1. Overview

T507/T507-H is a high-performance quad-core Cortex™-A53 platform SoC for the new generation of automotive markets. T507/T507-H is qualified to Automotive AEC-Q100 testing. The chip family integrates Cortex™-A53 quad-core CPU, G31 MP2 GPU, 32-bit DDR3/LPDDR3/DDR4/LPDDR4 DRAM, multi video output interfaces (RGB/2*LVDS/HDMI/CVBS OUT), and multi video input interfaces (MIPI CSI/BT656/BT1120). The chip family supports 4K@30fps H.265 decoder, 4K@30fps VP9 decoder, 4K@30fps AVS2 decoder, 4K@25fps H.264 encoder, DI, 3D noise reduction, SmartColor system, and keystone correction module, which provides smooth user experience and professional visual effect. T507/T507-H can be used in IVI, digital cluster, HD AVM, HUD and other intelligent cockpit products.

1.1. Device Difference

The main differences among T507 and T507-H are summarized in Table 1-1.

Table 1-1. Device Difference Details

Contents	T507	T507-H
Wire	Copper wire	Copper wire
HDMI	Not support	Support

2. Features

2.1. CPU Architecture

- Quad-core ARM Cortex™-A53 processor
- Power-efficient ARM v8 architecture
- 32 KB L1 I-cache + 32 KB L1 D-cache per core, and 512 KB L2 cache
- 64 and 32bit execution states for scalable high performance
- Trustzone technology supported
- Supports NEON Advanced SIMD instruction for acceleration of media and signal processing functions
- Large Physical Address Extensions (LPAE)
- VFPv4 Floating Point Unit

2.2. GPU Architecture

- G31 MP2
- Supports OpenGL ES 1.0/2.0/3.2, Vulkan 1.1, OpenCL 2.0

2.3. Memory Subsystem

2.3.1. Boot ROM

- On-chip memory
- Supports system boot from the following devices:
  - SD/eMMC (SMHC0, SMHC2)
  - Nand Flash
  - SPI Nor Flash
  - SPI Nand Flash
- Supports secure boot and normal boot
- Supports mandatory upgrade process through SMHC0 and USB
- Secure brom supports load only certified firmware
- Secure brom ensures that the secure boot is a trusted environment

2.3.2. SDRAM

- 32-bit DDR4/DDR3/DDR3L/LPDDR3/LPDDR4 interface
- Maximum 792 MHz working frequency for DDR4
- Maximum 792 MHz working frequency for DDR3/DDR3L
- Maximum 792 MHz working frequency for LPDDR3
- Maximum 792 MHz working frequency for LRDDR4
- Memory capacity up to 4 GB

2.3.3. NAND Flash

- Compliant with ONFI 2.0 and Toggle 2.0
- Up to 80-bit ECC per 1024 bytes
- Supports 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports 2 chip selects, and 2 ready_busy signals

- Supports SLC/MLC/TLC flash and EF-NAND
- Supports SDR/Toggle DDR/ONFI DDR NAND interface

2.3.4. SMHC

- Three SD/MMC host controller (SMHC) interfaces
- SMHC0 controls the devices that comply with the Secure Digital (SD3.0)
  - 4-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- SMHC1 controls the devices that comply with the Secure Digital Input/Output (SDIO3.0)
  - 4-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- SMHC2 controls the devices that comply with the Multimedia Card (eMMC5.0)
  - 8-bit bus width
  - SDR mode 50 MHz@3.3V IO pad
  - SDR mode 150 MHz@1.8V IO pad
  - DDR mode 50 MHz@3.3V IO pad
  - DDR mode 100 MHz@1.8V IO pad
- Supports hardware CRC generation and error detection
- Supports block size of 1 to 65535 bytes

2.4. Video Engine

2.4.1. Video Decoding

- Supports video decoding up to 4K@30fps
- Supports multi-formats:
  - H.265 Main10@L5.1 up to 4K@30fps
  - VP9 Profile 2 up to 4K@30fps
  - AVS2 JiZhun 10bit Profile up to 4K@30fps
  - H.264 BP/MP/HP@L4.2 up to 4K@30fps
  - H.263 BP up to 1080p@60fps
  - MPEG-4 SP/ASP@L5 up to 1080p@60fps
  - MPEG-2 MP/HL up to 1080p@60fps
  - MPEG-1 MP/HL up to 1080p@60fps
  - Xvid up to 1080p@60fps
  - Sorenson Spark up to 1080p@60fps
  - VP8 up to 1080p@60fps
  - AVS/AVS+ JiZhun Profile up to 1080p@60fps
  - WMV9/VC1 SP/MP/AP up to 1080p@60fps
  - JPEG HFIF file format up to 45 MPPS

2.4.2. Video Encoding

- H.264 BP/MP/HP
- H.264 supports I/P frame, and only supports single reference frame
- MJPEG/JPEG baseline
- Maximum 16-megapixel (4096 x 4096) resolution for H.264 encoding
- H.264 encoding capability: 4K@25fps
- JPEG snapshot performance of 1080p@60fps independently
- Supports the constant bit rate (CBR)/variable bit rate (VBR) bit rate control mode, ranging from 256 kbit/s to 100

Mbit/s

- Encoding of eight regions of interest (ROIs)

2.5. Video and Graphics

2.5.1. Display Engine (DE)

- Output size up to 4096 x 2048
- Six configurable alpha blending channels
- Four overlay layers in each channel, and has an independent scaler
- Potter-duff compatible blending operation
- Supports AFBC buffer
- Input format: semi-planar YUV422/YUV420/YUV411/P010/P210 and planar YUV422/YUV420/YUV411, ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data
- Supports 10-bit processing path for HDR video
- Supports SDR/HDR10/Hybrid-log gamma EOTF and color space conversion
- Supports SmartColor™ 3.3 for excellent display experience
  - Adaptive detail/edge enhancement
  - Adaptive color enhancement and fresh tone protection
  - Adaptive contrast enhancement
  - Adaptive de-noising for compression noise or mosquito noise with YUV420/422 input
- Supports write back only for high efficient dual display and miracast
- Supports output format YUV444/YUV422/YUV420/RGB444 for 10/8bit

2.5.2. De-interlacer (DI)

- Supports off-line processing mode only
- Supports 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined input data format
- Supports 8-bit NV12/NV21/YV12 and planar YUV422/planar YUV422 UV-combined output data format for DIT, and YV12/planar YUV422 output data format for TNR
- Supports video resolution from 32 x 32 to 2048 x 1280 pixel
- Supports weave/pixel-motion-adaptive de-interlace method
- Supports temporal noise reduction function
- Supports film mode detection with video-on-film detection
- Performance: Module clock 150 MHz for 1080p@60Hz

2.5.3. Graphic 2D (G2D)

- Supports layer size up to 2048 x 2048 pixels
- Supports input/output formats: YUV422 (semi-planar and planar format)/YUV420 (semi-planar and planar format)/P010/P210/P410/Y8/ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/ARGB2101010 and RGB565
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

2.6. System Peripherals

2.6.1. Timer

- The timer module implements the timing and counting functions, including Timer0, Timer1, Watchdog and AVS0, AVS1
- Timer0 and Timer1 for system scheduler counting
  - Configurable 8 prescale factors
  - Programmable 32-bit down timer
  - Supports two working modes: continue mode and single count mode

  - Generates an interrupt when the count is decreased to 0
- 1 Watchdog for transmitting a reset signal to reset the entire system after an exception occurs in the system
  - Supports 12 initial values to configure
  - Generation of timeout interrupts
  - Generation of reset signal
  - Watchdog restart the timing
- 2 AVS counters (AVS0 and AVS1) for synchronizing video and audio in the player
  - Programmable 33-bit up timer
  - Initial value can be updated anytime
  - 12-bit frequency divider factor
  - Pause/Start function

2.6.2. High Speed Timer

- One high speed timer with 56-bit counter
- Configurable 5 prescale factor
- Clock source is synchronized with AHB1 clock, much more accurate than other timers
- Supports 2 working modes: continuous mode and single mode
- Generates an interrupt when the count is decreased to 0

2.6.3. RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- External connect a 32.768 kHz low-frequency oscillator for count clock
- Supports one solution without low-frequency crystal, a precise 32.768 kHz counter clock can be generated by using HOSC to calibrate the internal RC clock
- Configurable initial value by software anytime
- Periodically alarm to wakeup the external devices
- 16 general purpose registers for storing power-off information

2.6.4. GIC

- Supports 16 Software Generated Interrupts (SGIs), 16 Private Peripheral Interrupts (PPIs) and 160 Shared Peripheral Interrupts (SPIs)
- Enabling, disabling, and generating processor interrupts from hardware interrupt
- Interrupt masking and prioritization

2.6.5. DMA

- Up to 16-channel DMA
- Interrupt generated for each DMA channel
- Flexible data width of 8/16/32/64-bit
- Supports linear and IO address modes
- Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral
- Supports transfer with linked list
- DRQ response includes wait mode and handshake mode
- DMA channel supports pause function

2.6.6. CCU

- 13 PLLs
- One on-chip RC oscillator

- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Supports clock configuration and clock generated for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

2.6.7. Thermal Sensor Controller

- Temperature accuracy: ±3°C from 0°C to +100°C, ±5°C from -25°C to +125°C
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Averaging filter for thermal sensor reading
- Four thermal sensors: sensor0 located in the GPU, sensor1 located in the VE, sensor2 located in the CPU and sensor3 located in the DDR

2.6.8. CPU Configuration

- Capable of CPU reset, including core reset, debug circuit reset, etc
- Capable of other CPU-related control, including interface control and CP15 control
- Capable of checking CPU status, including idle status, SMP status, and interrupt status, etc
- Including CPU debug control and status register

2.6.9. IOMMU

- Supports virtual address to physical address mapping by hardware implementation
- Supports DE, DI, VE_R, VE, CSI0, CSI1, G2D parallel address mapping
- Supports DE, DI, VE_R, VE, CSI0, CSI1, G2D bypass function independently
- Supports DE, DI, VE_R, VE, CSI0, CSI1, G2D prefetch independently
- Supports DE, DI, VE_R, VE, CSI0, CSI1, G2D interrupt handing mechanism independently
- Supports 2 levels TLB (level1 TLB for special using, and level2 TLB for sharing)
- Supports TLB Fully cleared and Partially disabled
- Supports trigger PTW behavior when TLB miss
- Supports checking the permission

2.7. Image Input

- Supports 1 serial interface(MIPI) + 1 parallel interface
- Supports image crop function
- Parallel interface
  - Supports 8-bit DC interface
  - Supports BT656, BT601, BT1120 interface
  - Supports ITU-R BT.656 time-multiplexed format up to 4*720p@30fps in DDR sample mode
  - Supports progress and interleave video input
  - Maximum video capture resolution for parallel interface to 5M@15fps or 1080p@30fps
  - Maximum pixel clock for parallel to 148.5 MHz
- MIPI interface
  - Supports MIPI Version 1.0
  - Up to 1.0Gbps/Lane
  - Maximum video capture resolution for serial interface up to 8M@30fps or 4*1080p@25fps
  - Supports interlaced mode
- Camera control interface
  - Compatible with i2c transmission in 7 bit slave ID + 1 bit R/W
  - Automatic transmission
  - 0/8/16/32 bit register address supported
  - 8/16/32 bit data supported
  - 64bytes-FIFO input CCI data supported
  - Synchronized with CSI signal and delay trigger supported
  - Repeated transmission with sync signal supported

2.8. Video Output

2.8.1. TCON_LCD

- RGB interface with DE/SYNC mode, up to 1920 x 1080@60fps
- Serial RGB/dummy RGB interface, up to 800 x 480@60fps
- i8080 interface, up to 800 x 480@60fps
- BT656 interface, up to 1280 x 720@60fps or 1920 x 1080@30fps
- Supports RGB888, RGB666 and RGB565 with dither function
- Supports Gamma correction with R/G/B channel independence
- Supports dual link LVDS interface
  - Dual link up to 1920 x 1080@60fps
  - Single link up to 1366 x 768@60fps
  - LVDS pins are multiplexed with that of RGB

2.8.2. TCON_TV

- Supports 10-bit pixel depth YUV422/YUV420, HV format output up to 4K@60Hz
- Supports 8-bit pixel depth YUV444, HV format output up to 4K@60Hz

2.8.3. TVE

- Supports 1-ch TV CVBS output
- Supports NTSC and PAL mode
- Plug status auto detecting

2.8.4. HDMI (Only for T507-H)

- Compatible with HDCP 2.2 and HDCP 1.4
- Supports DDC and SCDC
- Integrated CEC hardware engine
- Video support
  - 2D Video: 4K/1080P/1080I/720P/576P/480P/576I/480I, up to 4K@30fps
  - 3D Video: 4K/1080P/720P/576P/480P, up to 4K@30fps
  - Supports RGB888/YUV444/YUV422 output
  - Color depth: 8/10-bit
  - HDR10: compliant with CTA-861.3 and SMPTE ST 2048
- Audio support
  - Uncompressed audio formats: IEC60985 L-PCM audio samples, up to 192 kHz
  - Compressed audio formats: IEC61937 compressed audio, up to 1536 kHz

2.9. Audio Subsystem

2.9.1. Audio Codec

- Two audio digital-to-analog (DAC) channels
  - Supports 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95±2dB SNR@A-weight, -80±3dB THD+N, output Level more than 0.55Vrms
- One audio output:
  - One differential LINEOUTP/N or single-ended LINEOUTL/R output
- Supports Dynamic Range Controller adjusting the DAC playback
- One 128x24-bits FIFO for DAC data transmit

- Programmable FIFO thresholds
- DMA and Interrupt support

2.9.2. Audio HUB

- One Audio HUB
- Supports 2 Digital Audio MIXER (DAM)
- Supports 3 I2S/PCM interfaces for connecting external devices, and 1 I2S/PCM for connecting internal HDMI
- Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode
- I2S mode supports 8 channels, and 32-bit/192kbit sample rate
- I2S and TDM modes support maximum 16 channels, and 32-bit/96kbit sample rate

2.9.3. DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

2.9.4. One Wire Audio (OWA)

- One OWA TX
- IEC-60958 transmitter functionality
- Compliance with S/PDIF Interface
- Supports channel status insertion for the transmitter
- Hardware parity generation on the transmitter
- One 128×24bits TXFIFO for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support
- Supports 16-bit, 20-bit and 24-bit data formats

2.10. Security Engine

2.10.1. Crypto Engine (CE)

- Supports Symmetrical algorithm: AES, DES, TDES, XTS
  - ECB, CBC, CTS, CTR, CFB, OFB, CBC-MAC mode for AES
  - 128/192/256-bit key for AES
  - 256-bit, 512-bit key for XTS
  - ECB, CBC, CTR, CBC-MAC mode for DES/TDES
- Supports Hash algorithm: MD5, SHA, HMAC
  - SHA1, SHA224, SHA256, SHA384, SHA512 for SHA
  - HMAC-SHA1, HMAC-SHA256 for HMAC
  - MD5, SHA, HMAC are padded using hardware
- Supports Asymmetrical algorithm: RSA, ECC
  - RSA supports 512/1024/2048/4096-bit width
  - ECC supports 160/224/256/384/521-bit width
- Supports 160-bit hardware PRNG
- Supports 256-bit hardware TRNG
- Internal embedded DMA to do data transfer
- Supports secure and non-secure interfaces respectively
- Supports task chain mode for each request. Task or task chain are executed at request order
- 8 scatter group (sg) are supported for both input and output data
- DMA has multiple channels, each channel corresponds one suit of algorithm

2.10.2. Security ID

- Supports 2 Kbits EFUSE for chip ID and security application
- EFUSE has secure zone and non-secure zone

2.10.3. Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Set secure area of DRAM
- Set secure property that Master accesses to DRAM
- Set DRM area
- Set whether DRM master can access to DRM area or not

2.10.4. Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Set secure property of peripherals

2.11. External Peripherals

2.11.1. USB

- One USB 2.0 OTG (USB0), with integrated USB 2.0 analog PHY
  - Compatible with USB2.0 Specification
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) in host mode
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) in device mode
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a for host mode
  - Up to 8 User-Configurable Endpoints (EPs) for Bulk, Isochronous and Interrupt bi-directional transfers
  - Supports (4 KB+64 Bytes) FIFO for all EPs (including EP0)
  - Supports point-to-point and point-to-multipoint transfer in both host and peripheral mode
- Three USB 2.0 HOST (USB1, USB2, USB3), with integrated USB 2.0 analog PHY
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
  - Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) device
  - Only USB2 supports USB standby

2.11.2. EMAC

- Two EMAC interfaces for connecting external Ethernet PHY
  - EMAC0: 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces
  - EMAC1: 10/100 Mbps Ethernet port with RMII interface
  - EMAC0 and EMAC1 can use at the same time
- Compliant with IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operation
- Supports MDIO
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Supports a variety of flexible address filtering modes
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention; each descriptor can transfer up to 4 KB of data
- Comprehensive status reporting for normal operation and transfers with errors

- 4 KB TXFIFO for transmission packets and 16 KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions

2.11.3. UART

- Up to 6 UART controllers (UART0, UART1, UART2, UART3, UART4, UART5)
- UART0, UART5: 2-wire; UART1, UART2, UART3,UART4: 4-wire
- 2-wire UART can be used for printing; 4-wire UART can be used for flow control
- Compatible with industry-standard 16550 UARTs
- Capable of speed up to 4 Mbit/s
- Supports 5 to 8 data bits and 1/1.5/2 stop bits
- Supports even, odd or no parity
- Supports DMA controller interface
- Supports software/hardware flow control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode

2.11.4. SPI

- Up to 2 SPI controllers (SPI0, SPI1)
- Full-duplex synchronous serial interface
- Master/slave configurable
- Mode0~3 are supported for both transmit and receive operations
- Two 64 bytes FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI-CS) and SPI Clock (SPI-CLK) are configurable
- Interrupt or DMA support
- Supports 3-wire/4-wire SPI
- Supports programmable serial data frame length: 1-bit to 32-bit
- Supports Standard SPI, Dual-Output/Dual-Input SPI, Dual IO SPI, Quad-Output/Quad-Input SPI

2.11.5. Two Wire Interface (TWI)

- Up to 6 TWI controllers (TWI0, TWI1, TWI2, TWI3, TWI4, S_TWI0)
- Software-programmable for slave or master
- Supports repeated START signal
- Multi-master system supported
- Allows 10-bit addressing transactions
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s)
- Allows operation from a wide range of input clock frequency
- TWI driver supports packet transmission and DMA when TWI works in Master mode

2.11.6. CIR Receiver

- Full physical layer implementation
- Supports NEC format infrared data
- Supports CIR for remote control or wireless keyboard
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

2.11.7. PWM

- 6 PWM channels(3 PWM pairs: PWM01, PWM23, PWM45)
- Supports pulse, cycle and complementary pair output
- Supports capture input
- Programming deadzone output
- Build-in the programmable dead-time generator, controllable dead-time
- Three kinds of output waveform: continuous waveform, pulse waveform and complementary pair
- Output frequency range: 0–24 MHz/100 MHz
- Various duty-cycle: 0–100%
- Minimum resolution: 1/65536
- Interrupt generation of PWM output and capture input

2.11.8. Low Rate ADC (LRADC)

- One LRADC input channel
- 6-bit resolution
- Sample rate up to 2 kHz
- Supports hold Key and general Key
- Supports normal, continue and single work mode
- Power supply voltage: 1.8 V, power reference voltage: 1.35 V, analog input and detected voltage range: 0 to LEVELB (the maximum value is 1.266 V)

2.11.9. General Purpose ADC (GPADC)

- 12-bit resolution
- 8-bit effective successive approximation register (SAR) type A/D converter
- Power reference voltage: 1.8 V, analog input voltage range: 0 to 1.8 V
- Maximum sampling frequency: 1 MHz
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode

2.11.10. Transport Stream Controller (TSC)

- Supports SPI/SSI interface, interface timing parameters are configurable
- 32 channels PID filter for each TSF
- Supports multiple transport stream packet (188, 192, 204) format
- Hardware packet synchronous byte error detecting
- Hardware PCR packet detecting
- 64x16-bits FIFO for TSG, 64x32-bits FIFO for TSF
- Configurable SPI transport stream generator for streams in DRAM memory
- Supports DVB-CSA V1.1, DVB-CSA V2.1 Descrambler

2.11.11. Smart Card Reader (SCR)

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) Specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Supports adjustable clock rate and bit rate
- Configurable automatic byte repetition

- Supports commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Supports FIFOs for receive and transmit buffers (up to 128 characters) with threshold
- Supports configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Supports synchronous and any other non-ISO 7816 and non-EMV cards

2.12. Package

- TFBGA421 balls, 0.65 mm ball pitch, 0.35 mm ball size, 15 mm x 15 mm body

3. Block Diagram

Figure 3-1 shows the system block diagram of the T507/T507-H.

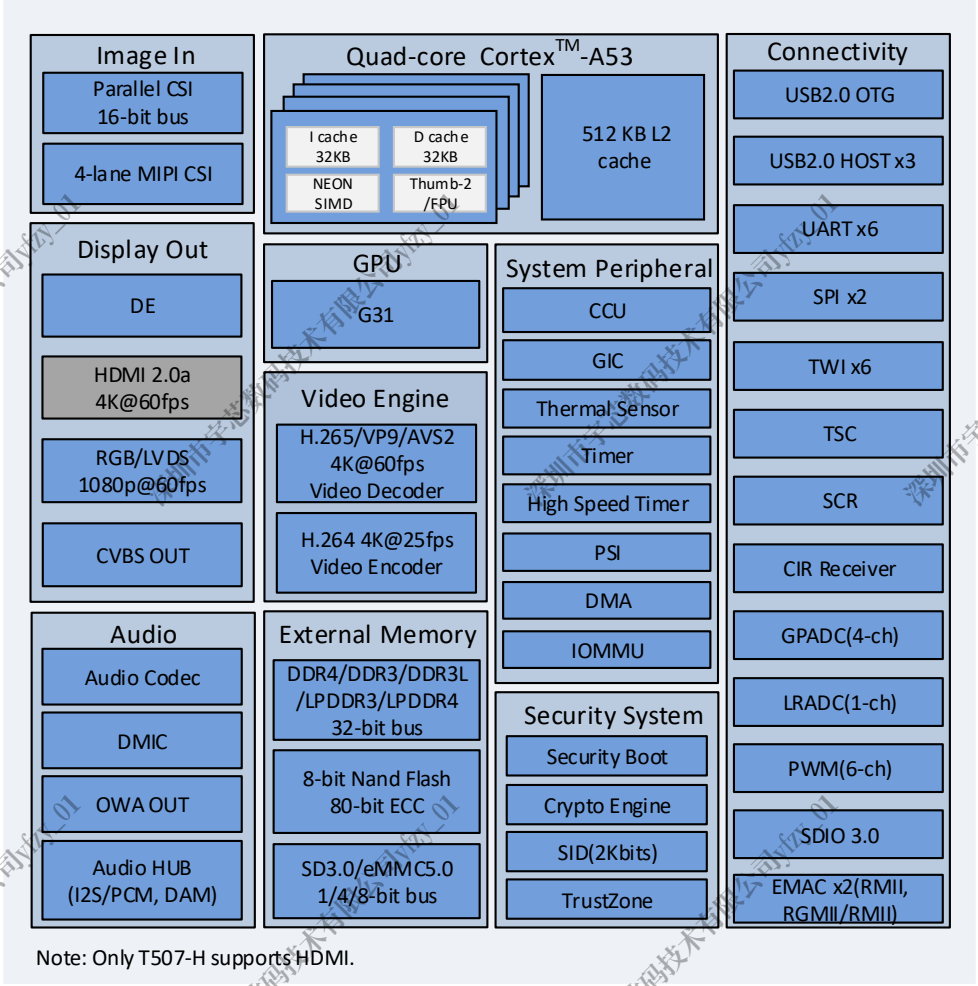


Figure 3-1. T507/T507-H System Block Diagram

Figure 3-2 shows the typical application diagram of the T507/T507-H.

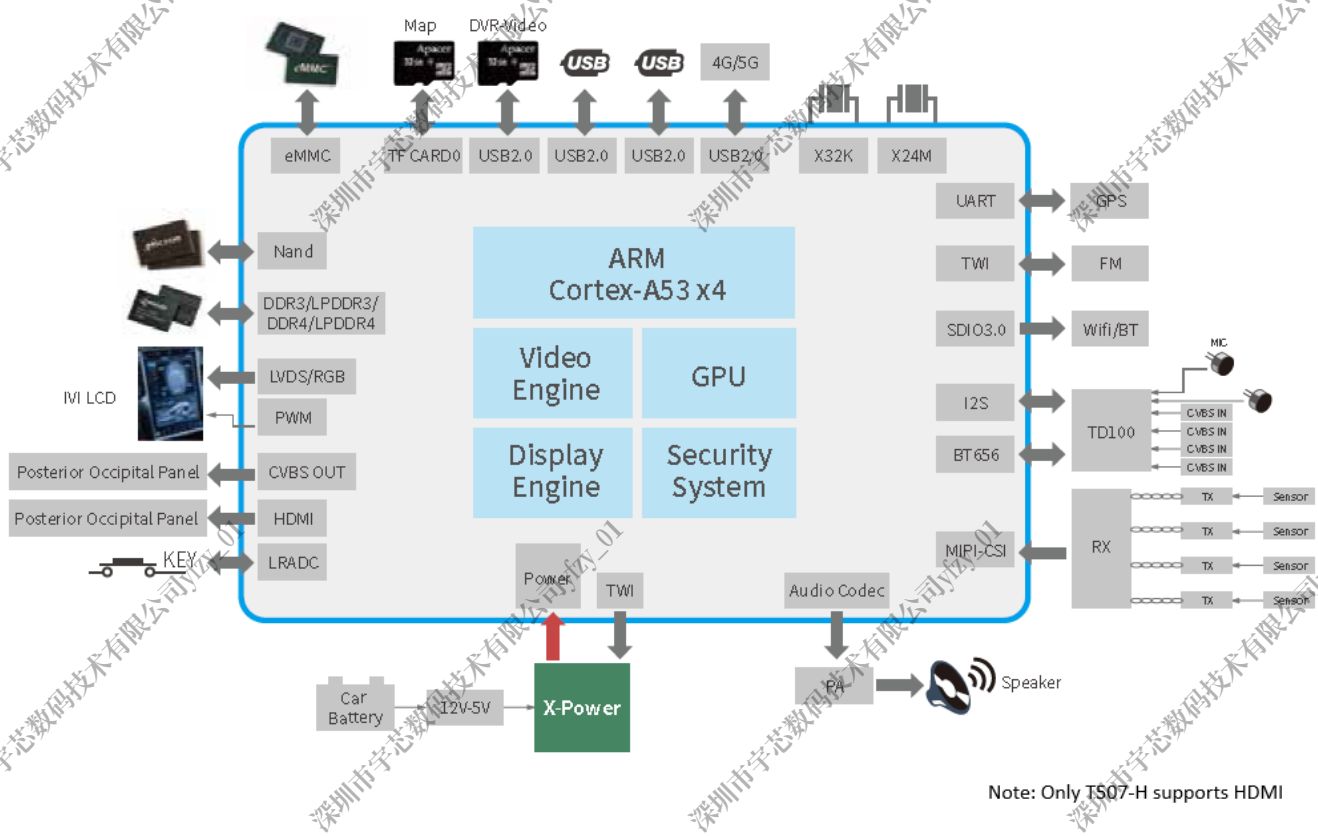


Figure 3-2. T507/T507-H Typical Application Diagram

4. Pin Description

4.1. Pin Quantity

Table 4-1 lists the pin quantity of the T507/T507-H.

Table 4-1. Pin Quantity

Pin Type	Quantity
I/O	275
Power	44
Ground	92
DDR Power	10
Total	421

4.2. Pin Characteristics

Table 4-2 lists the characteristics of the T507/T507-H pins from the following seven aspects.

[1].Ball#: Package ball numbers associated with each signals.

[2].Pin Name: The name of the package pin.

[3].Type: Denotes the signal direction

I (Input),
O (Output),
I/O (Input/Output),
OD (Open-Drain),
A (Analog),
AI (Analog Input),
AO (Analog Output),
P (Power),
G (Ground)

[4].Ball Reset State: The state of the terminal at reset. PU: pull up; PD: pull down; Z: high impedance.

[5].Pull Up/Down: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled by software.

[6].Default Buffer Strength: Defines default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

[7].Power Supply: The voltage supply for the terminal's IO buffers.

Table 4-2. Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
SDRAM						
AB17	SA0	O	Z	NA	NA	VCC_DRAM
V15	SA1	O	Z	NA	NA	VCC_DRAM
Y13	SA2	O	Z	NA	NA	VCC_DRAM
AA15	SA3	O	Z	NA	NA	VCC_DRAM
AB12	SA4	O	Z	NA	NA	VCC_DRAM
V12	SA5	O	Z	NA	NA	VCC_DRAM
W12	SA6	O	Z	NA	NA	VCC_DRAM
AC18	SA7	O	Z	NA	NA	VCC_DRAM
AB16	SA8	O	Z	NA	NA	VCC_DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
AA18	SA9	O	Z	NA	NA	VCC_DRAM
AC16	SA10	O	Z	NA	NA	VCC_DRAM
AA16	SA11	O	Z	NA	NA	VCC_DRAM
AA20	SA12	O	Z	NA	NA	VCC_DRAM
W15	SA13	O	Z	NA	NA	VCC_DRAM
AC12	SA14	O	Z	NA	NA	VCC_DRAM
Y12	SA15	O	Z	NA	NA	VCC_DRAM
AB13	SA16	O	Z	NA	NA	VCC_DRAM
U2	SDQ0	I/O	Z	NA	NA	VCC_DRAM
U1	SDQ1	I/O	Z	NA	NA	VCC_DRAM
V3	SDQ2	I/O	Z	NA	NA	VCC_DRAM
V2	SDQ3	I/O	Z	NA	NA	VCC_DRAM
AA1	SDQ4	I/O	Z	NA	NA	VCC_DRAM
Y2	SDQ5	I/O	Z	NA	NA	VCC_DRAM
Y3	SDQ6	I/O	Z	NA	NA	VCC_DRAM
AA2	SDQ7	I/O	Z	NA	NA	VCC_DRAM
AC3	SDQ8	I/O	Z	NA	NA	VCC_DRAM
AB3	SDQ9	I/O	Z	NA	NA	VCC_DRAM
AA3	SDQ10	I/O	Z	NA	NA	VCC_DRAM
V4	SDQ11	I/O	Z	NA	NA	VCC_DRAM
V5	SDQ12	I/O	Z	NA	NA	VCC_DRAM
W4	SDQ13	I/O	Z	NA	NA	VCC_DRAM
W5	SDQ14	I/O	Z	NA	NA	VCC_DRAM
Y6	SDQ15	I/O	Z	NA	NA	VCC_DRAM
AC4	SDQ16	I/O	Z	NA	NA	VCC_DRAM
AB4	SDQ17	I/O	Z	NA	NA	VCC_DRAM
AA4	SDQ18	I/O	Z	NA	NA	VCC_DRAM
V6	SDQ19	I/O	Z	NA	NA	VCC_DRAM
Y9	SDQ20	I/O	Z	NA	NA	VCC_DRAM
V10	SDQ21	I/O	Z	NA	NA	VCC_DRAM
V9	SDQ22	I/O	Z	NA	NA	VCC_DRAM
W9	SDQ23	I/O	Z	NA	NA	VCC_DRAM
AC6	SDQ24	I/O	Z	NA	NA	VCC_DRAM
AB5	SDQ25	I/O	Z	NA	NA	VCC_DRAM
AA5	SDQ26	I/O	Z	NA	NA	VCC_DRAM
AB6	SDQ27	I/O	Z	NA	NA	VCC_DRAM
AB8	SDQ28	I/O	Z	NA	NA	VCC_DRAM
AB9	SDQ29	I/O	Z	NA	NA	VCC_DRAM
AC8	SDQ30	I/O	Z	NA	NA	VCC_DRAM
AA8	SDQ31	I/O	Z	NA	NA	VCC_DRAM
AB2	SDQM0	O	Z	NA	NA	VCC_DRAM
W6	SDQM1	O	Z	NA	NA	VCC_DRAM
W10	SDQM2	O	Z	NA	NA	VCC_DRAM

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
AA9	SDQM3	O	Z	NA	NA	VCC_DRAM
W1	SDQS0P	I/O	Z	NA	NA	VCC_DRAM
Y4	SDQS1P	I/O	Z	NA	NA	VCC_DRAM
V7	SDQS2P	I/O	Z	NA	NA	VCC_DRAM
AB7	SDQS3P	I/O	Z	NA	NA	VCC_DRAM
W2	SDQS0N	I/O	Z	NA	NA	VCC_DRAM
Y5	SDQS1N	I/O	Z	NA	NA	VCC_DRAM
W7	SDQS2N	I/O	Z	NA	NA	VCC_DRAM
AA7	SDQS3N	I/O	Z	NA	NA	VCC_DRAM
V16	SACT	O	Z	NA	NA	VCC_DRAM
AA14	SBA0	O	Z	NA	NA	VCC_DRAM
AA13	SBA1	O	Z	NA	NA	VCC_DRAM
AA19	SBG0	O	Z	NA	NA	VCC_DRAM
AB19	SBG1	O	Z	NA	NA	VCC_DRAM
AB11	SCKP	O	Z	NA	NA	VCC_DRAM
AC11	SCKN	O	Z	NA	NA	VCC_DRAM
AB14	SCKE0	O	Z	NA	NA	VCC_DRAM
AC14	SCKE1	O	Z	NA	NA	VCC_DRAM
V13	SCS0	O	Z	NA	NA	VCC_DRAM
AC21	SCS1	O	Z	NA	NA	VCC_DRAM
AA17	SODT0	O	Z	NA	NA	VCC_DRAM
AB20	SODT1	O	Z	NA	NA	VCC_DRAM
Y16	SRST	O	Z	NA	NA	VCC_DRAM
T16	SZQ	AI	Z	NA	NA	VCC_DRAM
R11,R12,R13, T9,T10,T11, T12,T13,T14	VCC_DRAM	P	NA	NA	NA	NA
T15	VDD18_DRAM	P	NA	NA	NA	NA
GPIOA						
D19	PA0	I/O	Z	PU/PD	4	VCC_PA
D18	PA1	I/O	Z	PU/PD	4	VCC_PA
E18	PA2	I/O	Z	PU/PD	4	VCC_PA
D17	PA3	I/O	Z	PU/PD	4	VCC_PA
A18	PA4	I/O	Z	PU/PD	4	VCC_PA
B18	PA5	I/O	Z	PU/PD	4	VCC_PA
D20	PA6	I/O	Z	PU/PD	4	VCC_PA
E20	PA7	I/O	Z	PU/PD	4	VCC_PA
C19	PA8	I/O	Z	PU/PD	4	VCC_PA
C20	PA9	I/O	Z	PU/PD	4	VCC_PA
B19	PA10	I/O	PU	PU/PD	4	VCC_PA
E17	PA11	I/O	PU	PU/PD	4	VCC_PA
F20	PA12	I/O	Z	PU/PD	4	VCC_PA
F17	VCC_PA	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
GPIOC						
G3	PC0	I/O	Z	PU/PD	4	VCC_PC
J5	PC1	I/O	Z	PU/PD	4	VCC_PC
F3	PC2	I/O	Z	PU/PD	4	VCC_PC
F2	PC3	I/O	PU	PU/PD	4	VCC_PC
F1	PC4	I/O	PU	PU/PD	4	VCC_PC
K5	PC5	I/O	PU	PU/PD	4	VCC_PC
K4	PC6	I/O	PU	PU/PD	4	VCC_PC
M6	PC7	I/O	PU	PU/PD	4	VCC_PC
G2	PC8	I/O	Z	PU/PD	4	VCC_PC
H3	PC9	I/O	Z	PU/PD	4	VCC_PC
H1	PC10	I/O	Z	PU/PD	4	VCC_PC
J4	PC11	I/O	Z	PU/PD	4	VCC_PC
J3	PC12	I/O	Z	PU/PD	4	VCC_PC
J2	PC13	I/O	Z	PU/PD	4	VCC_PC
K1	PC14	I/O	Z	PU/PD	4	VCC_PC
K2	PC15	I/O	Z	PU/PD	4	VCC_PC
K3	PC16	I/O	Z	PU/PD	4	VCC_PC
K7	VCC_PC	P	NA	NA	NA	NA
GPIOD						
D22	PD0	I/O	Z	PU/PD	4	VCC_PD
D21	PD1	I/O	Z	PU/PD	4	VCC_PD
C23	PD2	I/O	Z	PU/PD	4	VCC_PD
C22	PD3	I/O	Z	PU/PD	4	VCC_PD
B22	PD4	I/O	Z	PU/PD	4	VCC_PD
C21	PD5	I/O	Z	PU/PD	4	VCC_PD
B21	PD6	I/O	Z	PU/PD	4	VCC_PD
A21	PD7	I/O	Z	PU/PD	4	VCC_PD
B20	PD8	I/O	Z	PU/PD	4	VCC_PD
A20	PD9	I/O	Z	PU/PD	4	VCC_PD
H22	PD10	I/O	Z	PU/PD	4	VCC_PD
H21	PD11	I/O	Z	PU/PD	4	VCC_PD
G23	PD12	I/O	Z	PU/PD	4	VCC_PD
G22	PD13	I/O	Z	PU/PD	4	VCC_PD
G21	PD14	I/O	Z	PU/PD	4	VCC_PD
F22	PD15	I/O	Z	PU/PD	4	VCC_PD
F21	PD16	I/O	Z	PU/PD	4	VCC_PD
E23	PD17	I/O	Z	PU/PD	4	VCC_PD
E22	PD18	I/O	Z	PU/PD	4	VCC_PD
E21	PD19	I/O	Z	PU/PD	4	VCC_PD
K20	PD20	I/O	Z	PU/PD	4	VCC_PD
G19	PD21	I/O	Z	PU/PD	4	VCC_PD
M20	PD22	I/O	Z	PU/PD	4	VCC_PD

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
F19	PD23	I/O	Z	PU/PD	4	VCC_PD
J19	PD24	I/O	Z	PU/PD	4	VCC_PD
K19	PD25	I/O	Z	PU/PD	4	VCC_PD
G20	PD26	I/O	Z	PU/PD	4	VCC_PD
K18	PD27	I/O	Z	PU/PD	4	VCC_PD
J20	PD28	I/O	Z	PU/PD	4	VCC_PD
G18	VCC_PD	P	NA	NA	NA	NA
F18	VCC_LVDS	P	NA	NA	NA	NA
GPIOE						
C3	PE0	I/O	Z	PU/PD	4	VCC_PE
E6	PE1	I/O	Z	PU/PD	4	VCC_PE
D6	PE2	I/O	Z	PU/PD	4	VCC_PE
D5	PE3	I/O	Z	PU/PD	4	VCC_PE
E2	PE4	I/O	Z	PU/PD	4	VCC_PE
E3	PE5	I/O	Z	PU/PD	4	VCC_PE
D2	PE6	I/O	Z	PU/PD	4	VCC_PE
D1	PE7	I/O	Z	PU/PD	4	VCC_PE
D3	PE8	I/O	Z	PU/PD	4	VCC_PE
C1	PE9	I/O	Z	PU/PD	4	VCC_PE
C2	PE10	I/O	Z	PU/PD	4	VCC_PE
B2	PE11	I/O	Z	PU/PD	4	VCC_PE
G6	PE12	I/O	Z	PU/PD	4	VCC_PE
G5	PE13	I/O	Z	PU/PD	4	VCC_PE
G4	PE14	I/O	Z	PU/PD	4	VCC_PE
F4	PE15	I/O	Z	PU/PD	4	VCC_PE
F5	PE16	I/O	Z	PU/PD	4	VCC_PE
E5	PE17	I/O	Z	PU/PD	4	VCC_PE
E4	PE18	I/O	Z	PU/PD	4	VCC_PE
D4	PE19	I/O	Z	PU/PD	4	VCC_PE
A3	PE20	I/O	Z	PU/PD	4	VCC_PE
B3	PE21	I/O	Z	PU/PD	4	VCC_PE
F6	PE22	I/O	Z	PU/PD	4	VCC_PE
J7	VCC_PE	P	NA	NA	NA	NA
GPIOF						
T2	PF0	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
T3	PF1	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
R1	PF2	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
R2	PF3	I/O	PU	PU/PD	4	VCC_IO, or VCC_PLL
R3	PF4	I/O	Z	PU/PD	4	VCC_IO, or VCC_PLL
P3	PF5	I/O	Z	PU/PD	4	VCC_IO, or

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
						VCC_PLL
T4	PF6	I/O	PU	PU/PD	4	VCC_IO, or VCC_PLL
GPIOG						
B10	PG0	I/O	Z	PU/PD	4	VCC_PG
A9	PG1	I/O	PU	PU/PD	4	VCC_PG
B9	PG2	I/O	PU	PU/PD	4	VCC_PG
C9	PG3	I/O	PU	PU/PD	4	VCC_PG
C8	PG4	I/O	PU	PU/PD	4	VCC_PG
B8	PG5	I/O	PU	PU/PD	4	VCC_PG
A7	PG6	I/O	Z	PU/PD	4	VCC_PG
B7	PG7	I/O	Z	PU/PD	4	VCC_PG
A5	PG8	I/O	Z	PU/PD	4	VCC_PG
B6	PG9	I/O	Z	PU/PD	4	VCC_PG
C7	PG10	I/O	Z	PU/PD	4	VCC_PG
D9	PG11	I/O	Z	PU/PD	4	VCC_PG
B5	PG12	I/O	Z	PU/PD	4	VCC_PG
C5	PG13	I/O	Z	PU/PD	4	VCC_PG
C6	PG14	I/O	Z	PU/PD	4	VCC_PG
F9	PG15	I/O	Z	PU/PD	4	VCC_PG
E9	PG16	I/O	Z	PU/PD	4	VCC_PG
B4	PG17	I/O	Z	PU/PD	4	VCC_PG
D7	PG18	I/O	Z	PU/PD	4	VCC_PG
E7	PG19	I/O	Z	PU/PD	4	VCC_PG
F7	VCC_PG	P	NA	NA	NA	NA
GPIOH						
C14	PH0	I/O	Z	PU/PD	4	VCC_IO
C15	PH1	I/O	Z	PU/PD	4	VCC_IO
B12	PH2	I/O	Z	PU/PD	4	VCC_IO
B13	PH3	I/O	Z	PU/PD	4	VCC_IO
C17	PH4	I/O	Z	PU/PD	4	VCC_IO
B14	PH5	I/O	Z	PU/PD	4	VCC_IO
A13	PH6	I/O	Z	PU/PD	4	VCC_IO
E12	PH7	I/O	Z	PU/PD	4	VCC_IO
B11	PH8	I/O	Z	PU/PD	4	VCC_IO
C11	PH9	I/O	Z	PU/PD	4	VCC_IO
A11	PH10	I/O	Z	PU/PD	4	VCC_IO
GPIOI						
N5	PI0	I/O	Z	PU/PD	4	VCC_PI
L3	PI1	I/O	Z	PU/PD	4	VCC_PI
M4	PI2	I/O	Z	PU/PD	4	VCC_PI
M3	PI3	I/O	Z	PU/PD	4	VCC_PI
R6	PI4	I/O	Z	PU/PD	4	VCC_PI

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
L2	PI5	I/O	Z	PU/PD	4	VCC_PI
N4	PI6	I/O	Z	PU/PD	4	VCC_PI
M2	PI7	I/O	Z	PU/PD	4	VCC_PI
N6	PI8	I/O	Z	PU/PD	4	VCC_PI
M1	PI9	I/O	Z	PU/PD	4	VCC_PI
R4	PI10	I/O	Z	PU/PD	4	VCC_PI
N2	PI11	I/O	Z	PU/PD	4	VCC_PI
R5	PI12	I/O	Z	PU/PD	4	VCC_PI
P2	PI13	I/O	Z	PU/PD	4	VCC_PI
R7	PI14	I/O	Z	PU/PD	4	VCC_PI
T5	PI15	I/O	Z	PU/PD	4	VCC_PI
T6	PI16	I/O	Z	PU/PD	4	VCC_PI
M7	VCC_PI	P	NA	NA	NA	NA
GPIOL						
E15	PL0	I/O	Z	PU/PD	4	VCC_RTC
F15	PL1	I/O	Z	PU/PD	4	VCC_RTC
System						
D12	NMI	I	No Pull	PU/PD	NA	VCC_RTC
C12	TEST	I	PD	PU/PD	NA	VCC_RTC
D10	FEL	I	PU	PU/PD	NA	VCC_IO
E10	JTAG_SEL	I	PU	PU/PD	NA	VCC_IO
F10	BOOT_SEL	I	PU	PU/PD	NA	VCC_IO
C13	RESET	I/O	No Pull	PU/PD	NA	VCC_RTC
F12	EXTIRQ	OD	PU	PU/PD	NA	VCC_RTC
GPADC						
AB21	GPADC0	AI	NA	NA	NA	AVCC
Y20	GPADC1	AI	NA	NA	NA	AVCC
V18	GPADC2	AI	NA	NA	NA	AVCC
AA21	GPADC3	AI	NA	NA	NA	AVCC
LRADC						
V19	LRADC	AI	NA	NA	NA	AVCC
USB						
T21	USB0_DM	A I/O	NA	NA	NA	VCC_USB
T22	USB0_DP	A I/O	NA	NA	NA	VCC_USB
R22	USB1_DM	A I/O	NA	NA	NA	VCC_USB
R23	USB1_DP	A I/O	NA	NA	NA	VCC_USB
P21	USB2_DM	A I/O	NA	NA	NA	VCC_USB
P22	USB2_DP	A I/O	NA	NA	NA	VCC_USB
N21	USB3_DM	A I/O	NA	NA	NA	VCC_USB
N22	USB3_DP	A I/O	NA	NA	NA	VCC_USB
N17	VCC_USB	P	NA	NA	NA	NA
M17	VCC_USB2	P	NA	NA	NA	NA
N18	USB_TEST	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
MIPI CSI						
W23	MCSI_CKN	AI	NA	NA	NA	VCC_MCSI
W22	MCSI_CKP	AI	NA	NA	NA	VCC_MCSI
AA23	MCSI_D0N	AI	NA	NA	NA	VCC_MCSI
AA22	MCSI_D0P	AI	NA	NA	NA	VCC_MCSI
Y22	MCSI_D1N	AI	NA	NA	NA	VCC_MCSI
Y21	MCSI_D1P	AI	NA	NA	NA	VCC_MCSI
V22	MCSI_D2N	AI	NA	NA	NA	VCC_MCSI
V21	MCSI_D2P	AI	NA	NA	NA	VCC_MCSI
U22	MCSI_D3N	AI	NA	NA	NA	VCC_MCSI
U21	MCSI_D3P	AI	NA	NA	NA	VCC_MCSI
N19	VCC_MCSI	P	NA	NA	NA	NA
HDMI (Only for T507-H)						
L22	HTX0N	AO	NA	NA	NA	VCC_HDMI
L23	HTX0P	AO	NA	NA	NA	VCC_HDMI
K21	HTX1N	AO	NA	NA	NA	VCC_HDMI
K22	HTX1P	AO	NA	NA	NA	VCC_HDMI
J22	HTX2N	AO	NA	NA	NA	VCC_HDMI
J23	HTX2P	AO	NA	NA	NA	VCC_HDMI
M21	HTXCN	AO	NA	NA	NA	VCC_HDMI
M22	HTXCP	AO	NA	NA	NA	VCC_HDMI
N20	HCEC	I/O	NA	NA	NA	VCC_HDMI
J17	HHPD	I/O	NA	NA	NA	VCC_HDMI
M18	HSCL	O	NA	NA	NA	VCC_HDMI
M19	HSDA	I/O	NA	NA	NA	VCC_HDMI
K17	VCC_HDMI	P	NA	NA	NA	NA
Only for T507						
L22	NC1	NA	NA	NA	NA	NA
L23	NC0	NA	NA	NA	NA	NA
K21	NC3	NA	NA	NA	NA	NA
K22	NC2	NA	NA	NA	NA	NA
J22	NC5	NA	NA	NA	NA	NA
J23	NC4	NA	NA	NA	NA	NA
M21	NC7	NA	NA	NA	NA	NA
M22	NC6	NA	NA	NA	NA	NA
N20	NC10	NA	NA	NA	NA	NA
J17	NC11	NA	NA	NA	NA	NA
M18	NC8	NA	NA	NA	NA	NA
M19	NC9	NA	NA	NA	NA	NA
K17	VCC18	NA	NA	NA	NA	NA
TV OUT						
AB22	TV_OUT	AO	NA	NA	NA	VCC_TV
T17	VCC_TV	P	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
Audio Codec						
T19	VRA1	AO	NA	NA	NA	AVCC
R19	VRA2	AO	NA	NA	NA	AVCC
R18	AVCC	P	NA	NA	NA	NA
T20	LINEOUTL	AO	NA	NA	NA	AVCC
R20	LINEOUTR	AO	NA	NA	NA	AVCC
R17	AGND	G	NA	NA	NA	NA
W20	REXT	AO	NA	NA	NA	AVCC
RTC						
A15	X32KIN	AI	NA	NA	NA	VCC_RTC
B15	X32KOUT	AO	NA	NA	NA	VCC_RTC
G15	RTC_VIO	AO	NA	NA	NA	VCC_RTC
F14	VCC_RTC	P	NA	NA	NA	NA
DCXO						
B16	DXIN	AI	NA	NA	NA	VCC_DCXO
B17	DXOUT	AO	NA	NA	NA	VCC_DCXO
D14	DXLDO_OUT	AO	NA	NA	NA	VCC_DCXO
A17	REFCLK_OUT	AO	NA	NA	NA	VCC_DCXO
D15	WREQIN	I	NA	NA	NA	VCC_PG
E14	VCC_DCXO	P	NA	NA	NA	NA
Power						
G12	VCC_IO	P	NA	NA	NA	NA
K8,L8,L9,M8, M9,N8,N9,P9	VDD_CPU	P	NA	NA	NA	NA
P8	VDD_CPUFB	P	NA	NA	NA	NA
H10,H11,H12, H13,J10,J11, J12,J13	VDD_GPU	P	NA	NA	NA	NA
H9	VDD_GPUFB	P	NA	NA	NA	NA
J15,K15,L15, L16,M15,M16, K16	VDD_SYS	P	NA	NA	NA	NA
J16	VDD_SYSFB	P	NA	NA	NA	NA
G14	VCC_PLL	P	NA	NA	NA	NA
Ground						
A1,A2,A22,A23 ,AA12,AA6,AB1 ,AB10,AB15, AB18,AB23, AC1,AC2,AC22, AC23,B1,B23, C10,C16,C18, C4,E19,G10, G17,G7,H14, H15,H16,H2, H8,J14,J21,J8, J9,K10,K11,K12	GND	G	NA	NA	NA	NA

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6] (mA)	Power Supply[7]
,K13,K14,K6,K9 ,L10,L11,L12, L13,L14,L21, M10,M11,M12 ,M13,M14,M5, N10,N11,N12, N13,N14,N15, N16,N23,N3, P10,P11,P12, P13,P14,P15, P16,R10,R14, R15,R16,R21, R8,R9,T8,U10, U12,U15,U17, U23,U3,U7, W13,W16,W21 ,W3,Y10,Y19, Y7						
NC						
W18,Y18,W19, V20						

4.3. GPIO Multiplex Function

The following table provides a description of the T507/T507-H GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function.

Table 4-3. GPIO Multiplex Function

Pin Name	GPIO Group	IO Type	Function2	Function3	Function4	Function5	Function6
PA0	GPIOA	I/O	RMII_RXD1		TWI0_SCK		PA_EINT0
PA1		I/O	RMII_RXD0		TWI0_SDA		PA_EINT1
PA2		I/O	RMII_CRS_DV		TWI1_SCK		PA_EINT2
PA3		I/O	RMII_RXER		TWI1_SDA		PA_EINT3
PA4		I/O	RMII_TXD1	STANDBY_STATE			PA_EINT4
PA5		I/O	RMII_TXD0	H_I2S0_DOUT0			PA_EINT5
PA6		I/O	RMII_TXCK	H_I2S0_MCLK			PA_EINT6
PA7		I/O	RMII_TXEN	H_I2S0_BCLK			PA_EINT7
PA8		I/O	MDC	H_I2S0_LRCK			PA_EINT8
PA9		I/O	MDIO	H_I2S0_DIN0			PA_EINT9
PA10		I/O	TWI3_SCK				PA_EINT10
PA11		I/O	TWI3_SDA				PA_EINT11
PA12		I/O	PWM5		WATCHDOG_SIG		PA_EINT12
PC0	GPIOC	I/O	NAND_WE	SDC2_DS	SPI0_CLK		PC_EINT0
PC1		I/O	NAND_ALE	SDC2_RST			PC_EINT1
PC2		I/O	NAND_CLE		SPI0_MOSI		PC_EINT2
PC3		I/O	NAND_CE1		SPI0_CS0	BOOT_SEL1	PC_EINT3
PC4		I/O	NAND_CE0		SPI0_MISO	BOOT_SEL2	PC_EINT4
PC5		I/O	NAND_RE	SDC2_CLK		BOOT_SEL3	PC_EINT5

PC6		I/O	NAND_RB0	SDC2_CMD		BOOT_SEL4	PC_EINT6
PC7		I/O	NAND_RB1		SPI0_CS1		PC_EINT7
PC8		I/O	NAND_DQ7	SDC2_D3			PC_EINT8
PC9		I/O	NAND_DQ6	SDC2_D4			PC_EINT9
PC10		I/O	NAND_DQ5	SDC2_D0			PC_EINT10
PC11		I/O	NAND_DQ4	SDC2_D5			PC_EINT11
PC12		I/O	NAND_DQS				PC_EINT12
PC13		I/O	NAND_DQ3	SDC2_D1			PC_EINT13
PC14		I/O	NAND_DQ2	SDC2_D6			PC_EINT14
PC15		I/O	NAND_DQ1	SDC2_D2	SPI0_WP		PC_EINT15
PC16		I/O	NAND_DQ0	SDC2_D7	SPI0_HOLD		PC_EINT16
PD0	GPIOD	I/O	LCD_D0	LVDS0_V0P	TS0_CLK		PD_EINT0
PD1		I/O	LCD_D1	LVDS0_V0N	TS0_ERR		PD_EINT1
PD2		I/O	LCD_D2	LVDS0_V1P	TS0_SYNC		PD_EINT2
PD3		I/O	LCD_D3	LVDS0_V1N	TS0_DVLD		PD_EINT3
PD4		I/O	LCD_D4	LVDS0_V2P	TS0_D0		PD_EINT4
PD5		I/O	LCD_D5	LVDS0_V2N	TS0_D1		PD_EINT5
PD6		I/O	LCD_D6	LVDS0_CKP	TS0_D2		PD_EINT6
PD7		I/O	LCD_D7	LVDS0_CKN	TS0_D3		PD_EINT7
PD8		I/O	LCD_D8	LVDS0_V3P	TS0_D4		PD_EINT8
PD9		I/O	LCD_D9	LVDS0_V3N	TS0_D5		PD_EINT9
PD10		I/O	LCD_D10	LVDS1_V0P	TS0_D6		PD_EINT10
PD11		I/O	LCD_D11	LVDS1_V0N	TS0_D7		PD_EINT11
PD12		I/O	LCD_D12	LVDS1_V1P	SIM0_VPPEN		PD_EINT12
PD13		I/O	LCD_D13	LVDS1_V1N	SIM0_VPPPP		PD_EINT13
PD14		I/O	LCD_D14	LVDS1_V2P	SIM0_PWREN		PD_EINT14
PD15		I/O	LCD_D15	LVDS1_V2N	SIM0_CLK		PD_EINT15
PD16		I/O	LCD_D16	LVDS1_CKP	SIM0_DATA		PD_EINT16
PD17		I/O	LCD_D17	LVDS1_CKN	SIM0_RST		PD_EINT17
PD18		I/O	LCD_D18	LVDS1_V3P	SIM0_DET		PD_EINT18
PD19		I/O	LCD_D19	LVDS1_V3N			PD_EINT19
PD20		I/O	LCD_D20				PD_EINT20
PD21		I/O	LCD_D21				PD_EINT21
PD22		I/O	LCD_D22				PD_EINT22
PD23		I/O	LCD_D23				PD_EINT23
PD24		I/O	LCD_CLK				PD_EINT24
PD25		I/O	LCD_DE				PD_EINT25
PD26		I/O	LCD_HSYNC				PD_EINT26
PD27		I/O	LCD_VSYNC				PD_EINT27
PD28		I/O	PWM0				PD_EINT28
PE0	GPIOE	I/O	NCSI_PCLK				PE_EINT0
PE1		I/O	NCSI_MCLK				PE_EINT1
PE2		I/O	NCSI_HSYNC				PE_EINT2
PE3		I/O	NCSI_VSYNC				PE_EINT3
PE4		I/O	NCSI_D0				PE_EINT4
PE5		I/O	NCSI_D1				PE_EINT5
PE6		I/O	NCSI_D2				PE_EINT6
PE7		I/O	NCSI_D3				PE_EINT7
PE8		I/O	NCSI_D4				PE_EINT8
PE9		I/O	NCSI_D5				PE_EINT9
PE10		I/O	NCSI_D6				PE_EINT10
PE11		I/O	NCSI_D7				PE_EINT11
PE12		I/O	NCSI_D8				PE_EINT12
PE13		I/O	NCSI_D9				PE_EINT13
PE14		I/O	NCSI_D10				PE_EINT14

PE15		I/O	NCSI_D11				PE_EINT15
PE16		I/O	NCSI_D12				PE_EINT16
PE17		I/O	NCSI_D13				PE_EINT17
PE18		I/O	NCSI_D14				PE_EINT18
PE19		I/O	NCSI_D15				PE_EINT19
PE20		I/O	NCSI_SCK			TWI2_SCK	PE_EINT20
PE21		I/O	NCSI_SDA			TWI2_SDA	PE_EINT21
PE22		I/O	CSI_FSIN0		TCON_TRIG0		PE_EINT22
PF0	GPIOF	I/O	SDC0_D1	JTAG_MS			PF_EINT0
PF1		I/O	SDC0_D0	JTAG_DI			PF_EINT1
PF2		I/O	SDC0_CLK	UART0_TX			PF_EINT2
PF3		I/O	SDC0_CMD	JTAG_DO			PF_EINT3
PF4		I/O	SDC0_D3	UART0_RX			PF_EINT4
PF5		I/O	SDC0_D2	JTAG_CK			PF_EINT5
PF6		I/O					PF_EINT6
PG0	GPIOG	I/O	SDC1_CLK				PG_EINT0
PG1		I/O	SDC1_CMD				PG_EINT1
PG2		I/O	SDC1_D0				PG_EINT2
PG3		I/O	SDC1_D1				PG_EINT3
PG4		I/O	SDC1_D2				PG_EINT4
PG5		I/O	SDC1_D3				PG_EINT5
PG6		I/O	UART1_TX		JTAG_MS		PG_EINT6
PG7		I/O	UART1_RX		JTAG_CK		PG_EINT7
PG8		I/O	UART1_RTS	PLL_LOCK_DBG	JTAG_DO		PG_EINT8
PG9		I/O	UART1_CTS		JTAG_DI		PG_EINT9
PG10		I/O	H_I2S2_MCLK	X32KFOUT			PG_EINT10
PG11		I/O	H_I2S2_BCLK		BIST_RESULT0		PG_EINT11
PG12		I/O	H_I2S2_LRCK		BIST_RESULT1		PG_EINT12
PG13		I/O	H_I2S2_DOUT0	H_I2S2_DIN1	BIST_RESULT2		PG_EINT13
PG14		I/O	H_I2S2_DIN0	H_I2S2_DOUT1	BIST_RESULT3		PG_EINT14
PG15		I/O	UART2_TX			TWI4_SCK	PG_EINT15
PG16		I/O	UART2_RX			TWI4_SDA	PG_EINT16
PG17		I/O	UART2_RTS	MCSI_SCK		TWI3_SCK	PG_EINT17
PG18		I/O	UART2_CTS	MCSI_SDA		TWI3_SDA	PG_EINT18
PG19		I/O		MCSI_MCLK	PWM1		PG_EINT19
PH0	GPIOH	I/O	UART0_TX		PWM3	TWI1_SCK	PH_EINT0
PH1		I/O	UART0_RX		PWM4	TWI1_SDA	PH_EINT1
PH2		I/O	UART5_TX	OWA_MCLK	PWM2	TWI2_SCK	PH_EINT2
PH3		I/O	UART5_RX		PWM1	TWI2_SDA	PH_EINT3
PH4		I/O		OWA_OUT		TWI3_SCK	PH_EINT4
PH5		I/O	UART2_TX	H_I2S3_MCLK	SPI1_CS0	TWI3_SDA	PH_EINT5
PH6		I/O	UART2_RX	H_I2S3_BCLK	SPI1_CLK	TWI4_SCK	PH_EINT6
PH7		I/O	UART2_RTS	H_I2S3_LRCK	SPI1_MOSI	TWI4_SDA	PH_EINT7
PH8		I/O	UART2_CTS	H_I2S3_DOUT0	SPI1_MISO	H_I2S3_DIN1	PH_EINT8
PH9		I/O		H_I2S3_DIN0	SPI1_CS1	H_I2S3_DOUT1	PH_EINT9
PH10		I/O		IR_RX	TCON_TRIG1		PH_EINT10
PI0	GPIOI	I/O	RGMII_RXD3/ RMII_NULL	DMIC_CLK	H_I2S0_MCLK	HDMI_SCL (Only for T507-H)	PI_EINT0
PI1		I/O	RGMII_RXD2/ RMII_NULL	DMIC_DATA0	H_I2S0_BCLK	HDMI_SDA (Only for T507-H)	PI_EINT1
PI2		I/O	RGMII_RXD1/ RMII_RXD1	DMIC_DATA1	H_I2S0_LRCK	HDMI_CEC (Only for T507-H)	PI_EINT2
PI3		I/O	RGMII_RXD0/	DMIC_DATA2	H_I2S0_DOUT0	H_I2S0_DIN1	PI_EINT3

			RMII_RXD0				
PI4		I/O	RGMII_RXCK/ RMII_NULL	DMIC_DATA3	H_I2S0_DIN0	H_I2S0_DOUT1	PI_EINT4
PI5		I/O	RGMII_RXCTL/ RMII_CRS_DV	UART2_TX	TS0_CLK	TWI0_SCK	PI_EINT5
PI6		I/O	RGMII_NULL/ RMII_RXER	UART2_RX	TS0_ERR	TWI0_SDA	PI_EINT6
PI7		I/O	RGMII_TXD3/ RMII_NULL	UART2_RTS	TS0_SYNC	TWI1_SCK	PI_EINT7
PI8		I/O	RGMII_TXD2/ RMII_NULL	UART2_CTS	TS0_DVLD	TWI1_SDA	PI_EINT8
PI9		I/O	RGMII_TXD1/ RMII_TXD1	UART3_TX	TS0_D0	TWI2_SCK	PI_EINT9
PI10		I/O	RGMII_TXD0/ RMII_TXD0	UART3_RX	TS0_D1	TWI2_SDA	PI_EINT10
PI11		I/O	RGMII_TXCK/ RMII_TXCK	UART3_RTS	TS0_D2	PWM1	PI_EINT11
PI12		I/O	RGMII_TXCTL/ RMII_TXEN	UART3_CTS	TS0_D3	PWM2	PI_EINT12
PI13		I/O	RGMII_CLKIN/ RMII_NULL	UART4_TX	TS0_D4	PWM3	PI_EINT13
PI14		I/O	MDC	UART4_RX	TS0_D5	PWM4	PI_EINT14
PI15		I/O	MDIO	UART4_RTS	TS0_D6	CLK_FANOUT0	PI_EINT15
PI16		I/O	EPHY_25M	UART4_CTS	TS0_D7	CLK_FANOUT1	PI_EINT16
PL0	GPIOL	I/O		S_TWI0_SCK			
PL1		I/O		S_TWI0_SDA			

4.4. Detailed Signal Description

Table 4-4 shows the detailed function description of every signal based on the different interface.

[1].Signal Name: The name of every signal.

[2].Description: The detailed function description of every signal.

[3].Type: Denotes the signal direction:

I (Input),
O (Output),
I/O(Input/Output),
OD(Open-Drain),
A (Analog),
AI(Analog Input),
AO(Analog Output),
A I/O(Analog Input/Output),
P (Power),
G (Ground)

Table 4-4. Detailed Signal Description

Signal Name[1]	Description[2]	Type[3]
DRAM		
SDQ[31:0]	DRAM Bidirectional Data Line to the Memory Device	I/O
SDQS[3:0]P	DRAM Active-High Bidirectional Data Strobes to the Memory Device	I/O
SDQS[3:0]N	DRAM Active-Low Bidirectional Data Strobes to the Memory Device	I/O
SDQM[3:0]	DRAM Data Mask Signal to the Memory Device	O
SCKP	DRAM Active-High Clock Signal to the Memory Device	O

Signal Name[1]	Description[2]	Type[3]
SCKN	DRAM Active-Low Clock Signal to the Memory Device	O
SCKE[1:0]	DRAM Clock Enable Signal to the Memory Device	O
SA[16:0]	DRAM Address Signal to the Memory Device	O
SBA[1:0]	DRAM Bank Address Signal to the Memory Device	O
SBG[1:0]	DRAM Bank Group Address Signal to the Memory Device	O
SACT	DRAM Activation Command Output	O
SCS[1:0]	DRAM Chip Select Signal to the Memory Device	O
SODT[1:0]	DRAM On-Die Termination Output Signal	O
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
SRST	DRAM Reset Signal to the Memory Device	O
VCC_DRAM	DRAM Power Supply	P
VDD18_DRAM	SDRAM Controller Power Supply	P
System Control		
NMI	Non-maskable Interrupt	I
TEST	Test Signal	I
FEL	Boot Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process. For more details, see section 3.4 “BROM System” in the ***Allwinner T507&T507-H User Manual***.	I
BOOT_SEL[4:1]	Boot Media Select[4:1]	I
BOOT_SEL	Boot Media Select0	I
JTAG_SEL	JTAG Mode Select The signal is used to select the port from which JTAG function outputs.	I
RESET	Reset Signal(low active)	I/O
EXTIRQ	External IRQ	OD
DCXO		
DXLDO_OUT	Internal Supply Regulator Output	AO
REFCLK_OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
WREQIN	Request Signal of REFCLK(24MHz Fanout)	I
VCC_DCXO	Digital Compensated Crystal Oscillator Power Supply	P
RTC		
X32KIN	Clock Input of 32.768kHz Crystal	AI
X32KOUT	Clock Output of 32.768kHz Crystal	AO
X32KFOUT	32.768kHz Clock Fanout Provides low frequency clock for external devices	OD
RTC_VIO	RTC Low Voltage (generated via internal LDO)	AO
VCC_RTC	RTC Power	P
USB		
USB0_DM	USB0 Data Signal DM	A I/O
USB0_DP	USB0 Data Signal DP	A I/O
USB1_DM	USB1 Data Signal DM	A I/O

Signal Name[1]	Description[2]	Type[3]
USB1_DP	USB1 Data Signal DP	A I/O
USB2_DM	USB2 Data Signal DM	A I/O
USB2_DP	USB2 Data Signal DP	A I/O
USB3_DM	USB3 Data Signal DM	A I/O
USB3_DP	USB3 Data Signal DP	A I/O
VCC_USB, VCC_USB2	USB Analog Power Supply	P
USB_TEST	Only for USB2 Debug	P
GPADC		
GPADC0	General Purpose ADC Input Channel0	AI
GPADC1	General Purpose ADC Input Channel1	AI
GPADC2	General Purpose ADC Input Channel2	AI
GPADC3	General Purpose ADC Input Channel3	AI
LRADC		
LRADC	Low Rate ADC Input Channel	AI
AUDIO CODEC		
LINEOUTL	Stereo Lineout Output Left Channel	AO
LINEOUTR	Stereo Lineout Output Right Channel	AO
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
REXT	External Reference Pin	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G
HDMI (Only for T507-H)		
HTX0N	HDMI Negative TMDS Differential Line Driver Data0 Output	AO
HTX0P	HDMI Positive TMDS Differential Line Driver Data0 Output	AO
HTX1N	HDMI Negative TMDS Differential Line Driver Data1 Output	AO
HTX1P	HDMI Positive TMDS Differential Line Driver Data1 Output	AO
HTX2N	HDMI Negative TMDS Differential Line Driver Data2 Output	AO
HTX2P	HDMI Positive TMDS Differential Line Driver Data2 Output	AO
HTXCN	HDMI Negative TMDS Differential Line Driver Clock Output	AO
HTXCP	HDMI Positive TMDS Differential Line Driver Clock Output	AO
HCEC	HDMI Consumer Electronics Control	I/O
HHPD	HDMI Hot Plug Detection Signal	I/O
HSCL	HDMI Serial Clock	O
HSDA	HDMI Serial Data	I/O
VCC_HDMI	HDMI Power Supply	P
MIPI CSI		
MCSI_D0N	MIPI CSI Controller Data0 Negative Signal	AI
MCSI_D0P	MIPI CSI Controller Data0 Positive Signal	AI
MCSI_D1N	MIPI CSI Controller Data1 Negative Signal	AI
MCSI_D1P	MIPI CSI Controller Data1 Positive Signal	AI
MCSI_D2N	MIPI CSI Controller Data2 Negative Signal	AI
MCSI_D2P	MIPI CSI Controller Data2 Positive Signal	AI
MCSI_D3N	MIPI CSI Controller Data3 Negative Signal	AI

Signal Name[1]	Description[2]	Type[3]
MCSI_D3P	MIPI CSI Controller Data3 Positive Signal	AI
MCSI_CKN	MIPI CSI Controller Clock Negative Signal	AI
MCSI_CKP	MIPI CSI Controller Clock Positive Signal	AI
CSI_FSIN0	Frame SYNC Signal	I/O
MCSI_SCK	CCI Control Clock	O
MCSI_SDA	CCIC Control Data	I/O
MCSI_MCLK	Master Clock for MIPI Sensor	O
VCC_MCSI	MIPI CSI Controller Power Supply	P
TVOUT		
TV_OUT	TV-out Output	AO
VCC_TV	TV-out Power Supply	P
LCD		
LCD[23:0]	LCD Data Bit	O
LCD_CLK	LCD Clock Signal	O
LCD_DE	LCD Data Enable	O
LCD_HSYNC	LCD Horizontal Sync	O
LCD_VSYNC	LCD Vertical Sync	O
TCON_TRIG0	LCD Sync0(TCON outputs to LCD for sync)	O
TCON_TRIG1	LCD Sync1(TCON outputs to LCD for sync)	O
LVDS		
LVDS0_V[3:0]P	LVDS0 Data Positive Signal Output	O
LVDS0_V[3:0]N	LVDS0 Data Negative Signal Output	O
LVDS0_VPC	LVDS0 Clock Positive Signal Output	O
LVDS0_VNC	LVDS0 Clock Negative Signal Output	O
LVDS1_V[3:0]P	LVDS1 Data Positive Signal Output	O
LVDS1_V[3:0]N	LVDS1 Data Negative Signal Output	O
LVDS1_VPC	LVDS1 Clock Positive Signal Output	O
LVDS1_VNC	LVDS1 Clock Negative Signal Output	O
Parallel CSI		
NCSI_PCLK	CSI Pixel Clock	I
NCSI_MCLK	CSI Master Clock	O
NCSI_HSYNC	CSI Horizontal Sync	I
NCSI_VSYNC	CSI Vertical Sync	I
NCSI_D[15:0]	CSI Data Bit	I
NCSI_SCK	CCI Control Clock	O,OD
NCSI_SDA	CCI Control Data	I/O,OD
NAND Flash		
NAND_WE	Nand Flash Write Enable	O
NAND_ALE	Nand Flash Address Latch Enable	O
NAND_CLE	Nand Flash Command Latch Enable	O
NAND_CE[1:0]	Nand Flash Chip Select	O
NAND_RE	Nand Flash Read Enable	O
NAND_RB[1:0]	Nand Flash Ready/Busy Status Indicator Signal	I
NAND_DQ[7:0]	Nand Flash Data Bit	I/O

Signal Name[1]	Description[2]	Type[3]
NAND_DQS	Nand Flash Data Strobe	I/O
SMHC		
SDC0_D[3:0]	SDC0 Data Bit	I/O
SDC0_CLK	SDC0 Clock	O
SDC0_CMD	SDC0 Command Signal	I/O,OD
SDC1_D[3:0]	SDC1 Data Bit	I/O
SDC1_CLK	SDC1 Clock	O
SDC1_CMD	SDC1 Command Signal	I/O,OD
SDC2_D[7:0]	SDC2 Data Bit	I/O
SDC2_CLK	SDC2 Clock	O
SDC2_CMD	SDC2 Command Signal	I/O,OD
SDC2_DS	SDC2 Data Strobe	I
SDC2_RST	SDC2 Reset	O
I2S/PCM		
H_I2S0_MCLK	I2S0 Master Clock	O
H_I2S0_LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
H_I2S0_BCLK	I2S0/PCM0 Sample Rate Clock	I/O
H_I2S0_DOUT[1:0]	I2S0/PCM0 Serial Data Output Channel [1:0]	O
H_I2S0_DIN[1:0]	I2S0/PCM0 Serial Data Input Channel [1:0]	I
H_I2S2_MCLK	I2S2 Master Clock	O
H_I2S2_LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
H_I2S2_BCLK	I2S2/PCM2 Sample Rate Clock	I/O
H_I2S2_DOUT[1:0]	I2S2/PCM2 Serial Data Output Channel [1:0]	O
H_I2S2_DIN[1:0]	I2S2/PCM2 Serial Data Input Channel [1:0]	I
H_I2S3_MCLK	I2S3 Master Clock	O
H_I2S3_LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
H_I2S3_BCLK	I2S3/PCM3 Sample Rate Clock	I/O
H_I2S3_DOUT[1:0]	I2S3/PCM3 Serial Data Output Channel [1:0]	O
H_I2S3_DIN[1:0]	I2S3/PCM3 Serial Data Input Channel [1:0]	I
DMIC		
DMIC_CLK	Digital Microphone Clock Output	O
DMIC_DATA[3:0]	Digital Microphone Data Input	I
OWA		
OWA_OUT	One Wire Audio Output	O
OWA_MCLK	One Wire Audio Master Clock	O
Interrupt		
PA_EINT[12:0]	GPIO A Interrupt	I
PC_EINT[16:0]	GPIO C Interrupt	I
PD_EINT[28:0]	GPIO D Interrupt	I
PE_EINT[22:0]	GPIO E Interrupt	I
PF_EINT[6:0]	GPIO F Interrupt	I
PG_EINT[19:0]	GPIO G Interrupt	I
PH_EINT[10:0]	GPIO H Interrupt	I
PI_EINT[16:0]	GPIO I Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PWM		
PWM[5:0]	Pulse Width Modulation Output Channel [5:0]	I/O
CIR Receiver		
IR_RX	Consumer Infrared Receiver	I
EMAC		
RGMII_RXD3/RMII_NULL	RGMII Receive Data3	I
RGMII_RXD2/RMII_NULL	RGMII Receive Data2	I
RGMII_RXD1/RMII_RXD1	RGMII/RMII Receive Data1	I
RGMII_RXD0/RMII_RXD0	RGMII/RMII Receive Data0	I
RGMII_RXCK/RMII_NULL	RGMII Receive Clock	I
RGMII_RXCTL/RMII_CRS_DV	RGMII Receive Control/RMII Carrier Sense Receive Data Valid	I
RGMII_NULL/RMII_RXER	RMII Receive Error	I
RGMII_TXD3/RMII_NULL	RGMII Transmit Data3	O
RGMII_TXD2/RMII_NULL	RGMII Transmit Data2	O
RGMII_TXD1/RMII_TXD1	RGMII/RMII Transmit Data1	O
RGMII_TXD0/RMII_TXD0	RGMII/RMII Transmit Data0	O
RGMII_TXCK/RMII_TXCK	RGMII/RMII Transmit Clock For RGMII, IO type is output; For RMII, IO type is input	I/O
RGMII_TXCTL/RMII_TXEN	RGMII Transmit Control/RMII Transmit Enable	O
RGMII_CLKIN/RMII_NULL	RGMII Transmit Clock from External	I
MDC	RGMII/RMII Management Data Clock	O
MDIO	RGMII/RMII Management Data Input/Output	I/O
EPHY_25M	25MHz Output for EPHY	O
TSC		
TS0_CLK	Transport Stream Clock	I
TS0_ERR	Transport Stream Error Indicate	I
TS0_SYNC	Transport Stream Sync	I
TS0_DVLD	Transport Stream Data Valid	I
TS0_D[7:0]	Transport Stream Data	I
Smart Card		
SIM_PWREN	Smart Card Power Enable	O
SIM_VPPEN	Smart Card Program Voltage Enable	O
SIM_VPPPP	Smart Card Program Control	O
SIM_CLK	Smart Card Clock	O
SIM_DATA	Smart Card Data	I/O
SIM_RST	Smart Card Reset	O
SIM_DET	Smart Card Detect	I
SPI		
SPI0_CS0	SPI0 Chip Select0 Signal, Low Active	I/O
SPI0_CS1	SPI0 Chip Select1 Signal, Low Active	I/O
SPI0_CLK	SPI0 Clock Signal	I/O
SPI0_MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0_MISO	SPI0 Master Data In, Slave Data Out	I/O

Signal Name[1]	Description[2]	Type[3]
SPI0_WP	SPI0 Write Protect, Low Active	I/O
SPI0_HOLD	SPI0 Hold Signal	I/O
SPI1_CS0	SPI1 Chip Select0 Signal, Low Active	I/O
SPI1_CS1	SPI1 Chip Select1 Signal, Low Active	I/O
SPI1_CLK	SPI1 Clock Signal	I/O
SPI1_MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1_MISO	SPI1 Master Data In, Slave Data Out	I/O
UART		
UART0_TX	UART0 Data Transmit	O
UART0_RX	UART0 Data Receive	I
UART1_TX	UART1 Data Transmit	O
UART1_RX	UART1 Data Receive	I
UART1_CTS	UART1 Data Clear to Send	I
UART1_RTS	UART1 Data Request to Send	O
UART2_TX	UART2 Data Transmit	O
UART2_RX	UART2 Data Receive	I
UART2_CTS	UART2 Data Clear to Send	I
UART2_RTS	UART2 Data Request to Send	O
UART3_TX	UART3 Data Transmit	O
UART3_RX	UART3 Data Receive	I
UART3_CTS	UART3 Data Clear to Send	I
UART3_RTS	UART3 Data Request to Send	O
UART4_TX	UART4 Data Transmit	O
UART4_RX	UART4 Data Receive	I
UART4_CTS	UART4 Data Clear to Send	I
UART4_RTS	UART4 Data Request to Send	O
UART5_TX	UART5 Data Transmit	O
UART5_RX	UART5 Data Receive	I
TWI		
TWI0_SCK	TWI0 Serial Clock Signal	I/O
TWI0_SDA	TWI0 Serial Data Signal	I/O
TWI1_SCK	TWI1 Serial Clock Signal	I/O
TWI1_SDA	TWI1 Serial Data Signal	I/O
TWI2_SCK	TWI2 Serial Clock Signal	I/O
TWI2_SDA	TWI2 Serial Data Signal	I/O
TWI3_SCK	TWI3 Serial Clock Signal	I/O
TWI3_SDA	TWI3 Serial Data Signal	I/O
TWI4_SCK	TWI4 Serial Clock Signal	I/O
TWI4_SDA	TWI4 Serial Data Signal	I/O
S_TWI0_SCK	S_TWI0 Serial Clock Signal	I/O
S_TWI0_SDA	S_TWI0 Serial Data Signal	I/O
JTAG		
JTAG_MS	JTAG Mode Select	I
JTAG_CK	JTAG Clock Signal	I

Signal Name[1]	Description[2]	Type[3]
JTAG_DO	JTAG Data Output	O
JTAG_DI	JTAG Data Input	I

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 5-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 5.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
AVCC	Analog Part Power		-0.3	2.16	V
VCC_PA	Digital GPIO A Power		-0.3	3.96	V
VCC_PC	Digital GPIO C Power		-0.3	3.96	V
VCC_PD	Digital GPIO D Power		-0.3	3.96	V
VCC_PE	Digital GPIO E Power		-0.3	3.96	V
VCC_PG	Digital GPIO G Power		-0.3	3.96	V
VCC_PI	Digital GPIO I Power		-0.3	3.96	V
VCC_IO	GPIO F, GPIO H and System Control Power		-0.3	3.96	V
VCC_LVDS	LVDS Power		-0.3	2.16	V
VCC_USB,VCC_USB2	USB Analog Power		-0.3	3.96	V
VCC_MCSI	MIPI CSI Power		-0.3	2.16	V
VCC_HDMI	HDMI Power (Only for T507-H)		-0.3	2.16	V
VCC_TV	TV OUT Power		-0.3	2.16	V
VCC_DCXO	DCXO Power		-0.3	2.16	V
VDD_CPU	CPU Power		-0.3	1.3	V
VDD_GPU	GPU Power		-0.3	1.1	V
VCC_PLL	System PLL Power		-0.3	2.16	V
VCC_RTC	RTC Power		-0.3	2.16	V
VCC_DRAM	DRAM Power		-0.3	2.16	V
VDD18_DRAM	DRAM 1.8V Internal PAD Power		-0.3	2.16	V
VDD_SYS	Power Supply for System		-0.3	1.1	V
T_{STG}	Storage Temperature		-40	150	°C
Tj	Working Junction Temperature		-40	125	°C
V_{ESD}	ESD Stress Voltage(1)	Human Body Model(HBM)(2)	-2000	2000	V
		Charged Device Model(CDM)(3)	-500	500	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(4)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(5)		Pass		

(1). Electrostatic discharge(ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.

(2). Level listed above is the passing level per ESDA/JEDEC JS-001-2017.
(3). Level listed above is the passing level per ESDA/JEDEC JS-002-2018.
(4). Based on JESD78E; each device is tested with IO pin injection of ±200mA at room temperature.
(5). Based on JESD78E; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.2. Recommended Operating Conditions

All T507/T507-H modules are used under the operating conditions contained in Table 5-2.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-40	-	85	°C
Tj	Working Junction Temperature Range	-40	-	120(1)	°C
AVCC	Analog Part Power	1.764	1.8	1.836	V
VCC_PA	Digital GPIO A Power	2.97	3.3	3.63	V
VCC_PC	Digital GPIO C Power 1.8 V Voltage 3.3 V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PD	Digital GPIO D Power 1.8 V Voltage 2.5 V Voltage 3.3 V Voltage	 1.62 2.25 2.97	 1.8 2.5 3.3	 1.98 2.75 3.63	V
VCC_PE	Digital GPIO E Power 1.8 V Voltage 2.8 V Voltage 3.3 V Voltage	 1.62 2.52 2.97	 1.8 2.8 3.3	 1.98 3.08 3.63	V
VCC_PG	Digital GPIO G Power 1.8 V Voltage 3.3 V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC_PI	Digital GPIO I Power 1.8 V Voltage 2.8 V Voltage 3.3 V Voltage	 1.62 2.52 2.97	 1.8 2.8 3.3	 1.98 3.08 3.63	V
VCC_IO	GPIO F, GPIO H and System Control Power	2.97	3.3	3.63	V
VCC_LVDS	LVDS Power	1.62	1.8	1.98	V
VCC_USB, VCC_USB2	USB Analog Power	2.97	3.3	3.63	V
VCC_MCSI	MIPI CSI Power	1.62	1.8	1.98	V
VCC_HDMI	HDMI Power (Only for T507-H)	1.62	1.8	1.98	V
VCC_TV	TV OUT Power	1.78	1.8	1.98	V
VCC_DCXO	DCXO Power	1.62	1.8	1.98	V
VDD_CPU	CPU Power	0.81	-	1.1	V
VDD_GPU	GPU Power	0.81	-	0.99	V
VCC_PLL	System PLL Power	1.62	1.8	1.98	V
VCC_RTC	RTC Power	1.62	1.8	1.98	V
VCC_DRAM	DRAM Power DDR4 IO Domain Power	 1.14	 1.2	 1.26	V

	LPDDR4 IO Domain Power LPDDR3 IO Domain Power DDR3 IO Domain Power DDR3L IO Domain Power	1.06 1.14 1.425 1.425	1.1 1.2 1.5 1.5	1.17 1.3 1.575 1.575	
VDD18_DRAM	DRAM 1.8 V Internal PAD Power	1.7	1.8	1.98	V
VDD_SYS	Power Supply for System	0.81	-	0.99	V

(1). The chip junction temperature in normal working condition should be less than or equal to the maximum junction temperature in Table 5-2.

5.3. Power Consumption Parameters

If you have questions about power consumption parameters, contact Allwinner FAE.

5.4. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of the T507/T507-H.

Table 5-3. DC Electrical Characteristics
(VCC_IO/VCC_PA/VCC_PC/VCC_PD/VCC_PE/VCC_PG/VCC_PI)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input Pull-up Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
R_{PD}	Input Pull-down Resistance	80 3.76 12	100 4.7 15	120 5.64 18	kΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO – 0.3	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

NOTE

For PA10, PA11, PL0, and PL1 ports, the R_{PU} and R_{PD} are 4.7kΩ ±20%.
For PC0, PC3~PC7, PF3, PF6, and PG1~PG5 ports, the R_{PU} and R_{PD} are 15kΩ ±20%.
For other GPIO ports, the R_{PU} and R_{PD} are 100kΩ ±20%.

5.5. SDIO Electrical Characteristics

The SDIO electrical parameters are related to different supply voltage.

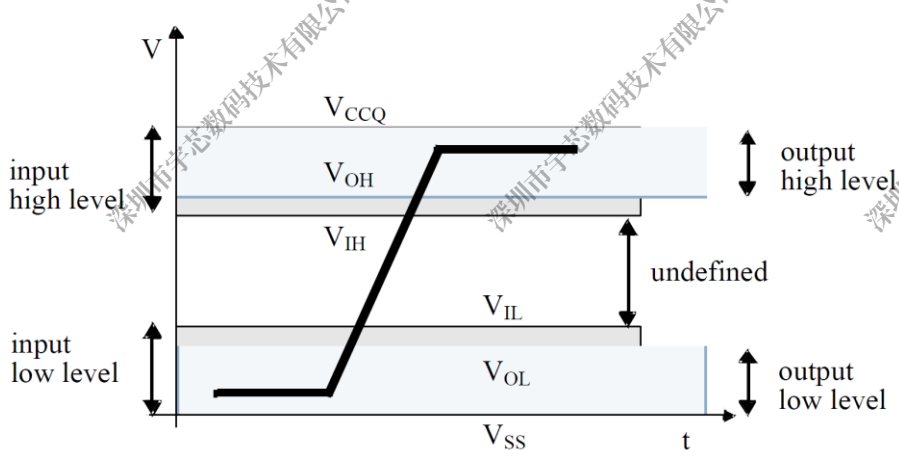


Figure 5-1. SDIO Voltage Waveform

Table 5-4 shows 3.3V SDIO electrical parameters.

Table 5-4. 3.3V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7	-	3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125* V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625* V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8V SDIO electrical parameters.

Table 5-5. 1.8V SDIO Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6. GPADC Electrical Characteristics

The GPADC contains 4-ch analog-to-digital(ADC) converter. Table 5-6 lists GPADC electrical characteristics.

Table 5-6. GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Quantizing Error	-	8	-	LSB
Clock Frequency	-	-	1	MHz
Conversion Time	-	14	-	ADC Clock Cycles

5.7. LRADC Electrical Characteristics

The LRADC is 6-bit resolution ADC for key application. The LRADC can work up to 2kHz conversion rate. Table 5-7 lists LRADC electrical characteristics.

Table 5-7. LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range	0	-	LEVELB(1)	V
Quantizing Error	-	2	-	LSB
Clock Frequency	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles
(1) The maximum value of LEVELB is 1.266V. For details, see the register description of LRADC in ***Allwinner_T507&T507-H_User_Manual.***				

5.8. Audio Codec Electrical Characteristics

Test conditions: VDD_SYS = 0.9 V, AVCC = 1.8 V, TA = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, 16-bit audio data unless otherwise stated.

Table 5-8. Audio Codec Typical Performance

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	**DACL/DACR to LINEOUTL/R(R=10 kΩ)**					
	Full-scale Level	0dBFS 1 kHz	-	0.56	-	Vrms
	SNR(A-weighted)	0data	-	94	-	dB
	THD+N	0dBFS 1 kHz	-	-84	-	dB
	Noise	0data	-	11	-	uV

5.9. Clock Electrical Characteristics

5.9.1. Input Clock Requirements

The T507/T507-H has two clock inputs. Each clock input passes through an internal oscillator which can be connected to an external crystal.

The 24 MHz oscillator provides a 24 MHz reference clock which is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through DXIN. Table 5-9 lists the recommended values of 24 MHz crystal.

Table 5-9. 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24	-	MHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-

The 32.768 kHz oscillator provides a 32.768 kHz reference clock which is used for RTC and low frequency operation. It supplies the wake-up domain for operation in low-power mode. The clock is provided through X32KIN. Table 5-10 lists the recommended values of 32.768 kHz crystal.

Table 5-10. 32.768 kHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	32.768	-	kHz
	Frequency Tolerance at 25 °C	-20	-	+20	ppm
	Oscillation Mode	Fundamental			-

5.10. External Memory Electrical Characteristics

5.10.1. SDRAM AC Electrical Characteristics

5.10.1.1. DDR3/DDR3L Parameters

Figure 5-2 shows the DDR3/DDR3L command and address timing diagram. The timing parameters for this diagram shows in Table 5-11.

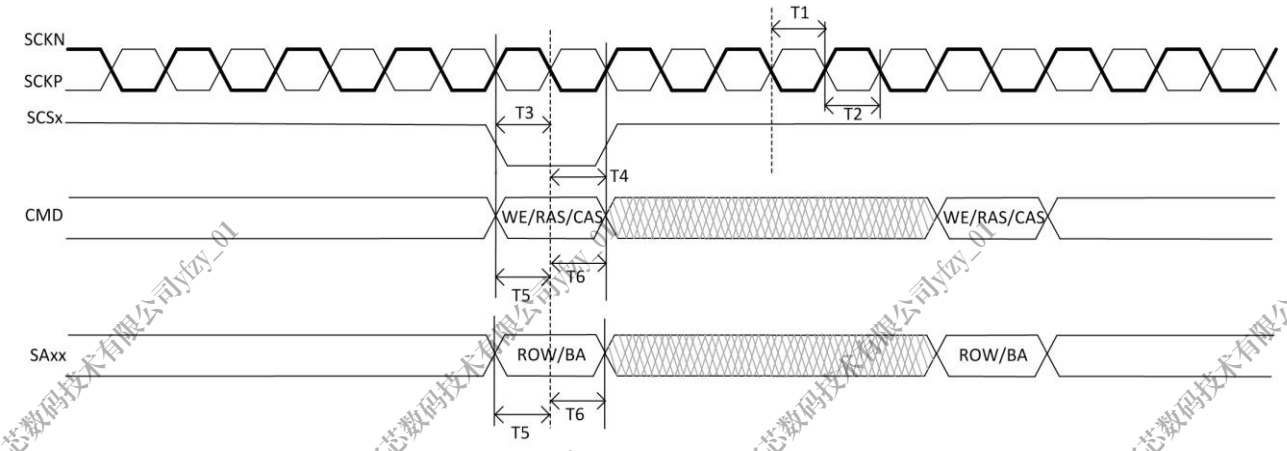


Figure 5-2. DDR3/DDR3L Command and Address Timing

Table 5-11. DDR3/DDR3L Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	SCKP clock high-level width	t_{CH}	0.47	-	0.53	tck
T2	SCKP clock low-level width	t_{CL}	0.47	-	0.53	tck
T3	CS setup time	t_{IS}	170	295	-	ps
T4	CS hold time	t_{IH}	120	245	-	ps
T5	Command and Address setup time to Clock edge	t_{IS}	170	295	-	ps
T6	Command and Address hold time to Clock edge	t_{IH}	120	245	-	ps

T1 and T2 are in reference to Vref level.
T3,T4,T5, and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-3 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram shows in Table 5-12.

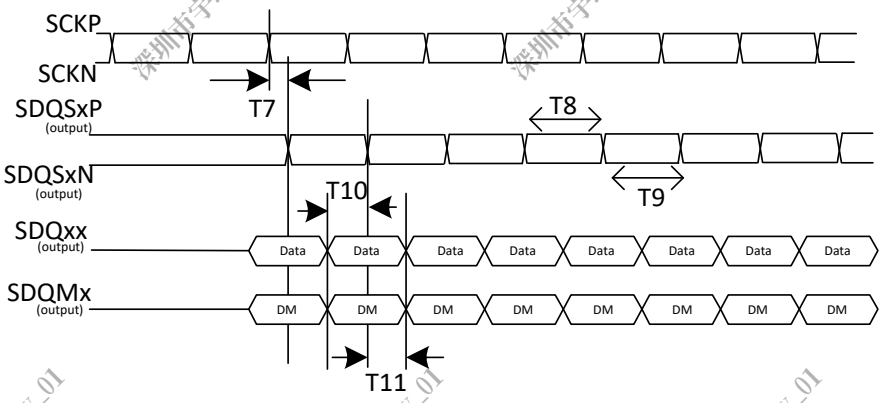


Figure 5-3. DDR3/DDR3L Write Cycle

Table 5-12. DDR3/DDR3L Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T7	SDQSxP/SDQSxN rising edge to SCKP/SCKN	t_{DQSS}	-0.27	-	0.27	t_{CK}

	rising edge					
T8	SDQSxP high level width	t_{DQSH}	0.45	-	0.55	t_{CK}
T9	SDQSxP low level width	t_{DQSL}	0.45	-	0.55	t_{CK}
T10	Data setup time to SDQSxP/SDQSxN	t_{DS}	10	145	-	ps
T11	Data hold time to SDQSxP/SDQSxN	t_{DH}	45	180	-	ps

To receive the reported setup and hold values, writing calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7,T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-4 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram shows in Table 5-13.

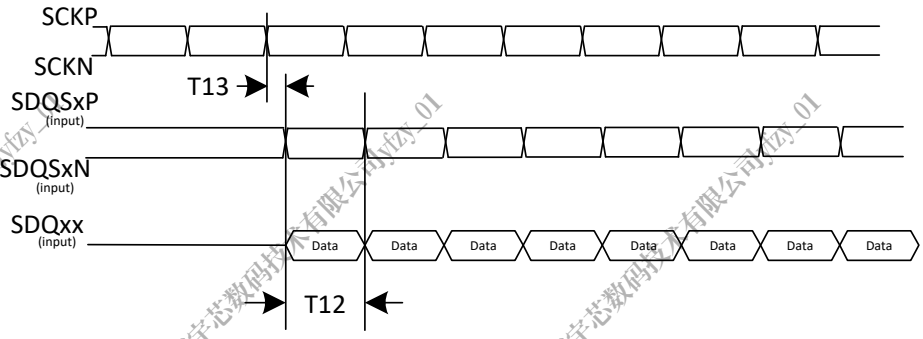


Figure 5-4. DDR3/DDR3L Read Cycle

Table 5-13. DDR3/DDR3L Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T12	Read Data valid width	t_{Data}	200	-	ps
T13	SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge	t_{DQSCK}	-225	225	ps

To receive the reported setup and hold values, writing calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 and T13 are in reference to Vref level.

5.10.1.2. LPDDR3 Parameters

Figure 5-5 shows the LPDDR3 command and address timing diagram. The timing parameters for this diagram shows in Table 5-14.

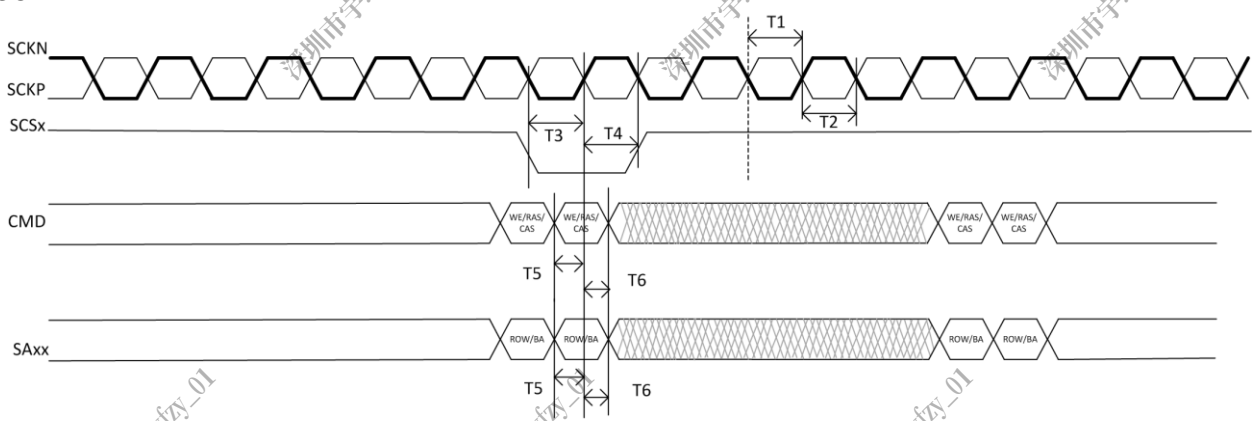


Figure 5-5. LPDDR3 Command and Address Timing Diagram

Table 5-14. LPDDR3 Command and Address Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	Clock high pulse width	t_{CH}	0.45	-	0.55	t_{CK}

T2	Clock low pulse width	t_{CL}	0.45	-	0.55	t_{CK}
T3	SCSx input setup time	t_{ISCS}	195	347.5	-	ps
T4	SCSx input hold time	t_{IHCS}	220	372.5	-	ps
T5	Address and control input setup time	t_{IAS}	75	152.5	-	ps
T6	Address and control input hold time	t_{IAH}	100	177.5	-	ps

T1 and T2 are in reference to Vref level.
T3,T4,T5,and T6 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).
Figure 5-6 shows the LPDDR3 write timing diagram. The timing parameters for this diagram shows in Table 5-15.

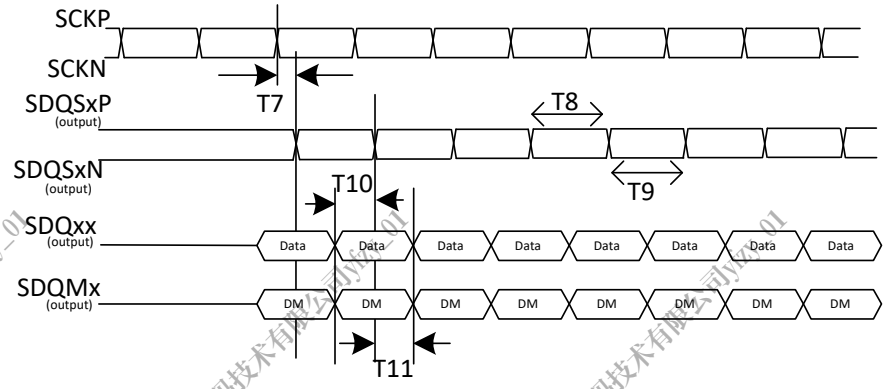


Figure 5-6. LPDDR3 Write Cycle

Table 5-15. LPDDR3 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T7	SDQSxP/SDQSxN rising edge to SCKP/SCKN rising edge	t_{DQSS}	0.75	-	1.25	t_{CK}
T8	SDQSx input high-level width	t_{DQSH}	0.4	-	-	t_{CK}
T9	SDQSx input low-level width	t_{DQSL}	0.4	-	-	t_{CK}
T10	SDQxx and SDQMx input setup time	t_{DS}	75	152.5	-	ps
T11	SDQxx and SDQMx input hold time	t_{DH}	100	177.5	-	ps

To receive the reported setup and hold values, the write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T7, T8, and T9 are in reference to Vref level.
T10 and T11 are in reference to Vih(ac) /Vil(ac) levels. (AC150/DC100).

Figure 5-7 shows the LPDDR3 read timing diagram. The timing parameters for this diagram shows in Table 5-16.

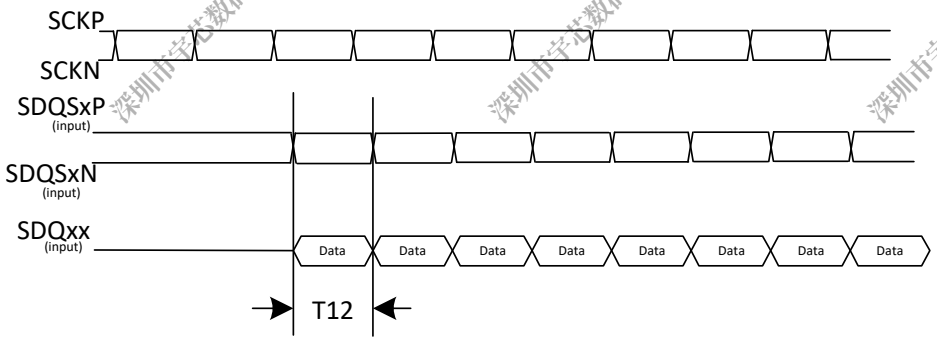


Figure 5-7. LPDDR3 Read Cycle

Table 5-16. LPDDR3 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T12	Read Data valid width	t_{DATA}	200	-	ps

To receive the reported setup and hold values, write calibration should be performed in order to locate the SDQSx in the middle of SDQxx window.
T12 is in reference to Vref level.

5.10.1.3. DDR4 Parameters

Figure 5-8 shows the DDR4 command and address timing diagram. The timing parameters foe this diagram shows in Table 5-17.

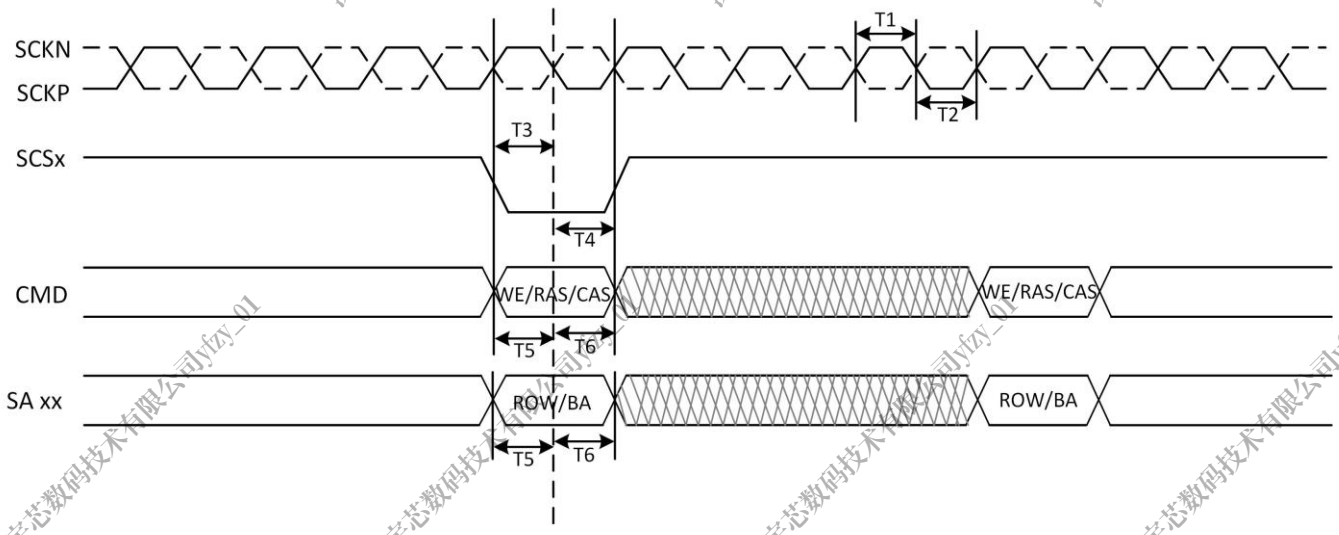


Figure 5-8. DDR4 Command and Address Timing

Table 5-17. DDR4 Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T1	Clock high-level width	t_{CH}	0.48	-	0.52	tck
T2	Clock low-level width	t_{CL}	0.48	-	0.52	tck
T3	CS setup time	t_{IS}	115	-	-	ps
T4	CS hold time	t_{IH}	140	-	-	ps
T5	Command and Address setup time to CK	t_{IS}	115	-	-	ps
T6	Command and Address hold time to CK	t_{IH}	140	-	-	ps

T1~T2 are in reference to Vref level.
T3/T5 are in reference to Vih(ac) / Vil(ac) levels.(AC100)
T4/T6 are in reference to Vih(ac) / Vil(ac) levels.(DC75)

Figure 5-9 shows the DDR4 write timing diagram. The timing parameter for this diagram shows in Table 5-18.

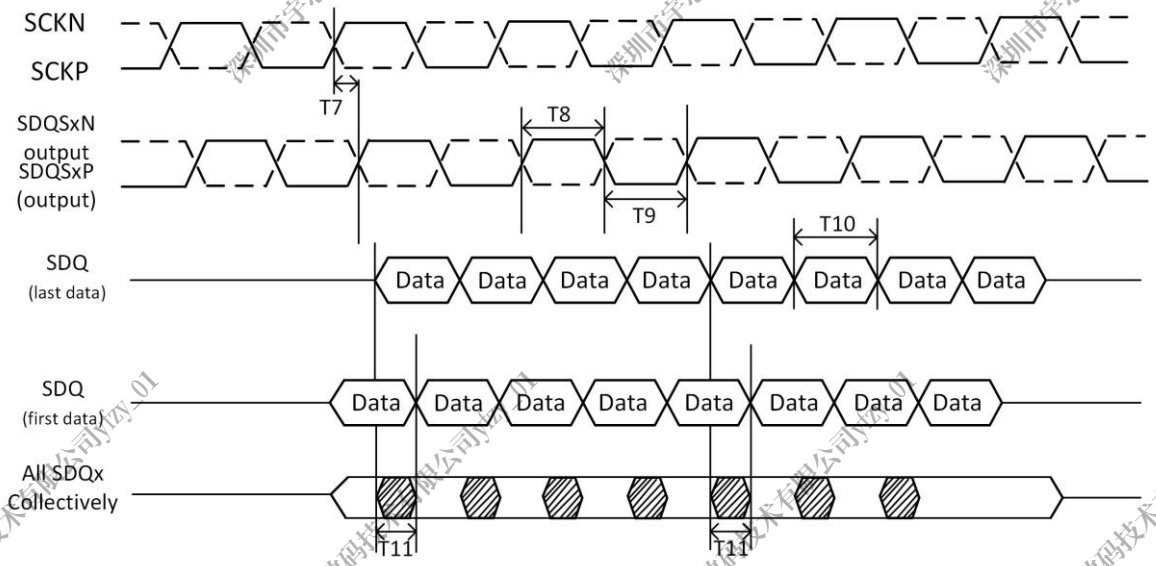


Figure 5-9. DDR4 Write Cycle

Table 5-18. DDR4 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T7	SDQS rising edge to SCK rising edge	t_{DQSS}	-0.27	-	0.27	t_{CK}
T8	SDQS high level width	t_{DQSH}	0.46	-	0.54	t_{CK}
T9	SDQS low level width	t_{DQSL}	0.46	-	0.54	t_{CK}
T10	Data Valid Window per pin per UI	t_{DVWp}	0.66	-	-	t_{ui}
T11	Data Valid Window per device per UI	t_{DVWd}	0.63	-	-	t_{ui}

T7~T9 are in reference to Vref level.
T10 is Data Valid Window per pin per UI and is derived from (t_{QH} - t_{DQSQ}) of each UI on a pin of a given DRAM.
T11 is the Data Valid Window per device per UI and is derived from (t_{QH} - t_{DQSQ}) of each UI on a given DRAM.

Figure 5-10 shows the DDR4 read timing diagram. The timing parameters for this diagram shows in Table 5-19.

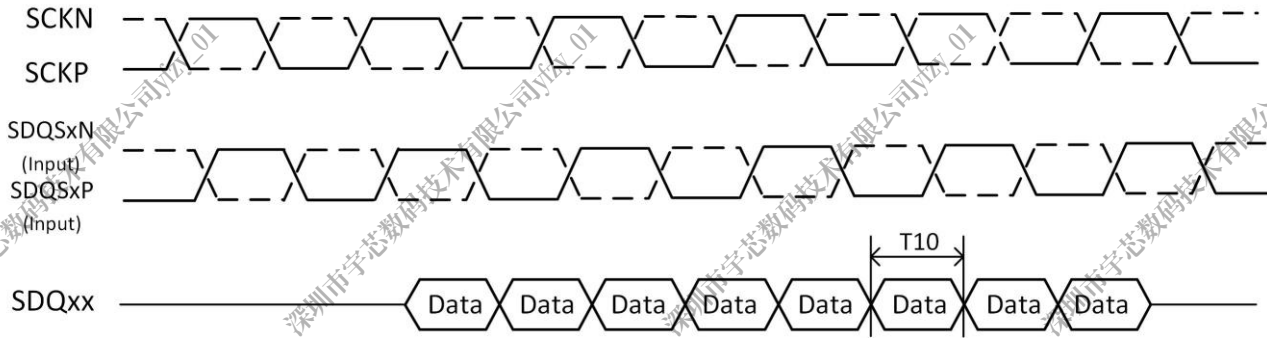


Figure 5-10. DDR4 Read Cycle

Table 5-19. DDR4 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	
T10	Data Valid Window per pin per UI	t_{DVWp}	0.66	-	t_{ui}

T10 is in reference to Vref level.

5.10.1.4. LPDDR4 Parameters

Figure 5-11 shows the LPDDR4 command and address timing diagram. The timing parameters for this diagram shows in Table 5-20.

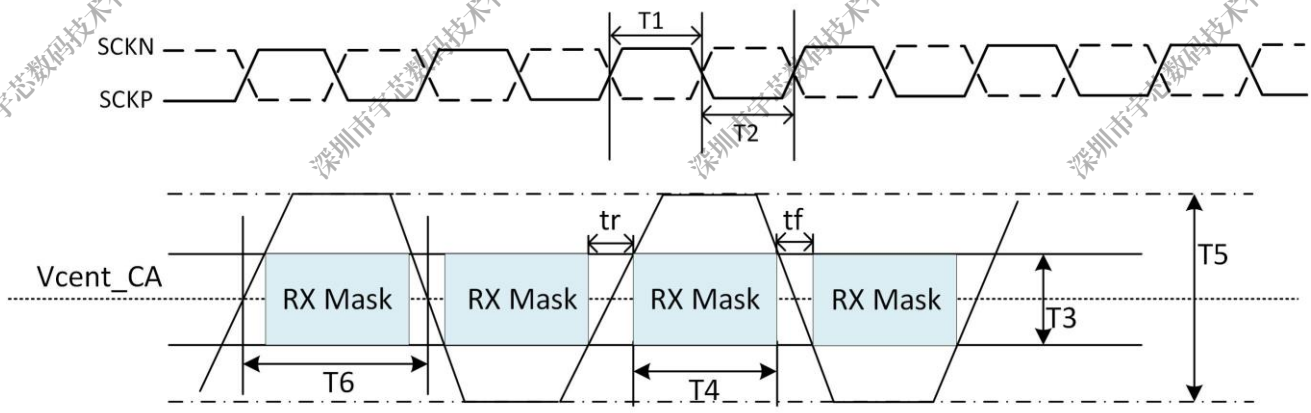


Figure 5-11. LPDDR4 Command and Address Timing Diagram

NOTE

T7 = T3/(tr or tf), signal must be monotonic within tr and tf range.

Table 5-20. LPDDR4 Command and Address Timing Parameters

ID	Parameter	Symbol	Clock = 792 MHz	Unit

			Min	Suggest	Max	
T1	Clock high pulse width	t_{CH}	0.46	-	0.54	t_{CK}
T2	Clock low pulse width	t_{CL}	0.46	-	0.54	t_{CK}
T3	Rx Mask voltage - p-p	V_{cIVW}	-	-	175	mV
T4	Rx timing window	T_{cIVW}	-	-	0.3	UI
T5	CA AC input pulse amplitude pk-pk	V_{IHL_AC}	210	-	-	mV
T6	CA input pulse width	T_{cIPW}	0.55	-	-	UI
T7	Input Slew Rate over VcIVW	SR_{IN_cIVW}	1	-	7	V/ns

Figure 5-12 shows the LPDDR4 write timing diagram. The timing parameters for this diagram shows in Table 5-21.

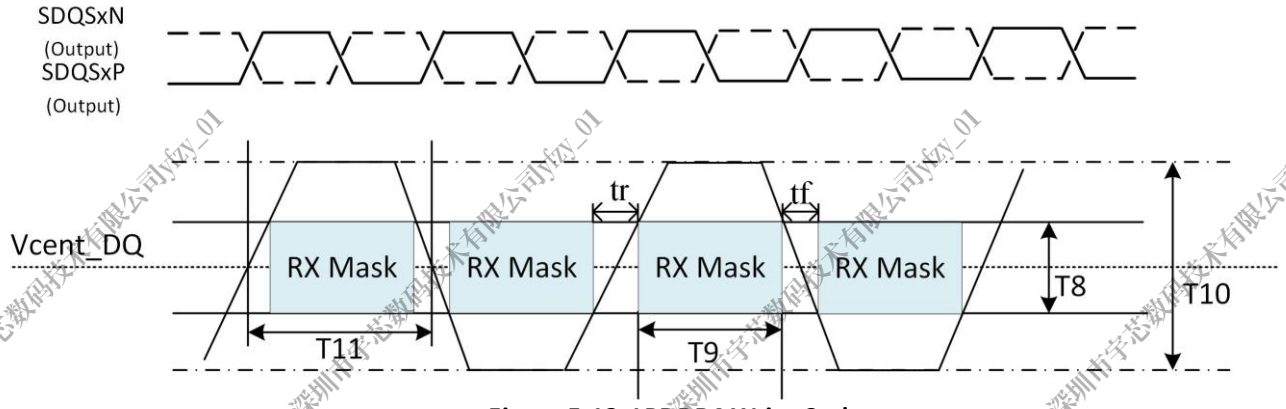


Figure 5-12. LPDDR4 Write Cycle

NOTE

T12 = T8/(tr or tf), signal must be monotonic within tr and tf range.

Table 5-21. LPDDR4 Write Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz			Unit
			Min	Suggest	Max	
T8	Rx Mask voltage - p-p total	V_{dIVW_total}	-	-	140	mV
T9	Rx timing window total (At VdIVW voltage levels)	T_{dIVW_total}	-	-	0.22	UI
T10	DQ AC input pulse amplitude pk-pk	V_{IHL_AC}	180	-	-	mV
T11	Input pulse width (At Vcent_DQ)	T_{dIPW_DQ}	0.45	-	-	UI
T12	Input Slew Rate over VdIVW_total	SR_{IN_dIVW}	1	-	7	V/ns

Figure 5-13 shows the LPDDR4 read timing diagram. The timing parameters for this diagram shows in Table 5-22.

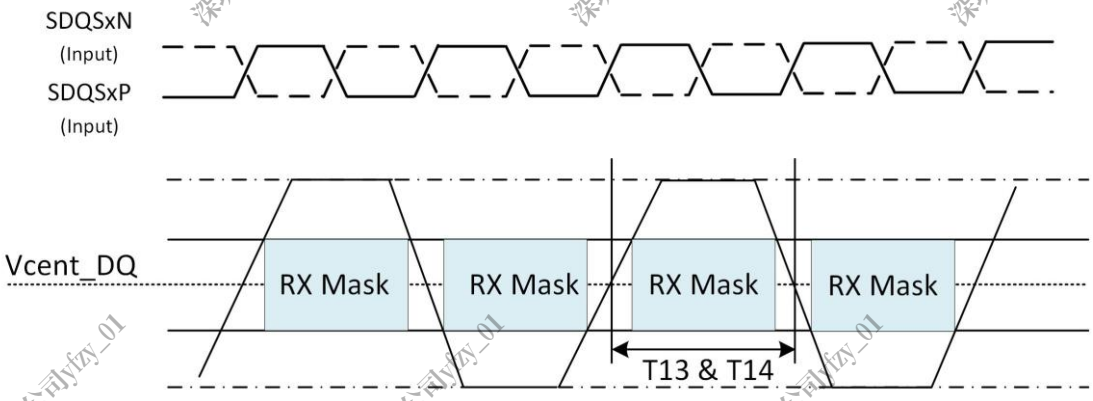


Figure 5-13. LPDDR4 Read Cycle

Table 5-22. LPDDR4 Read Cycle Parameters

ID	Parameter	Symbol	Clock = 792 MHz		Unit
			Min	Max	

T13	DQ output window time total, per pin (DBI-Disabled)	t_{QW_total}	0.75	-	UI
T14	DQ output window time total, per pin (DBI-Enabled)	$t_{QW\_total\_DBI}$	0.75	-	UI

5.10.2. Nand AC Electrical Characteristics

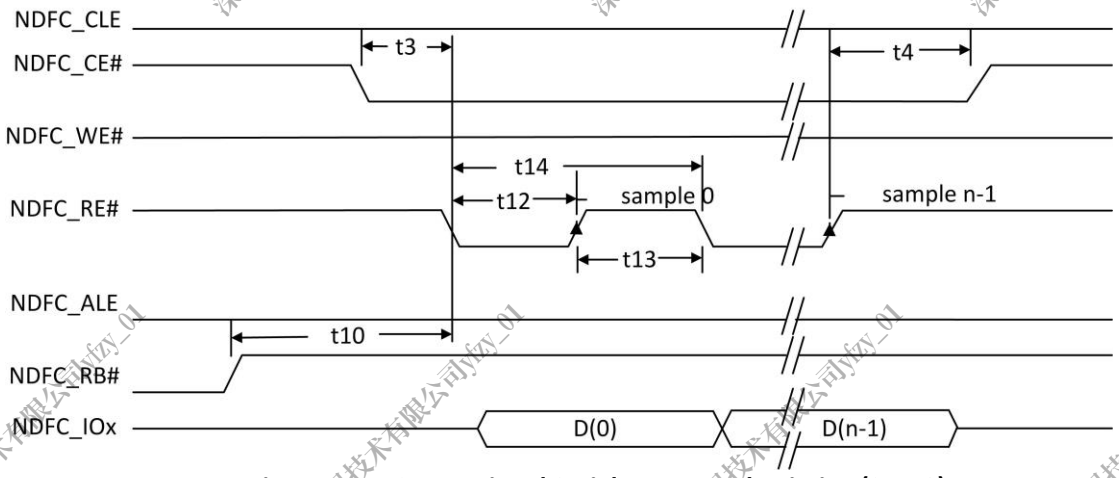


Figure 5-14. Conventional Serial Access Cycle Timing (SAM0)

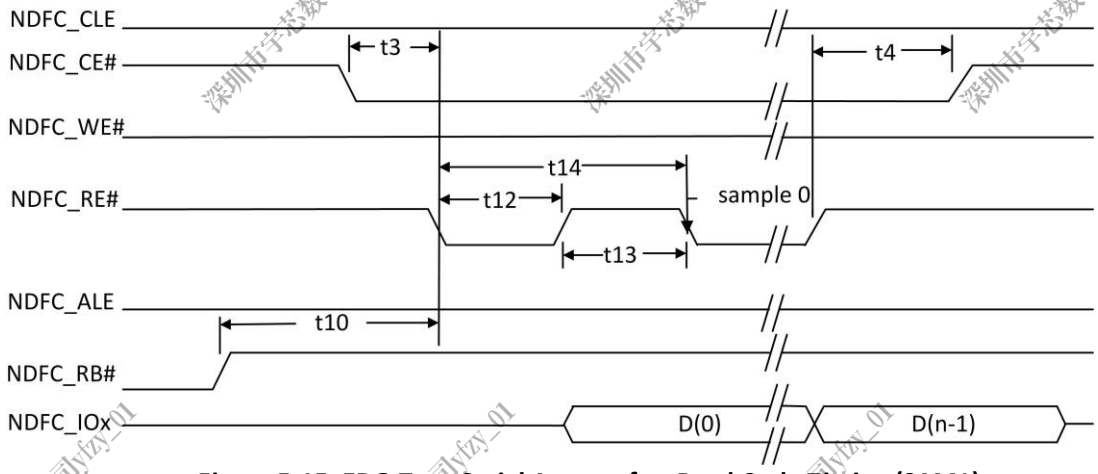


Figure 5-15. EDO Type Serial Access after Read Cycle Timing (SAM1)

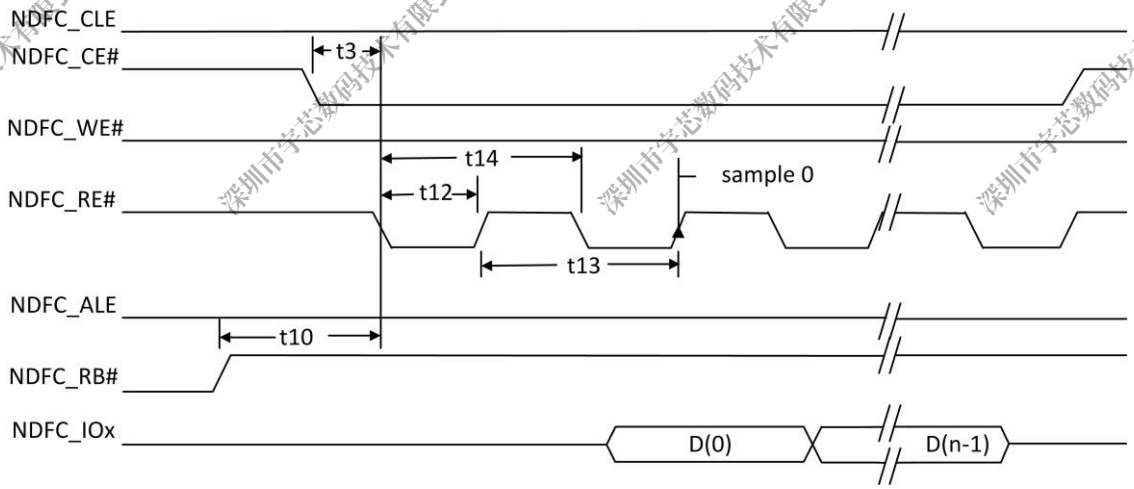


Figure 5-16. Extending EDO Type Serial Access Mode Timing (SAM2)

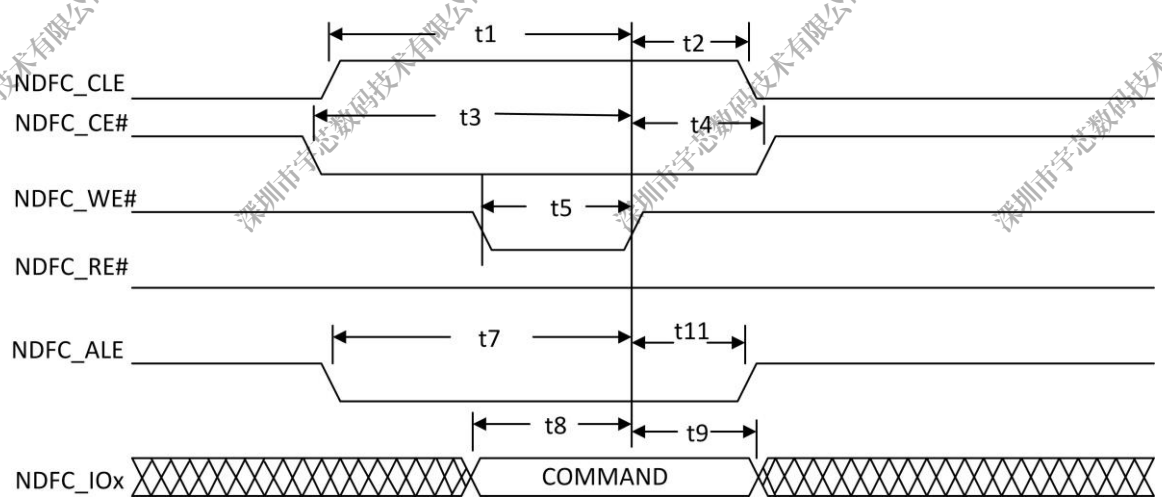


Figure 5-17. Command Latch Cycle Timing

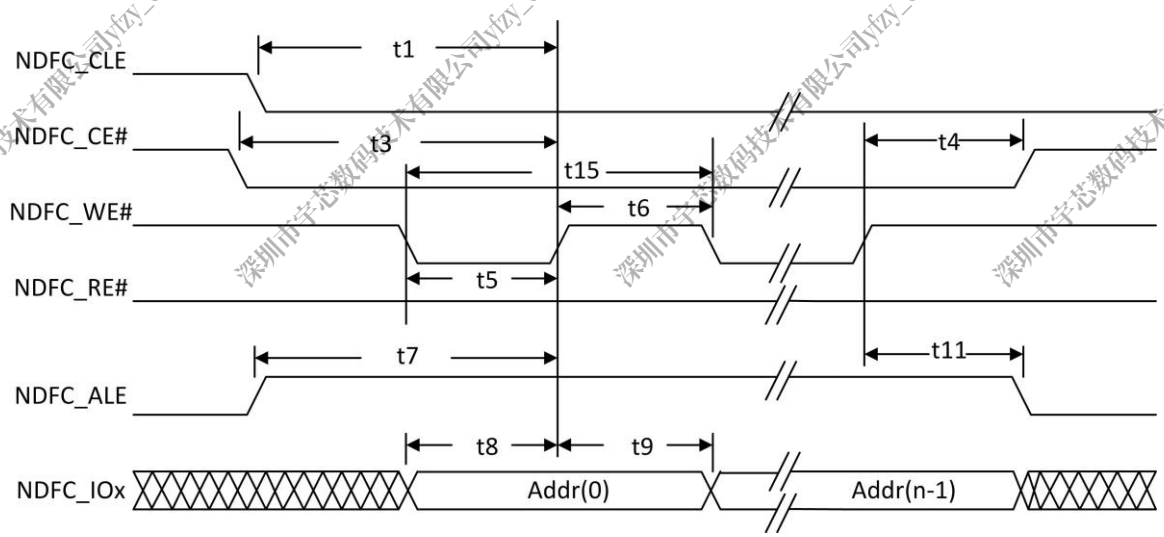


Figure 5-18. Address Latch Cycle Timing

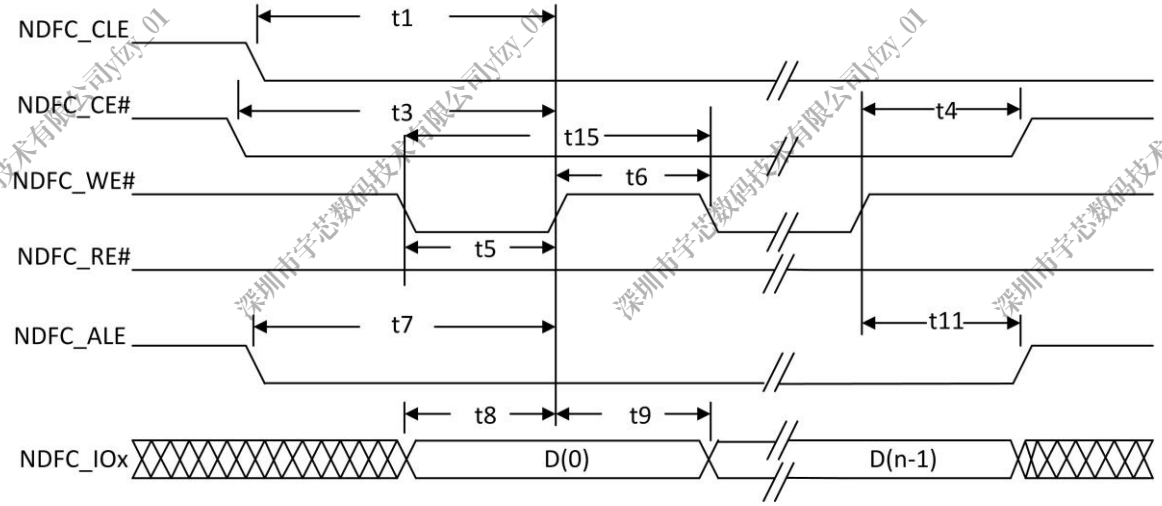


Figure 5-19. Write Data to Flash Cycle Timing

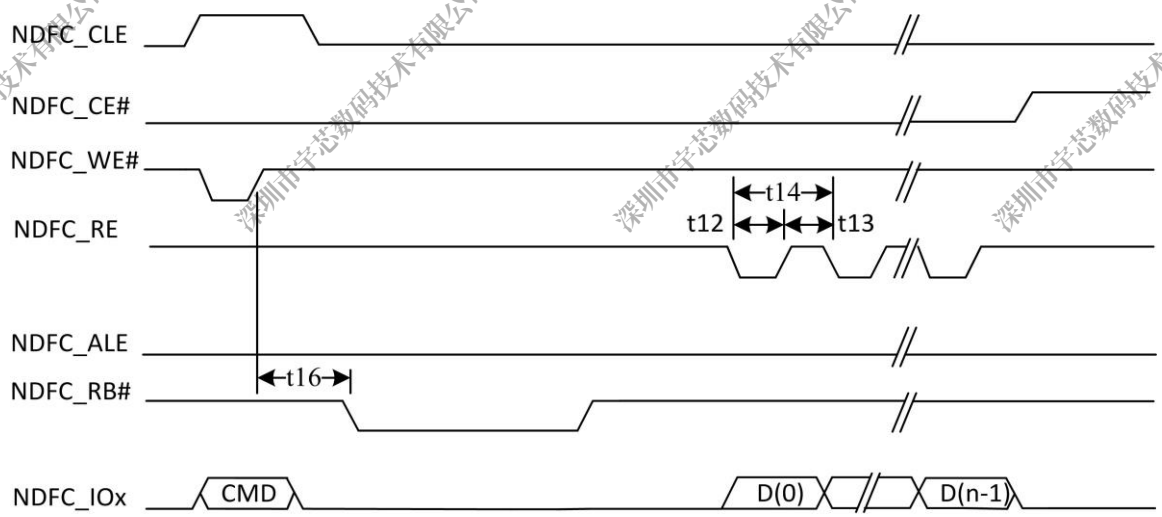


Figure 5-20. Waiting R/B# Ready Timing

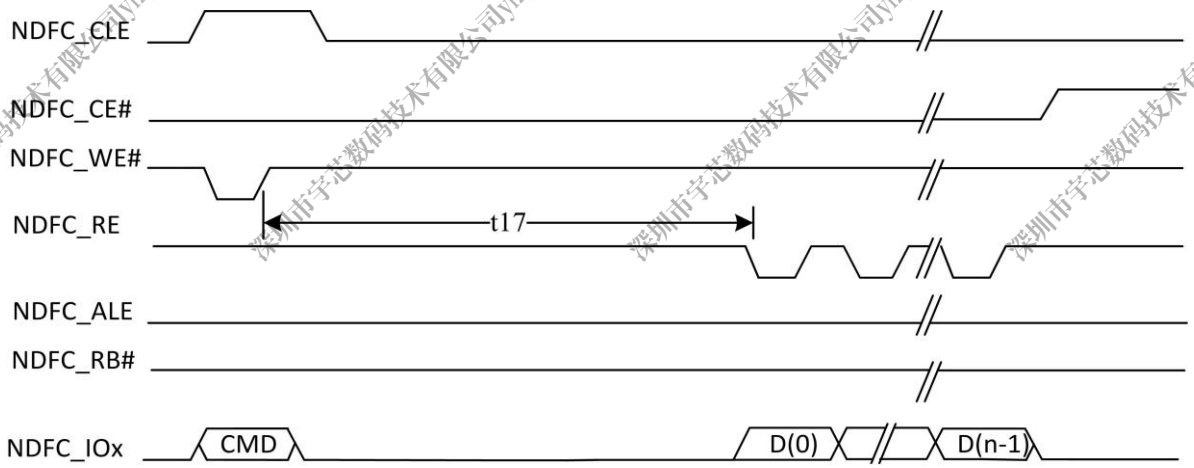


Figure 5-21. WE# High to RE# Low Timing

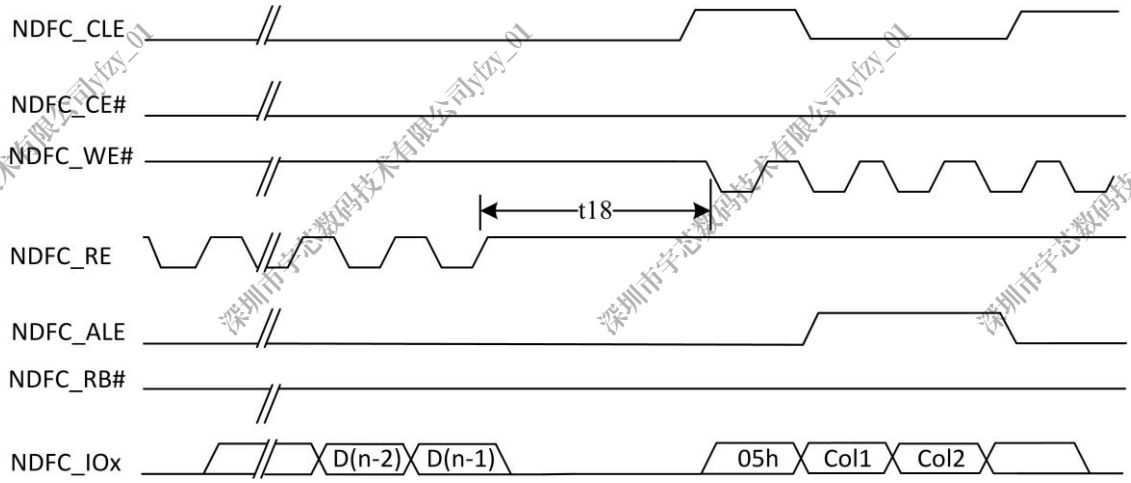


Figure 5-22. RE# High to WE# Low Timing

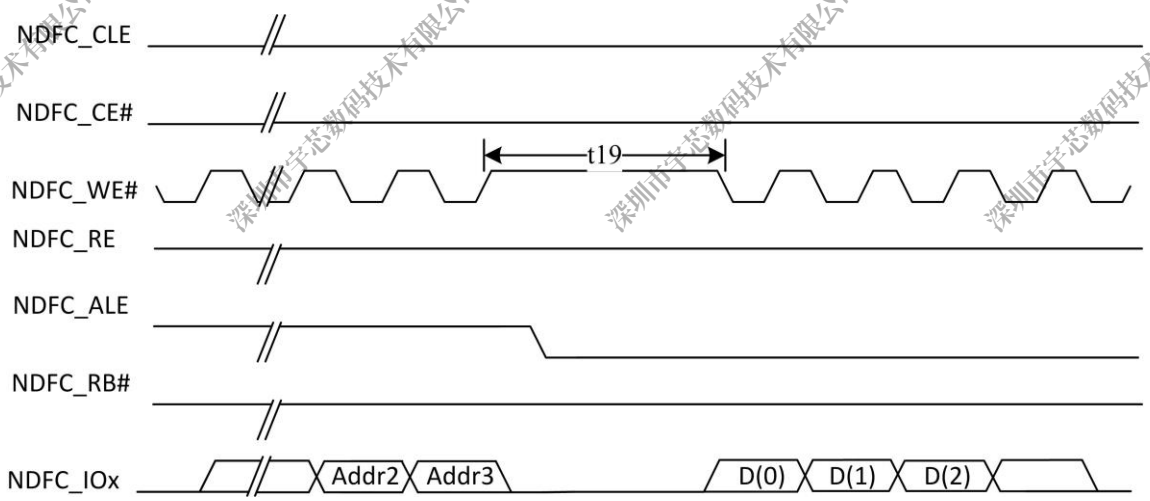


Figure 5-23. Address to Data Loading Timing

Table 5-23. NAND Timing Constants

Parameter	Symbol	Timing	Unit
NDFC_CLE setup time	t1	2T	ns
NDFC_CLE hold time	t2	2T	ns
NDFC_CE setup time	t3	2T	ns
NDFC_CE hold time	t4	2T	ns
NDFC_WE# pulse width	t5	T(1)	ns
NDFC_WE# hold time	t6	T	ns
NDFC_ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC_RE# low	t10	3T	ns
NDFC_ALE hold time	t11	2T	ns
NDFC_RE# pulse width	t12	T	ns
NDFC_RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC_WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC_WE# high to NDFC_RE# low	t17	T_WHR(3)	ns
NDFC_RE# high to NDFC_WE# low	t18	T_RHW(4)	ns
Address to Data Loading time	t19	T_ADL(5)	ns
(1):T is the cycle of internal clock. (2),(3),(4),(5): This values is configurable in nand flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 0*2T/6*2T/14*2T/22*2T, the value of T_RHW could be 4*2T/12*2T/20*2T/28*2T, the value of T_ADL could be 0*2T/6*2T/14*2T/22*2T.			

5.10.3. SMHC AC Electrical Characteristics

5.10.3.1. SMHC0/SMHC1

(1) SDR Mode(<100MHz)

The contents of this section can be applied to DS, HS, SDR12, SDR25, SDR50, SDR104(<100MHz) speed mode.

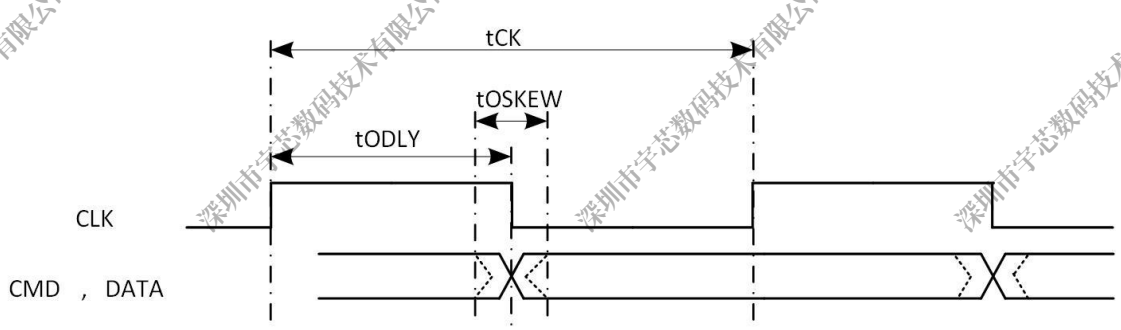


Figure 5-24. SMHC0/1 SDR Mode Output Timing Diagram

Table 5-24. SMHC0/1 SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.625	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

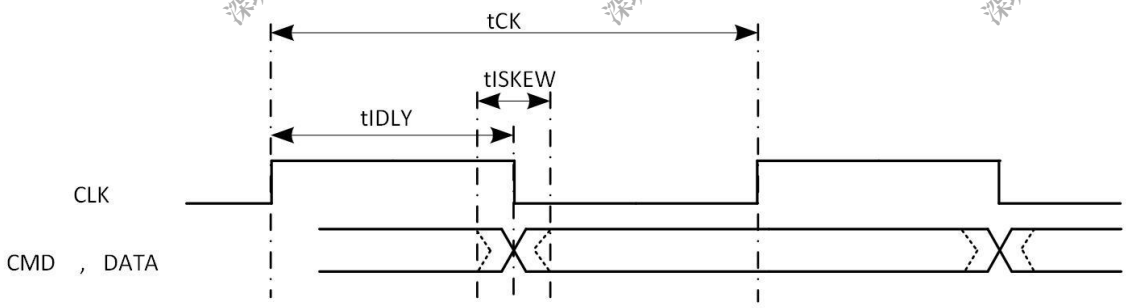


Figure 5-25. SMHC0/1 SDR Mode Input Timing Diagram

Table 5-25. SMHC0/1 SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
NOTE (1): The driver strength level of GPIO is 2 for test.					

(2) DDR50 Mode

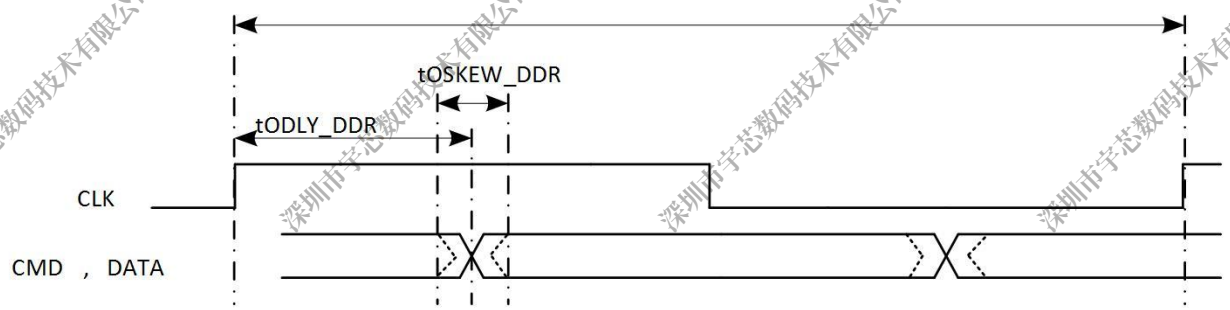


Figure 5-26. SMHC0/1 DDR50 Mode Output Timing Diagram

Table 5-26. SMHC0/1 DDR50 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI
Data output delay skew time	tOSKEW_DDR	-	-	0.884	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

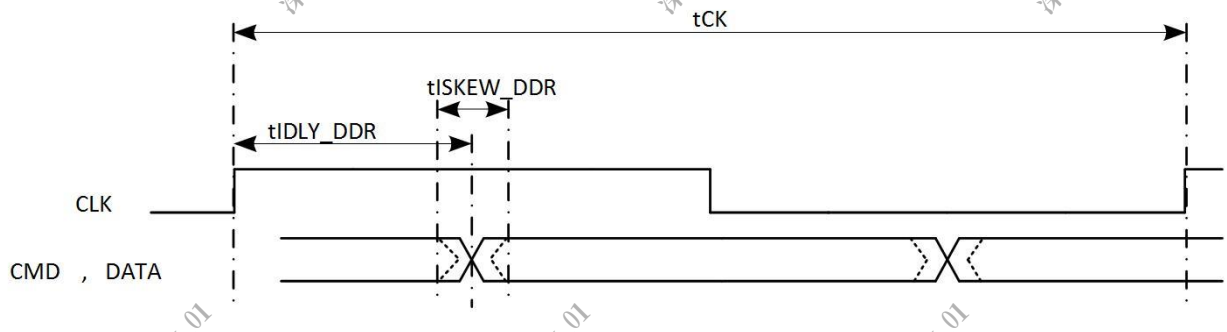


Figure 5-27. SMHC0/1 DDR50 Mode Input Timing Diagram

Table 5-27. SMHC0/1 DDR50 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-c	8.3	ns
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns
NOTE (1): The driver strength level of GPIO is 2 for test.					

(3) SDR104 Mode(>100MHz)

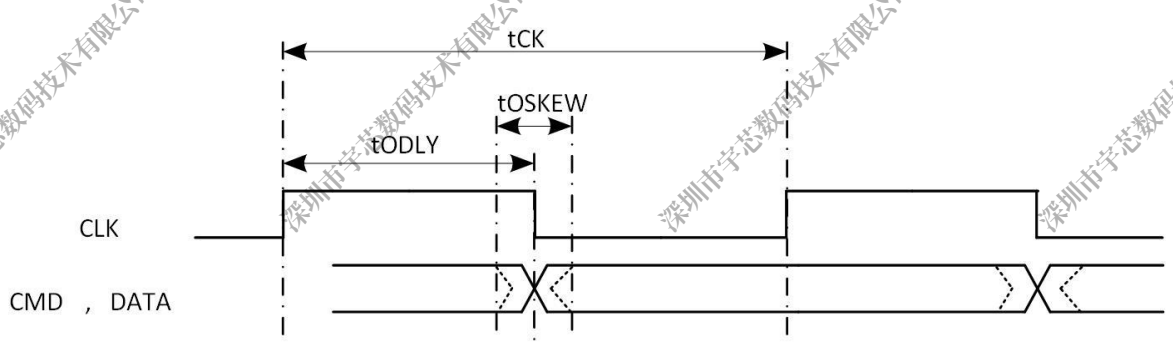


Figure 5-28. SMHC0/1 SDR104 Mode Output Timing Diagram

Table 5-28. SMHC0/1 SDR104 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	-	150	MHz
Duty cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-		0.884	ns
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**					

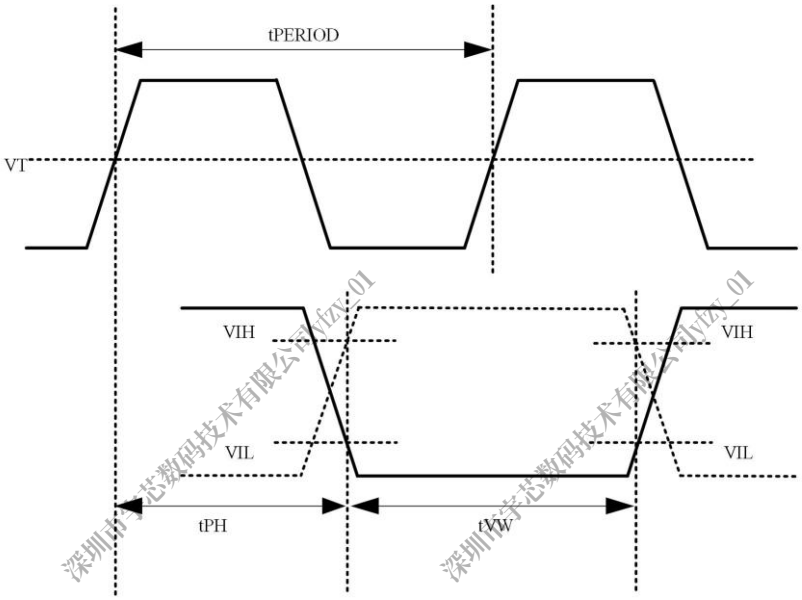


Figure 5-29. SMHC0/1 SDR104 Mode Input Timing Diagram

Table 5-29. SMHC0/1 SDR104 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD,Data valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz.						

NOTE (2): The driver strength level of GPIO is 3 for test. **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**

5.10.3.2. SMHC2

(1) HS-SDR/HS-DDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

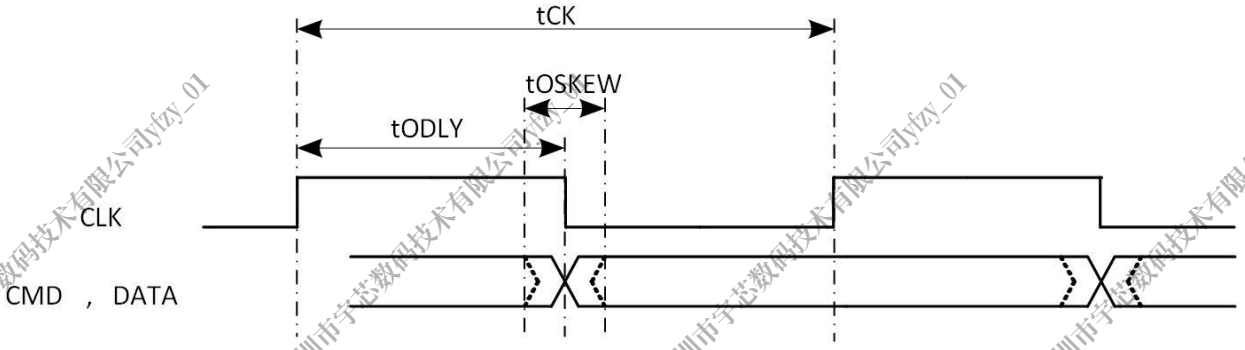


Figure 5-30. SMHC2 HS-SDR Mode Output Timing Diagram

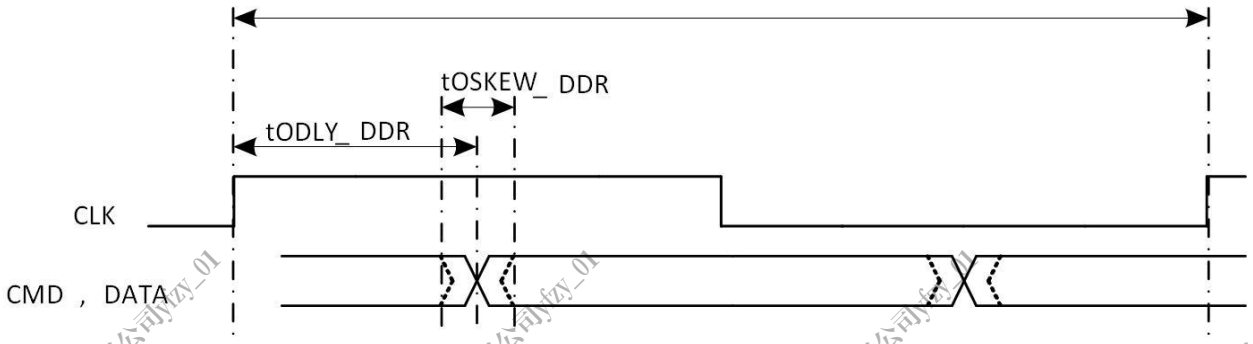


Figure 5-31. SMHC2 HS-DDR Mode Output Timing Diagram

Table 5-30. SMHC2 HS-SDR/HS-DDR Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
CMD, Data output delay time in DDR mode	tODLY_DDR	-	0.25	0.25	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=20ns at 50MHz. **NOTE (2): The driver strength level of GPIO is 2 for test.**						

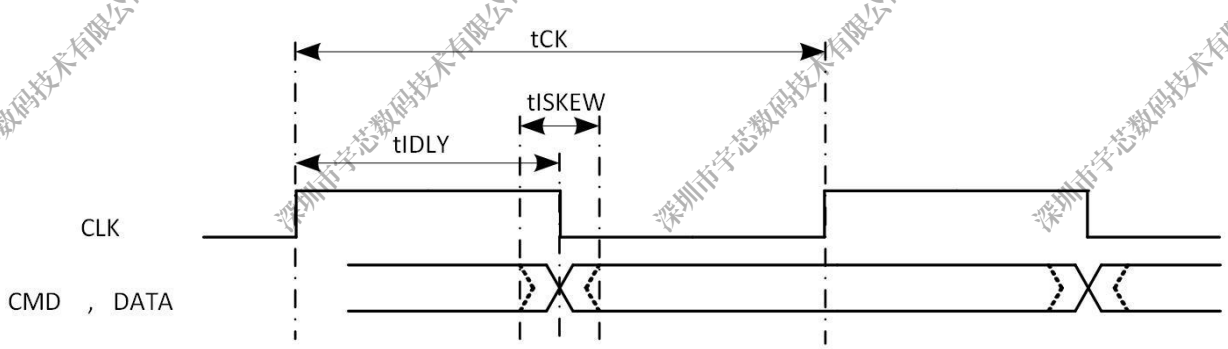


Figure 5-32. SMHC2 HS-SDR Mode Input Timing Diagram

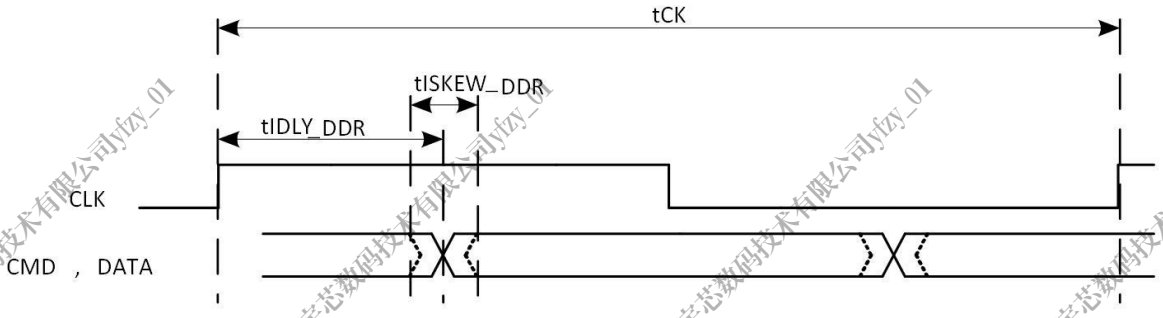


Figure 5-33. SMHC2 HS-DDR Mode Input Timing Diagram

Table 5-31. SMHC2 HS-SDR/HS-DDR Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock frequency	tCK	0	50	50	MHz	
Duty cycle	DC	45	50	55	%	
Input CMD, DATA(referenced to CLK 50MHz)						
Data input delay in SDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY	-	-	20	ns	
Data input delay in DDR mode. It includes Clock's PCB delay time, Data's PCB delay time and device's data output delay	tIDLY_DDR	-	-	8.3	ns	
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns	
Data input skew time in DDR mode	tISKEW_DDR	-	-	0.858	ns	
NOTE (1): The driver strength level of GPIO is 2 for test.						

(2) HS200 Mode

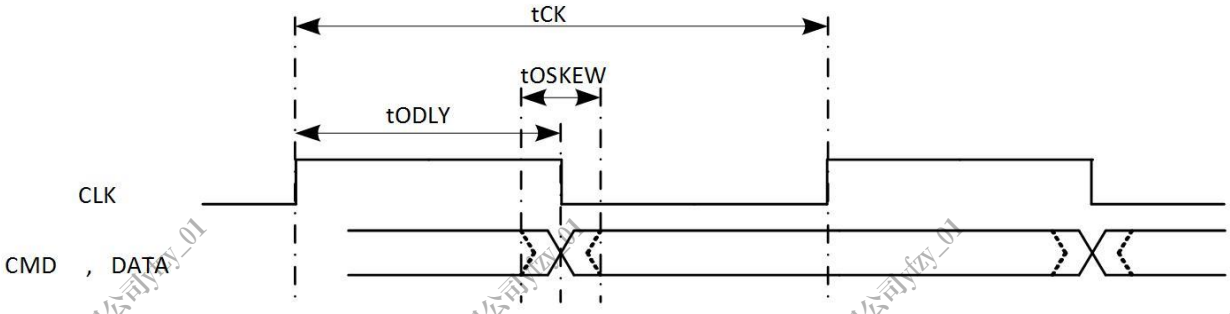


Figure 5-34. SMHC2 HS200 Mode Output Timing Diagram

Table 5-32. SMHC2 HS200 Mode Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark

CLK						
Clock frequency	tCK	-	-	150	MHz	
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Output CMD, DATA(referenced to CLK)						
CMD, Data output delay time	tODLY	-	0.25	0.5	UI	
Data output delay skew time	tOSKEW	-	-	0.884	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

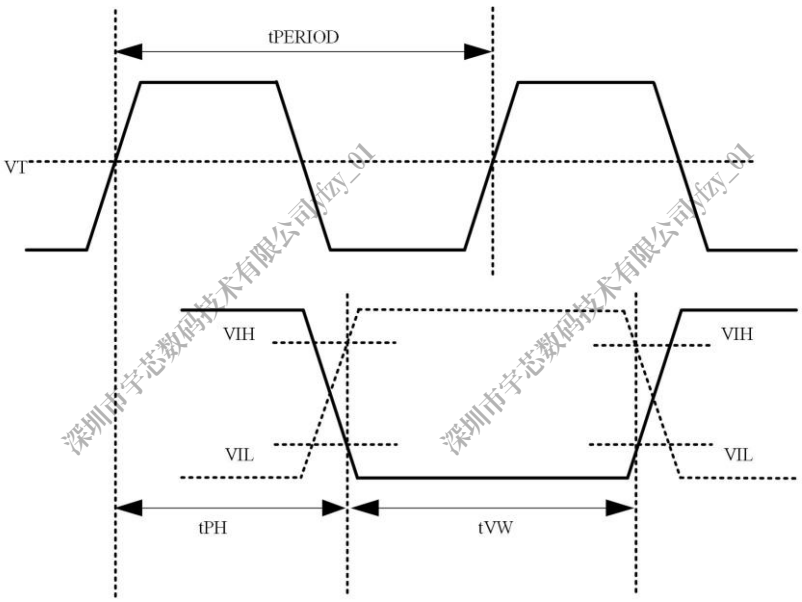


Figure 5-35. SMHC2 HS200 Mode Input Timing Diagram

Table 5-33. SMHC2 HS200 Mode Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max:150MHz
Duty cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA(referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350[3]	-	1550[4]	ps	
CMD, DATA valid window	tVW	0.575	-	-	UI	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.** **NOTE (3): Temperature variation: -20°C.** **NOTE (4): Temperature variation: 90°C.**						

(3) HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

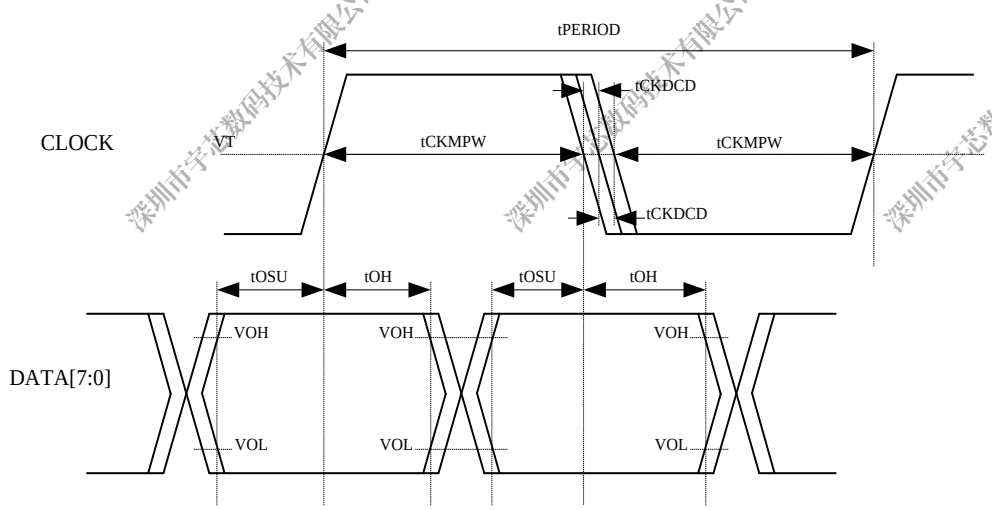


Figure 5-36. SMHC2 HS400 Mode Data Output Timing Diagram

Table 5-34. SMHC2 HS400 Mode Data Output Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	10	-	-	ns	Max:100MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA(referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

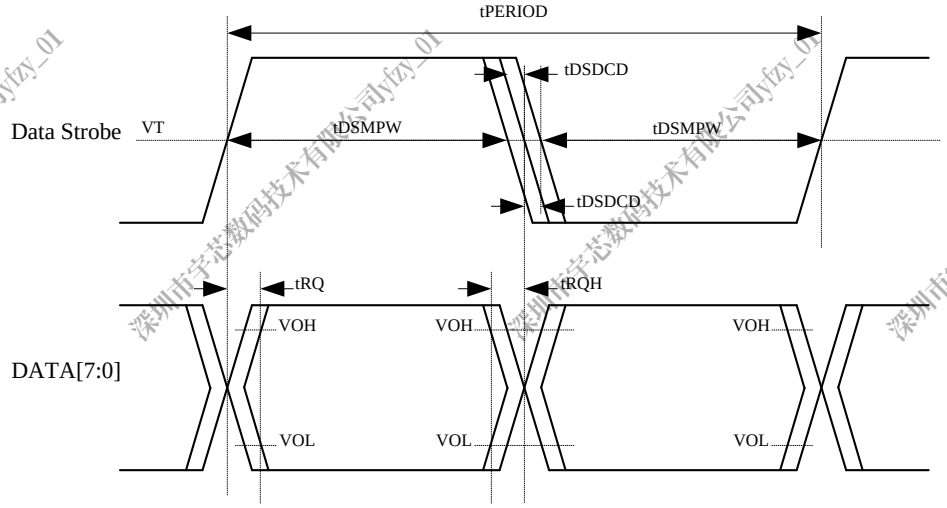


Figure 5-37. SMHC2 HS400 Mode Data Input Timing Diagram

Table 5-35. SMHC2 HS400 Mode Data Input Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS(Data Strobe)						
DS period	tPERIOD	10	-	-	ns	Max:100MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA(referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	

Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
NOTE (1): Unit Interval (UI) is one bit nominal time. For example, UI=10ns at 100MHz. **NOTE (2): The driver strength level of GPIO is 3 for test.**						

5.11. External Peripheral Electrical Characteristics

5.11.1. LCD AC Electrical Characteristics

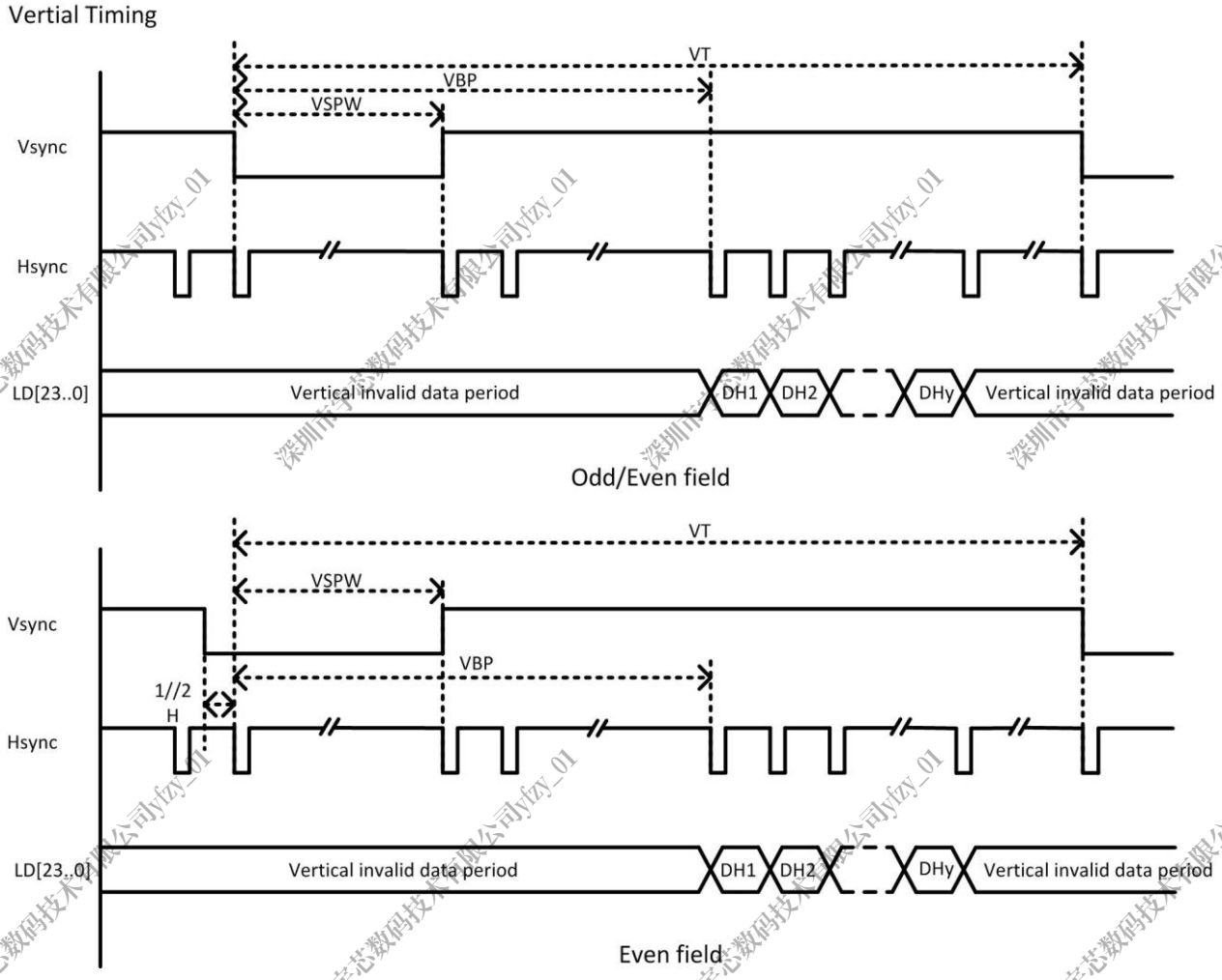


Figure 5-38. HV_IF Interface Vertical Timing

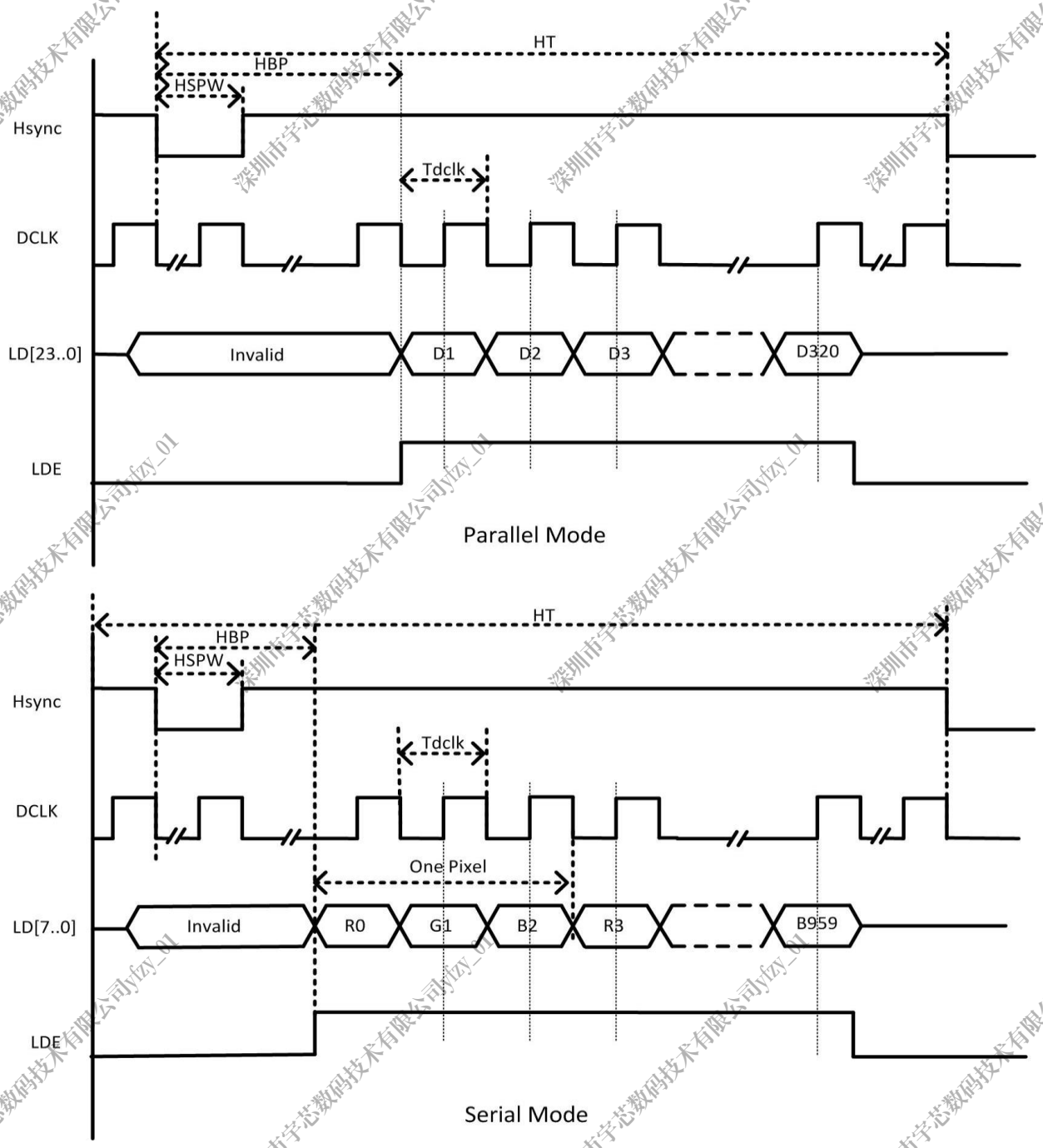


Figure 5-39. HV_IF Interface Horizontal Timing

Table 5-36. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
Hsync period time	tHT	-	HT+1	-	tDCLK
Hsync width	tHSPW	-	HSPW+1	-	tDCLK
Hsync back porch	tHBP	-	HBP+1	-	tDCLK
Vsync period time	tVT	-	VT/2	-	tHT
Vsync width	tVSPW	-	VSPW+1	-	tHT
Vsync back porch	tVBP	-	VBP+1	-	tHT

(1) Vsync: Vertical sync, indicates one new frame.
(2) Hsync: Horizontal sync, indicate one new scan line.
(3) DCLK: Dot clock, pixel data are sync by this clock.
(4) LDE: LCD data enable.
(5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

5.11.2. CSI AC Electrical Characteristics

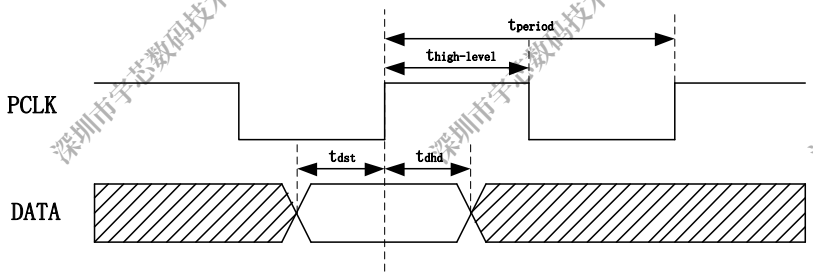


Figure 5-40. CSI Data Sample Timing

Table 5-37. CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.7	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.11.3. EMAC AC Electrical Characteristics

5.11.3.1. RMII

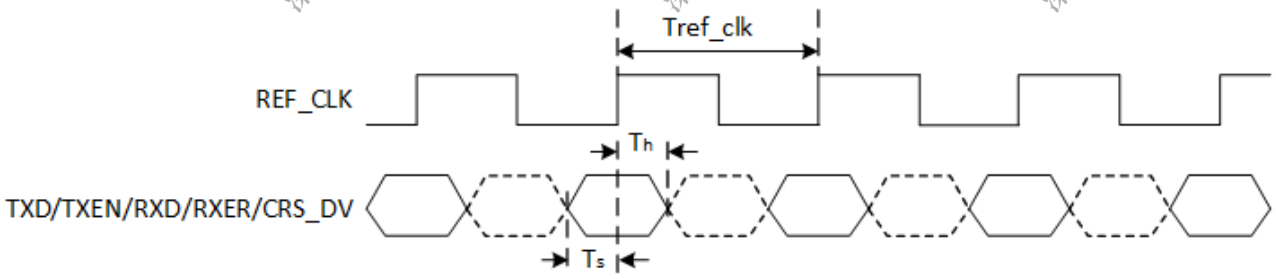


Figure 5-41. RMII Interface Timing

Table 5-38. RMII Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Reference clock period	T_{ref_clk}	-	20	-	ns
TXD/TXEN/RXD/RXER/CRS_DV to REF_CLK setup time	Ts	4	-	-	ns
TXD/TXEN/RXD/RXER/CRS_DV to REF_CLK hold time	Th	2	-	-	ns

5.11.3.2. RGMII

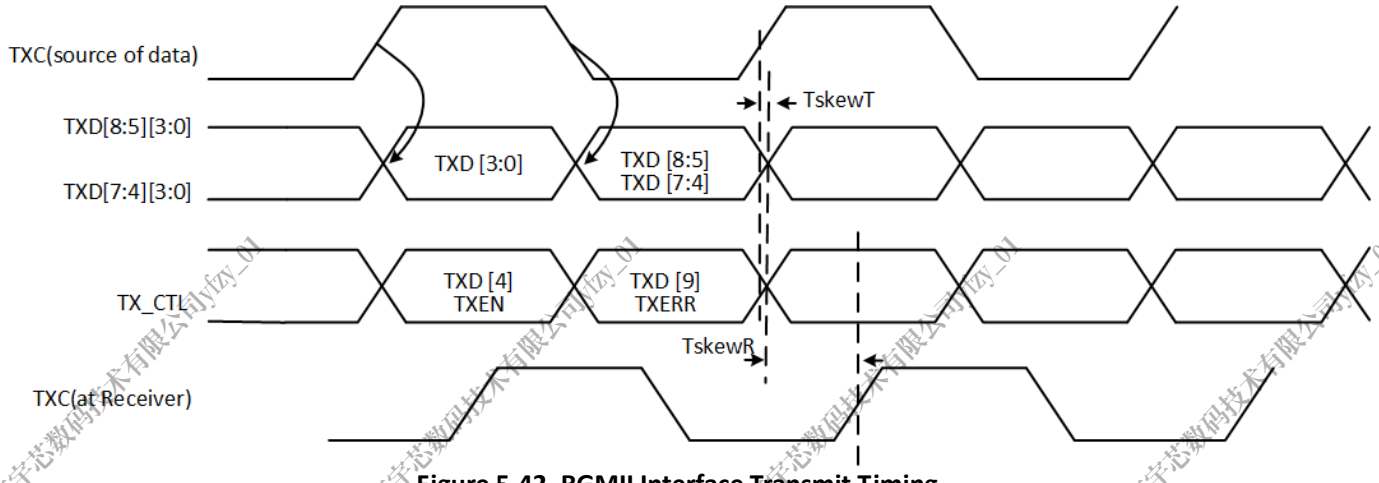


Figure 5-42. RGMII Interface Transmit Timing

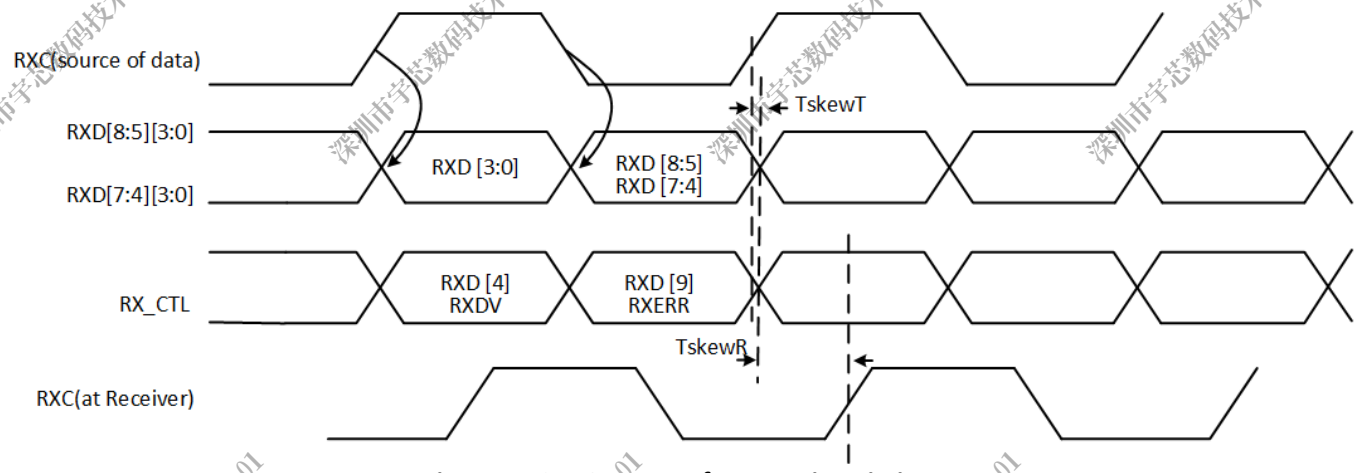


Figure 5-43. RGMII Interface Receive Timing

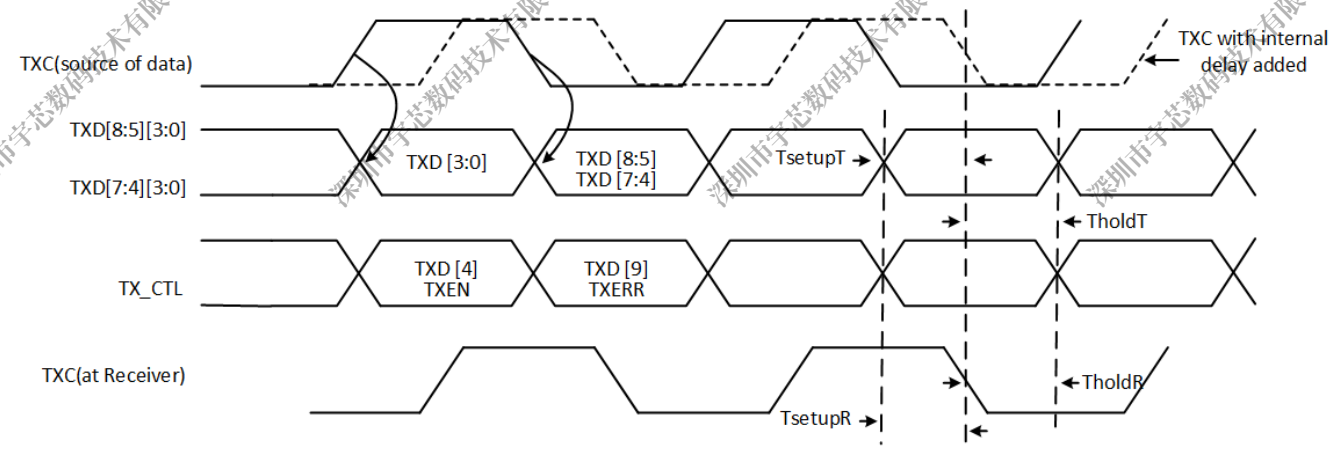


Figure 5-44. RGMII-ID Interface Transmit Timing

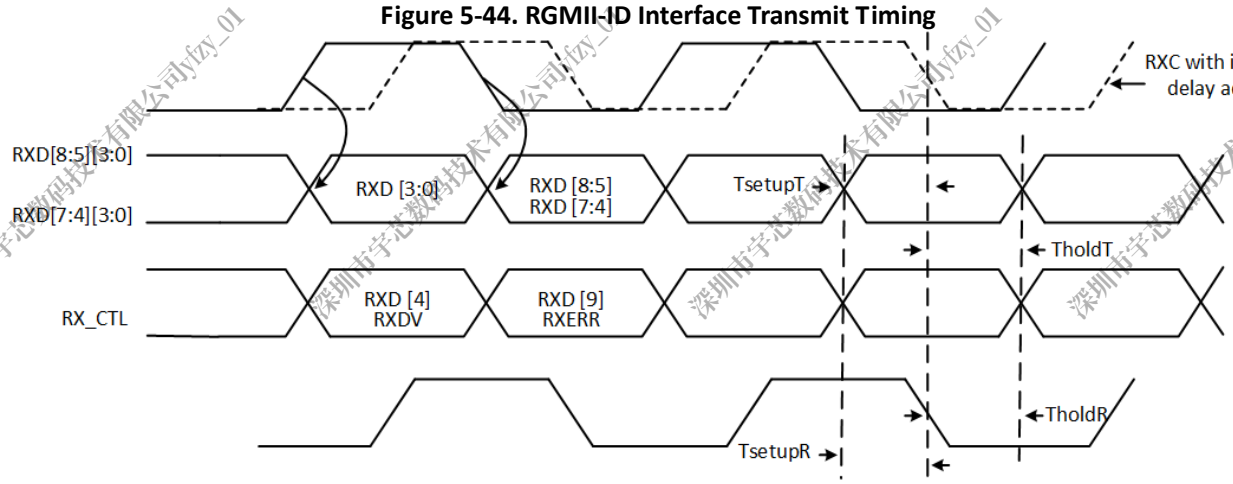


Figure 5-45. RGMII-ID Interface Receive Timing

Table 5-39. RGMII Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Data to Clock output Skew (at Transmitter)	TskewT	-500	0	500	ps
Data to Clock input Skew (at Receiver)	TskewR	1.0	1.8	2.6	ns
Data to Clock output Setup (at Transmitter – integrated delay)	TsetupT	1.2	2.0	-	ns
Clock to Data output Hold (at Transmitter –integrated delay)	TholdT	1.2	2.0	-	ns

Data to Clock input setup Setup (at Receiver –integrated delay)	TsetupR	1.0	2.0	-	ns
Data to Clock input setup Setup (at Receiver –integrated delay)	TholdR	1.0	2.0	-	ns
Clock Cycle Duration	Tcyc	7.2	8	8.8	ns
Duty Cycle for Gigabit	Duty_G	45	50	55	%
Duty Cycle for 10/100T	Duty_T	40	50	60	%
Rise / Fall Time (20-80%)	Tr/Tf	-	-	75	ns

5.11.4. CIR-RX AC Electrical Characteristics

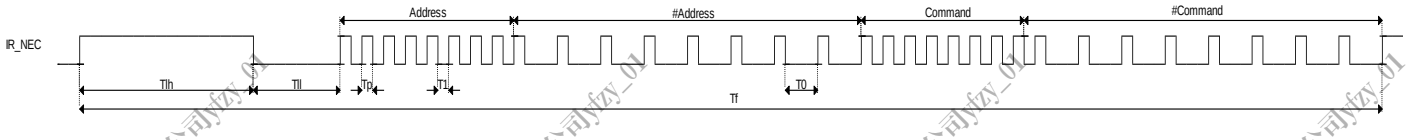


Figure 5-46. CIR-RX Timing

Table 5-40. CIR-RX Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Frame period	Tf	-	67.5	-	ms
Lead code high time	Tlh	-	9	-	ms
Lead code low time	Tll	-	4.5	-	ms
Pulse time	Tp	-	560	-	us
Logical 1 low time	T1	-	1680	-	us
Logical 0 low time	T0	-	560	-	us

5.11.5. SPI AC Electrical Characteristics

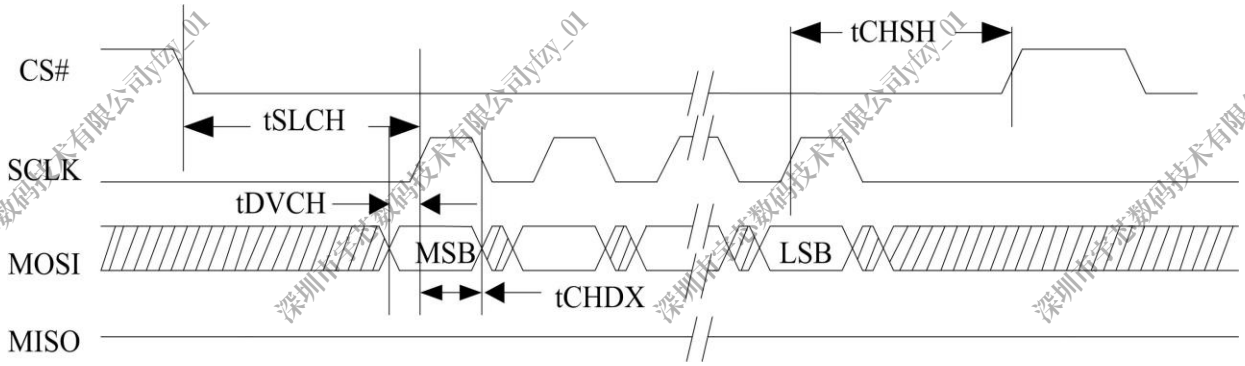


Figure 5-47. SPI MOSI Timing

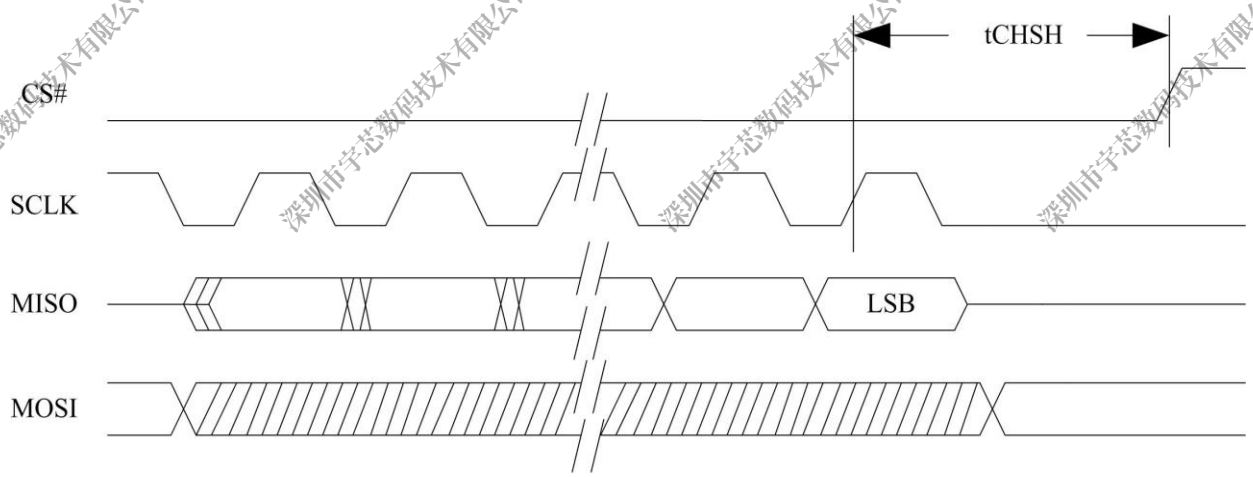


Figure 5-48. SPI MISO Timing

Table 5-41. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# active setup time	tSLCH	-	2T	-	ns
CS# active hold time	tCHSH	-	2T(1)	-	ns
Data in setup time	tDVCH	-	T/2-3	-	ns
Data in hold time	tCHDX	-	T/2-3	-	ns
NOTE (1):T is the cycle of clock.					

5.11.6. UART AC Electrical Characteristics

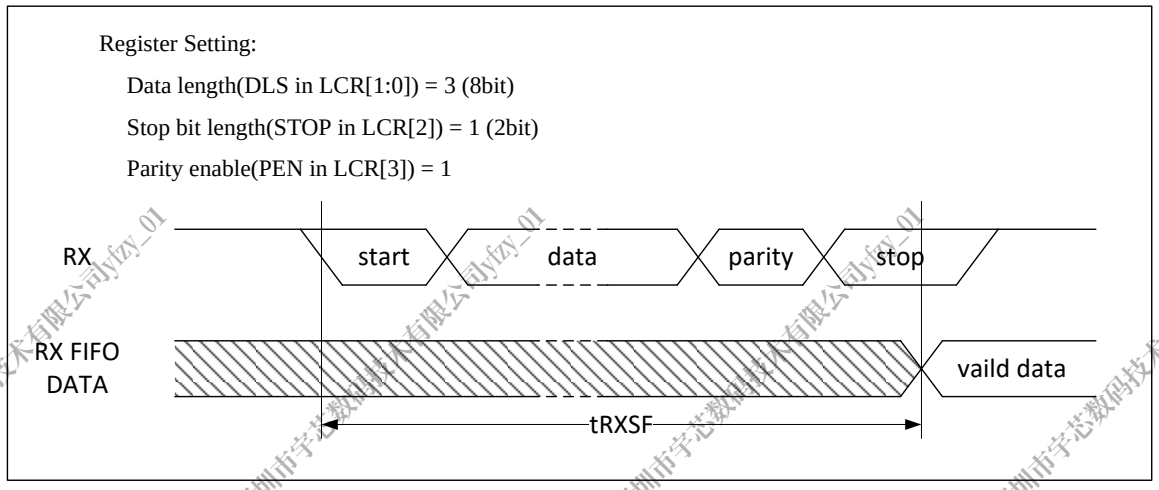


Figure 5-49. UART RX Timing

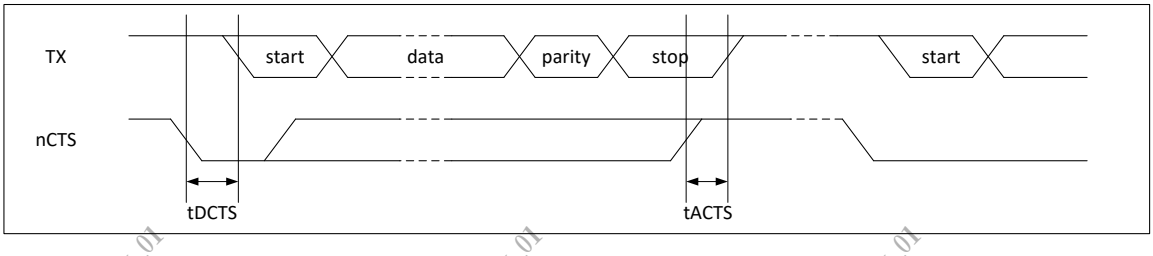


Figure 5-50. UART nCTS Timing

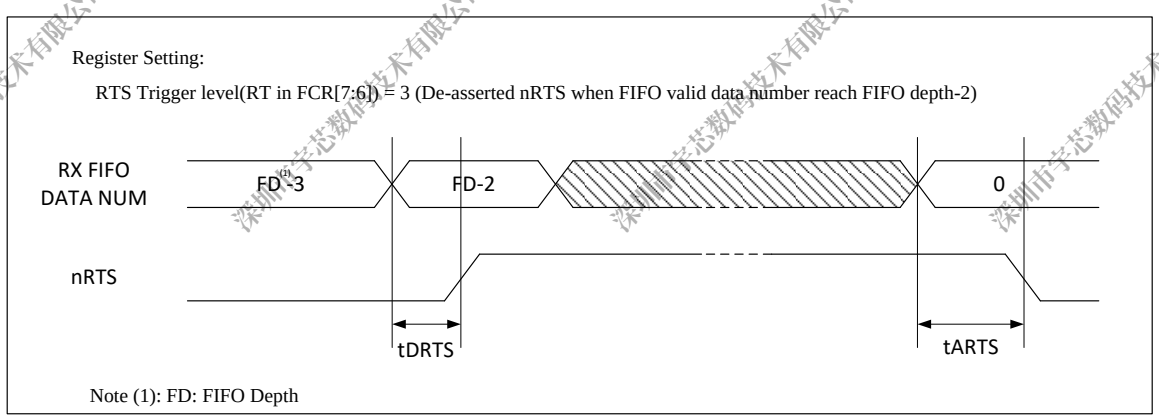


Figure 5-51. UART nRTS Timing

Table 5-42. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
NOTE (1): BRP(Baud-Rate Period).					

5.11.7. TWI AC Electrical Characteristics

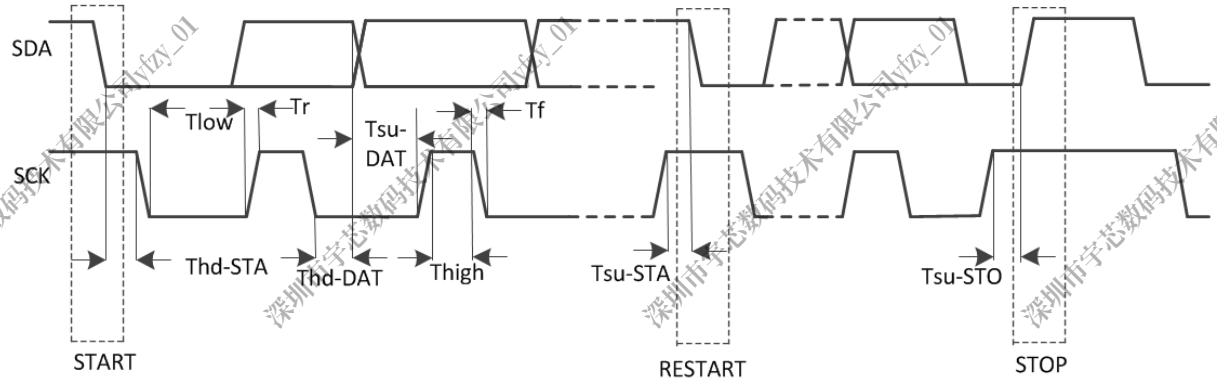


Figure 5-52. TWI Timing

Table 5-43. TWI Timing Constants

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup time in Start	Tsu-STA	4.7	-	0.6	-	us
Hold time in Start	Thd-STA	4.0	-	0.6	-	us
Setup time in Data	Tsu-DAT	250	-	100	-	ns
Hold time in Data	Thd-DAT	5.0	-	-	-	ns
Setup time in Stop	Tsu-STO	4.0	-	6.0	-	us
SCK low level time	Tlow	4.7	-	1.3	-	us
SCK high level time	Thigh	4.0	-	0.6	-	ns

SCK/SDA falling time	Tf	-	300	20	300	ns
SCK/SDA rising time	Tr	-	1000	20	300	ns

5.11.8. TSC AC Electrical Characteristics

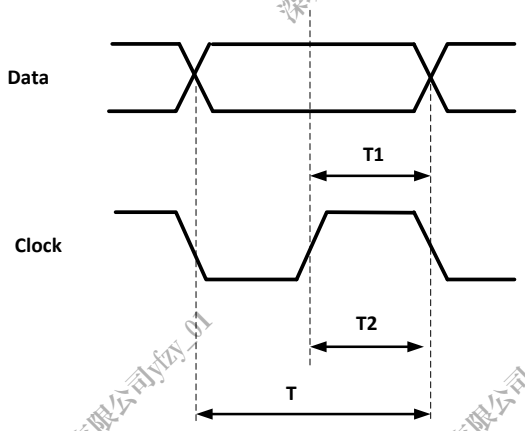


Figure 5-53. TSC Data and Clock Timing

Table 5-44. TSC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Data hold time	T1	$T^{[1]}/2-T^{[1]}/10$	$T^{[1]}/2$	$T^{[1]}/2+T^{[1]}/10$	us
Clock pulse width	T2	$T^{[1]}/2-T^{[1]}/10$	$T^{[1]}/2$	$T^{[1]}/2+T^{[1]}/10$	us
NOTE (1): T is the cycle of clock.					

5.11.9. SCR AC Electrical Characteristics

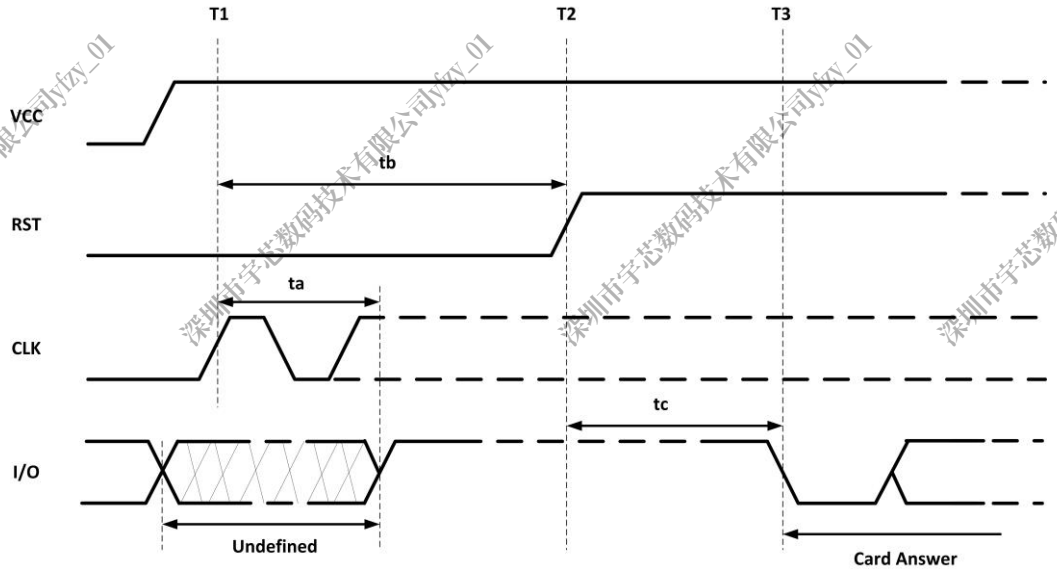


Figure 5-54. SCR Activation and Cold Reset Timing

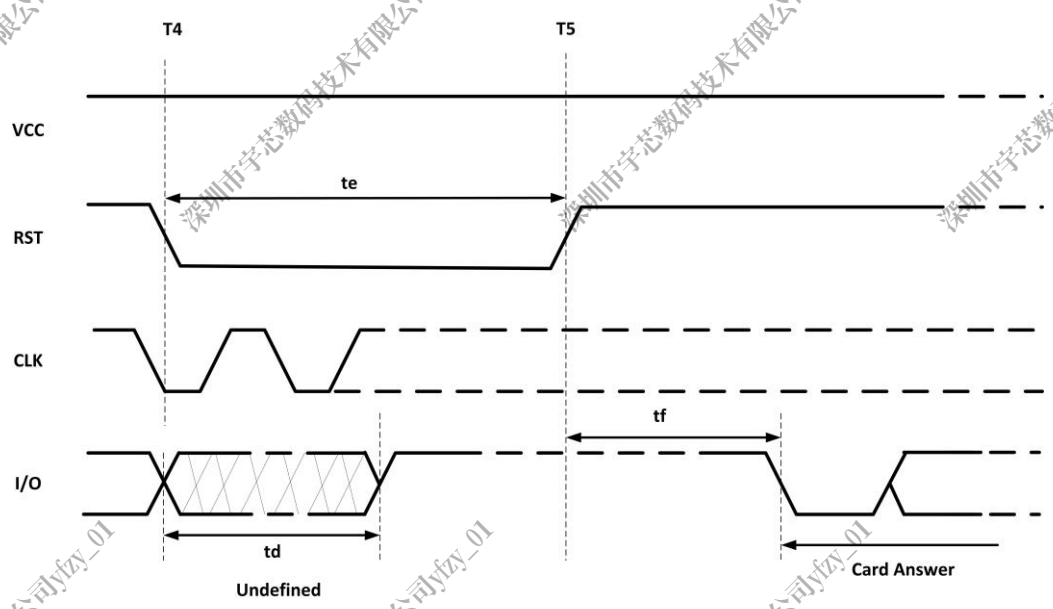


Figure 5-55. SCR Warm Reset Timing

Table 5-45. SCR Timing Constants

Symbol	Min	Typ	Max	Unit
ta	-	-	200/f	us
tb	400/f	-	-	us
tc	400/f	-	40000/f	us
td	-	-	200/f	us
te	400/f	-	-	us
tf	400/f	-	40000/f	us

(1) Activation: Before time T1
(2) Cold Reset: After time T1
(3) T1: The clock signal is applied to CLK at time T1.
(4) T2: The RST is putted to state H.
(5) T3: The card begin answer at time T3.
(6) ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).
(7) tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).
(8) tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).
(9) td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
(10) te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11) tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12) f is the frequency of clock.

5.11.10. I2S/PCM AC Electrical Characteristics

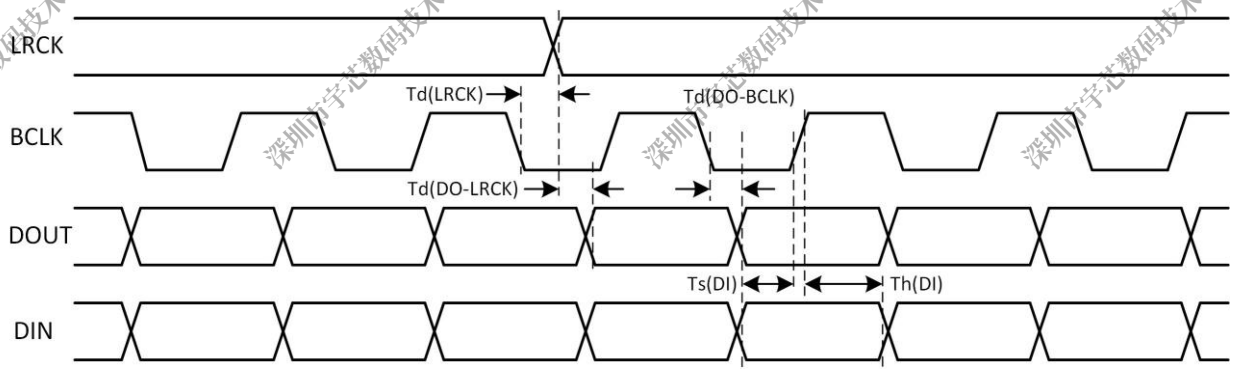


Figure 5-56. I2S/PCM Timing in Master Mode

Table 5-46. I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

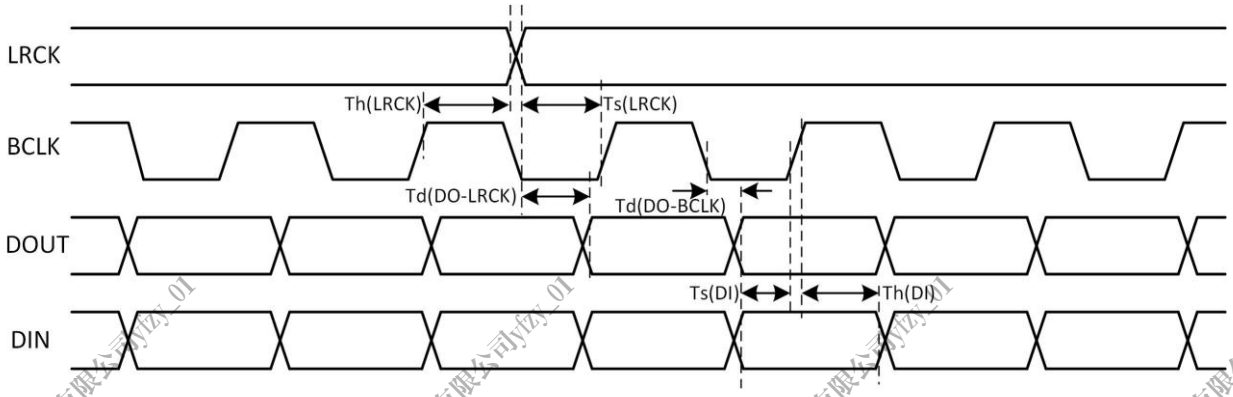


Figure 5-57. I2S/PCM Timing in Slave Mode

Table 5-47. I2S/PCM Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay(For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.11.11. DMIC AC Electrical Characteristics

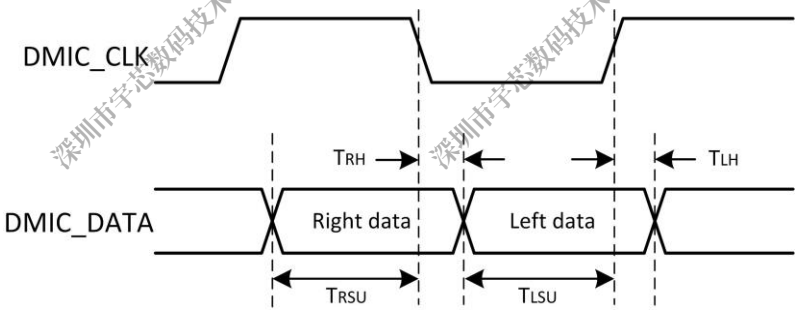


Figure 5-58. DMIC Timing

Table 5-48. DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) setup time to falling edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) hold time from falling edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) setup time to rising edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) hold time from rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

5.11.12. OWA AC Electrical Characteristics

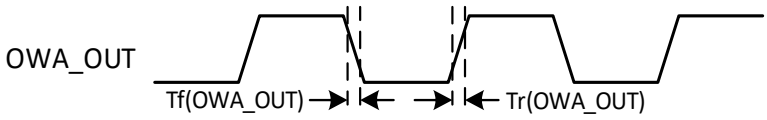


Figure 5-59. OWA Timing

Table 5-49. OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT rise time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT fall time	Tf(OWA_OUT)	-	-	8	ns

5.12. Power-On and Power-Off Sequence

5.12.1. Power-On Sequence

Figure 5-60 shows an example of the power on sequence for the T507/T507-H device. The description of the power on sequence is as follows.

- The consequent steps in power on sequence should not start before the previous step supplies have been stabilized within 90~110% of their nominal voltage, unless stated otherwise.
- Before the RESET pin holds on low, the power requirements of the T507/T507-H show at the following table. After all of the preceding powers have stabilized, the RESET can be released.

Power	Voltage	Sequencing Order	Note
VCC_RTC	1.8V	1	
VDD_SYS	0.9V	2	
VDD_CPU	0.9V	3	
AVCC, VCC_PLL, VCC_DCXO	1.8V	3	They are tied to the same power supply.
VDD18_DRAM	1.8V	3	
VPP_DRAM (DDR4 device power)	2.5V	3	VPP_DRAM starts ramping prior to VCC_DRAM.

Power	Voltage	Sequencing Order	Note
VCC_DRAM	1.1V, 1.2V, 1.5V	4	
VCC_IO,VCC_PA,VCC_PI,VCC_USB	3.3V	4	They are tied to the same power supply.
VCC_PG, VCC_PC	1.8V, 3.3V	4	They are tied to the same power supply.
RESET	1.8V	5	

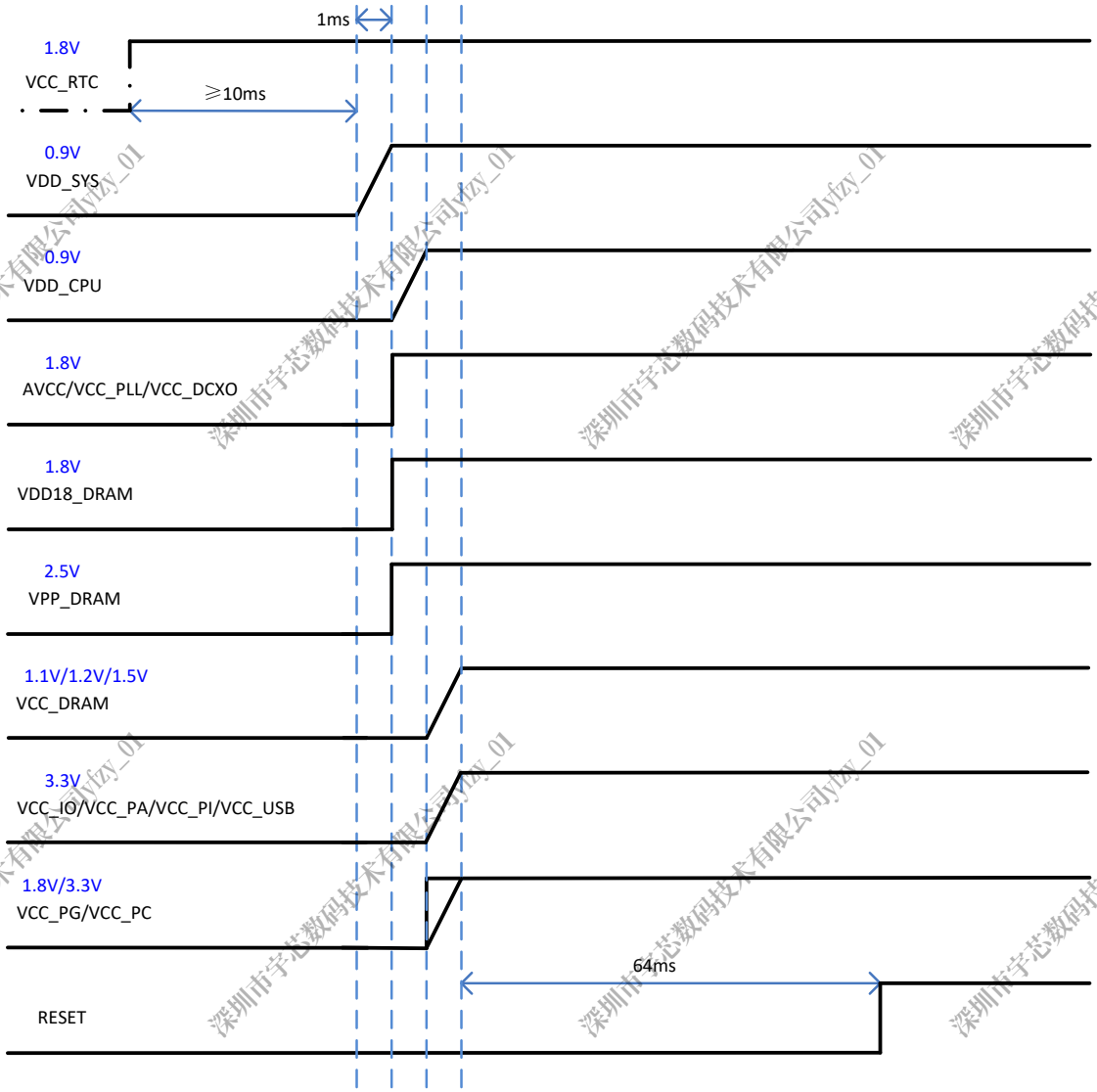


Figure 5-60. Power On Timing

5.12.2. Power-Off Sequence

No special restrictions.

6. Package Thermal Characteristics

Table 6-1 shows thermal resistance parameters of the T507/T507-H. The following thermal resistance characteristics in Table 6-1 is based on JEDEC JESD51 standard, because the actual system design and temperature could be different with JEDEC JESD51, the simulating result data is a reference only, please prevail in the actual application condition test.

Table 6-1. T507/T507-H Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	26	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	10.34	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	10.14	-	°C/W

7. Pin Assignment

7.1. Pin Map

For T507/T507-H, TFBGA 421 balls, 15 mm x 15 mm, 0.65 mm pitch package is offered. Figure 7-1 and Figure 7-2 illustrate the pin maps for T507 package and T507-H package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	PE20		PG8		PG6		PG1		PH10		PH6		X32KIN		REFCLK_OUT	PA4		PD9	PD7	GND	GND	A
B	GND	PE11	PE21	PG17	PG12	PG9	PG7	PG5	PG2	PG0	PH8	PH2	PH3	PH5	X32KOUT	DXIN	DXOUT	PA5	PA10	PD8	PD6	PD4	GND	B
C	PE9	PE10	PE0	GND	PG13	PG14	PG10	PG4	PG3	GND	PH9	TEST	RESET	PH0	PH1	GND	PH4	GND	PA8	PA9	PD5	PD3	PD2	C
D	PE7	PE6	PE8	PE19	PE3	PE2	PG18		PG11	FEL		NMI		DXLDO_OUT	VVREQIN		PA3	PA1	PA0	PA6	PD1	PD0		D
E		PE4	PE5	PE18	PE17	PE1	PG19		PG16	JTAG_SEL		PH7		VCC_DCXO	PL0		PA11	PA2	GND	PA7	PD19	PD18	PD17	E
F	PC4	PC3	PC2	PE15	PE16	PE22	VCC_PG		PG15	BOOT_SEL		EXTIRQ		VCC_RTC	PL1		VCC_PA	VCC_LVDS	PD23	PA12	PD16	PD15		F
G		PC8	PC0	PE14	PE13	PE12	GND			GND		VCC_IO		VCC_PLL	RTC_VIO		GND	VCC_PD	PD21	PD26	PD14	PD13	PD12	G
H	PC10	GND	PC9					GND	VDD_GPUFB	VDD_GPU	VDD_GPU	VDD_GPU	VDD_GPU	GND	GND	GND					PD11	PD10		H
J		PC13	PC12	PC11	PC1		VCC_PE	GND	GND	VDD_GPU	VDD_GPU	VDD_GPU	VDD_GPU	GND	VDD_SYS	VDD_SYSFB	NC11		PD24	PD28	GND	NC5	NC4	J
K	PC14	PC15	PC16	PC6	PC5	GND	VCC_PC	VDD_CPU	GND	GND	GND	GND	GND	GND	VDD_SYS	VDD_SYS	VCC18	PD27	PD25	PD20	NC3	NC2		K
L		PI5	PI1					VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	VDD_SYS	VDD_SYS					GND	NC1	NC0	L
M	PI9	PI7	PI3	PI2	GND	PC7	VCC_PI	VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	VDD_SYS	VDD_SYS	VCC_USB2	NC8	NC9	PD22	NC7	NC6		M
N		PI11	GND	PI6	PI0	PI8		VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	GND	GND	VCC_USB	USB_TEST	VCC_MCSI	NC10	USB3_DM	USB3_DP	GND	N
P		PI13	PF5					VDD_CPUFB	VDD_CPU	GND	GND	GND	GND	GND	GND	GND					USB2_DM	USB2_DP		P
R	PF2	PF3	PF4	PI10	PI12	PI4	PI14	GND	GND	GND	VCC_DRAM	VCC_DRAM	VCC_DRAM	GND	GND	GND	AGND	AVCC	VRA2	LINEOUTR	GND	USB1_DM	USB1_DP	R
T		PF0	PF1	PF6	PI15	PI16		GND	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VDD18_DRAM	SZQ	VCC_TV		VRA1	LINEOUTL	USB0_DM	USB0_DP		T
U	SDQ1	SDQ0	GND				GND			GND		GND			GND		GND				MCSI_D3P	MCSI_D3N	GND	U
V		SDQ3	SDQ2	SDQ11	SDQ12	SDQ19	SDQS2P		SDQ22	SDQ21		SA5	SCS0		SA1	SACT		GPADC2	LRADC	NC	MCSI_D2P	MCSI_D2N		V
W	SDQS0P	SDQS0N	GND	SDQ13	SDQ14	SDQM1	SDQS2N		SDQ23	SDQM2		SA6	GND		SA13	GND		NC	NC	REXT	GND	MCSI_CKP	MCSI_CKN	W
Y		SDQ5	SDQ6	SDQS1P	SDQS1N	SDQ15	GND		SDQ20	GND		SA15	SA2			SRST		NC	GND	GPADC1	MCSI_D1P	MCSI_D1N		Y
AA	SDQ4	SDQ7	SDQ10	SDQ18	SDQ26	GND	SDQS3N	SDQ31	SDQM3			GND	SBA1	SBA0	SA3	SA11	SODT0	SA9	SBG0	SA12	GPADC3	MCSI_D0P	MCSI_D0N	AA
AB	GND	SDQM0	SDQ9	SDQ17	SDQ25	SDQ27	SDQS3P	SDQ28	SDQ29	GND	SCKP	SA4	SA16	SCKE0	GND	SA8	SA0	GND	SBG1	SODT1	GPADC0	TV_OUT	GND	AB
AC	GND	GND	SDQ8	SDQ16		SDQ24		SDQ30			SCKN	SA14		SCKE1		SA10		SA7			SCS1	GND	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Figure 7-1. T507 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	PE20		PG8		PG6		PG1		PH10		PH6		X32KIN		REFCLK_OUT	PA4		PD9	PD7	GND	GND	A
B	GND	PE11	PE21	PG17	PG12	PG9	PG7	PG5	PG2	PG0	PH8	PH2	PH3	PH5	X32KOUT	DXIN	DXOUT	PA5	PA10	PD8	PD6	PD4	GND	B
C	PE9	PE10	PE0	GND	PG13	PG14	PG10	PG4	PG3	GND	PH9	TEST	RESET	PH0	PH1	GND	PH4	GND	PA8	PA9	PD5	PD3	PD2	C
D	PE7	PE6	PE8	PE19	PE3	PE2	PG18		PG11	FEL		NMI		DXLDO_OUT	WREQIN		PA3	PA1	PA0	PA6	PD1	PD0		D
E		PE4	PE5	PE18	PE17	PE1	PG19		PG16	JTAG_SEL		PH7		VCC_DCXO	PL0		PA11	PA2	GND	PA7	PD19	PD18	PD17	E
F	PC4	PC3	PC2	PE15	PE16	PE22	VCC_PG		PG15	BOOT_SEL		EXTIRQ		VCC_RTC	PL1		VCC_PA	VCC_LVDS	PD23	PA12	PD16	PD15		F
G		PC8	PC0	PE14	PE13	PE12	GND			GND		VCC_IO		VCC_PLL	RTC_VIO		GND	VCC_PD	PD21	PD26	PD14	PD13	PD12	G
H	PC10	GND	PC9					GND	VDD_GPUFB	VDD_GPU	VDD_GPU	VDD_GPU	VDD_GPU	GND	GND	GND					PD11	PD10		H
J		PC13	PC12	PC11	PC1		VCC_PE	GND	GND	VDD_GPU	VDD_GPU	VDD_GPU	VDD_GPU	GND	VDD_SYS	VDD_SYSFB	HHPD		PD24	PD28	GND	HTX2N	HTX2P	J
K	PC14	PC15	PC16	PC6	PC5	GND	VCC_PC	VDD_CPU	GND	GND	GND	GND	GND	GND	VDD_SYS	VDD_SYS	VCC_HDMI	PD27	PD25	PD20	HTX1N	HTX1P		K
L		PI5	PI1					VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	VDD_SYS	VDD_SYS					GND	HTX0N	HTX0P	L
M	PI9	PI7	PI3	PI2	GND	PC7	VCC_PI	VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	VDD_SYS	VDD_SYS	VCC_USB2	HSCL	HSDA	PD22	HTXCN	HTXCP		M
N		PI11	GND	PI6	PI0	PI8		VDD_CPU	VDD_CPU	GND	GND	GND	GND	GND	GND	GND	VCC_USB	USB_TEST	VCC_MCSI	HCEC	USB3_DM	USB3_DP	GND	N
P		PI13	PF5					VDD_CPUFB	VDD_CPU	GND	GND	GND	GND	GND	GND	GND					USB2_DM	USB2_DP		P
R	PF2	PF3	PF4	PI10	PI12	PI4	PI14	GND	GND	GND	VCC_DRAM	VCC_DRAM	VCC_DRAM	GND	GND	GND	AGND	AVCC	VRA2	LINEOUTR	GND	USB1_DM	USB1_DP	R
T		PF0	PF1	PF6	PI15	PI16		GND	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VCC_DRAM	VDD18_DRAM	SZQ	VCC_TV		VRA1	LINEOUTL	USB0_DM	USB0_DP		T
U	SDQ1	SDQ0	GND				GND			GND		GND			GND		GND				MCSI_D3P	MCSI_D3N	GND	U
V		SDQ3	SDQ2	SDQ11	SDQ12	SDQ19	SDQS2P		SDQ22	SDQ21		SA5	SCS0		SA1	SACT		GPADC2	LRADC	NC	MCSI_D2P	MCSI_D2N		V
W	SDQS0P	SDQS0N	GND	SDQ13	SDQ14	SDQM1	SDQS2N		SDQ23	SDQM2		SA6	GND		SA13	GND		NC	NC	REXT	GND	MCSI_CKP	MCSI_CKN	W
Y		SDQ5	SDQ6	SDQS1P	SDQS1N	SDQ15	GND		SDQ20	GND		SA15	SA2			SRST		NC	GND	GPADC1	MCSI_D1P	MCSI_D1N		Y
AA	SDQ4	SDQ7	SDQ10	SDQ18	SDQ26	GND	SDQS3N	SDQ31	SDQM3			GND	SBA1	SBA0	SA3	SA11	SODT0	SA9	SBG0	SA12	GPADC3	MCSI_D0P	MCSI_D0N	AA
AB	GND	SDQM0	SDQ9	SDQ17	SDQ25	SDQ27	SDQS3P	SDQ28	SDQ29	GND	SCKP	SA4	SA16	SCKE0	GND	SA8	SA0	GND	SBG1	SODT1	GPADC0	TV_OUT	GND	AB
AC	GND	GND	SDQ8	SDQ16		SDQ24		SDQ30			SCKN	SA14		SCKE1		SA10		SA7			SCS1	GND	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

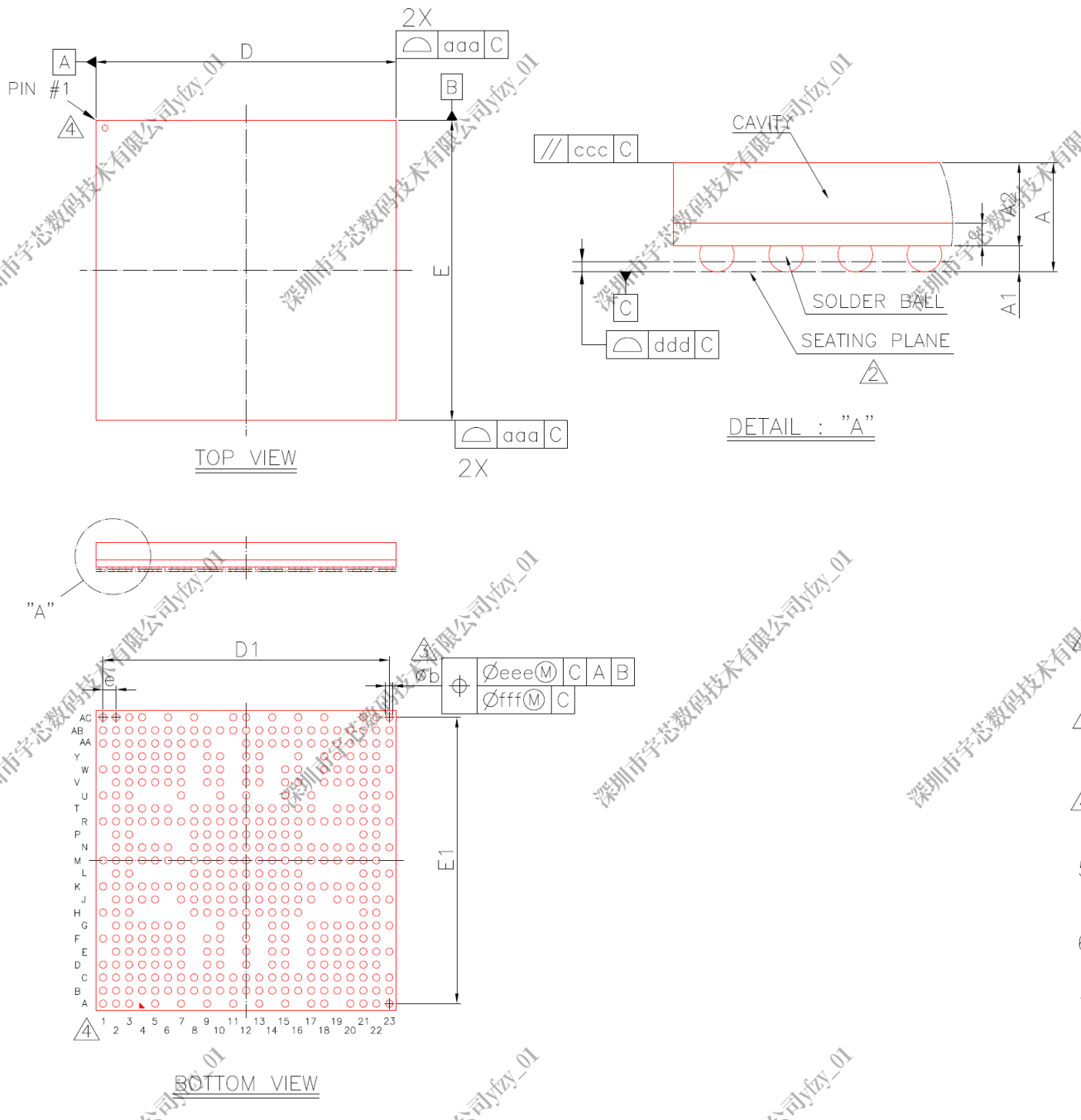
Figure 7-2. T507-H Pin Map

Table 7-1. The Pin Map Difference among T507 and T507-H

Ball Number	T507 Pin	T507-H Pin
L22	NC1	HTX0N
L23	NC0	HTX0P
K21	NC3	HTX1N
K22	NC2	HTX1P
J22	NC5	HTX2N
J23	NC4	HTX2P
M21	NC7	HTXCN
M22	NC6	HTXCP
N20	NC10	HCEC
J17	NC11	HHPD
M18	NC8	HSCL
M19	NC9	HSDA
K17	VCC18	VCC_HDMI

7.2. Package Dimension

Figure 7-4 shows the top, bottom, and side views of T507/T507-H package dimension.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.47	1.54	0.055	0.058	0.061
A1	0.20	0.25	0.30	0.008	0.010	0.012
A2	1.17	1.22	1.27	0.046	0.048	0.050
c	0.32	0.36	0.40	0.013	0.014	0.016
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	14.30	---	---	0.563	---
E1	---	14.30	---	---	0.563	---
e	---	0.65	---	---	0.026	---
b	0.31	0.36	0.41	0.012	0.014	0.016
aaa	0.15			0.006		
ccc	0.15			0.006		
ddd	0.13			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23 / 23					

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd (SPIL STANDARD).
6. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5
7. PKG BALL DIAMETER IS 0.35 mm BEFORE REFLOW.

Figure 7-3. T507/T507-H Package Dimension

8. Carrier, Storage and Baking Information

8.1. Carrier

8.1.1. Matrix Tray Information

Table 8-1 shows the T507/T507-H matrix tray carrier information.

Table 8-1. Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	315 mm x 136 mm x 7.62 mm	126 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12 mm x 180 mm x 85 mm Front-Back:12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

HIC :

Desiccant :

RoHS symbol:

Product label:

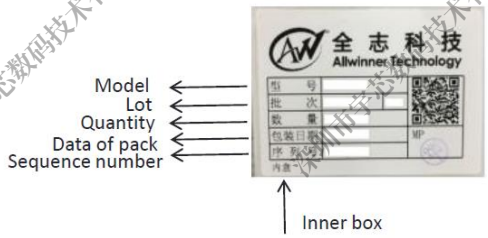
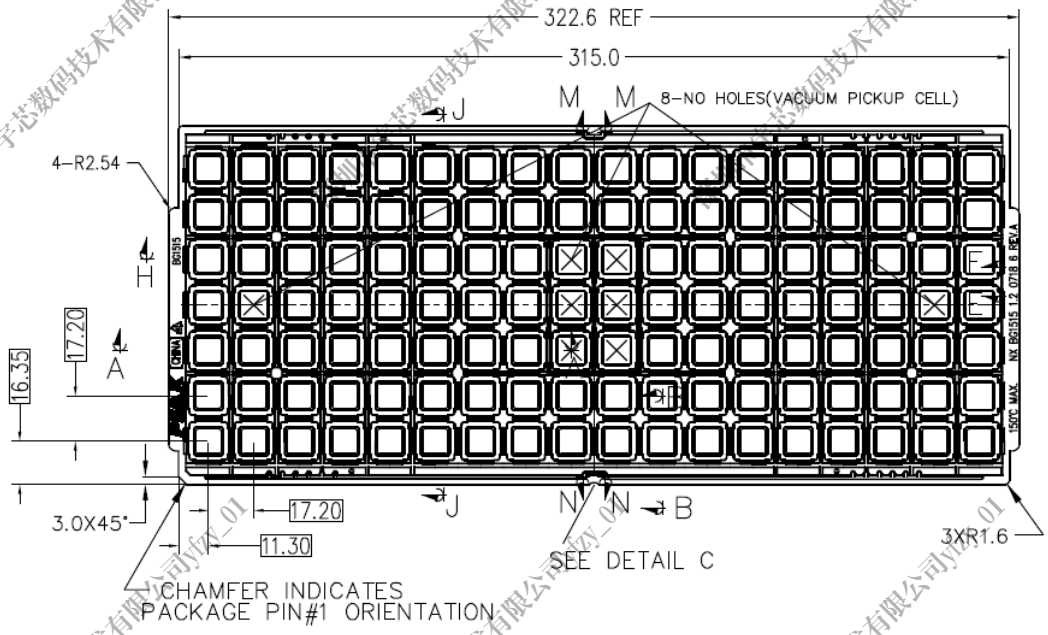


Table 8-2 shows the T507/T507-H packing quantity.

Table 8-2. Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
T507, T507-H,	15x15	126	10	1260	6	7560

Figure 8-1 shows tray dimension drawing of the T507/T507-H.



NOTES :
1. MATERIAL – MPPO.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TOLERANCES – X.X=±0.25
   – X.XX=±0.13
   UNLESS OTHERWISE SPECIFIED.
4. ESD – SURFACE RESISTIVITY
   – 10^5 TO 10^{11} OHMS/SQ.
5. FOR PACKAGE – BG1515
6. PART NO. : NX BG1515 1.2 0718 6 REV.A
   (PLEASE INDICATE ON PURCHASE ORDER).
7. DATECODE AT TRAY BOTTOM SIDE

Figure 8-1. Tray Dimension Drawing

8.2. Storage

Reliability is affected if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

8.2.1. Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL is defined in Table 8-3.

Table 8-3. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The T507/T507-H device samples are classified as MSL3.

8.2.2. Bagged Storage Conditions

The shelf life of the T507/T507-H device samples is defined in Table 8-4.

Table 8-4. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

8.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the T507/T507-H are as follows.

Table 8-5. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

8.3. Baking

It is not necessary to bake the T507/T507-H if the conditions specified in Section 8.2.2 and Section 8.2.3 have not been exceeded. It is necessary to bake the T507/T507-H if any condition specified in Section 8.2.2 and Section 8.2.3 has been exceeded.

It is necessary to bake the T507/T507-H if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the sample baking should not exceed 3 times, and the tray baking should not exceed 1 time, with a distortion risk.

9. Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with Allwinner FAE.

The appropriate reflow conditions are defined in Figure 9-1 and Table 9-1.

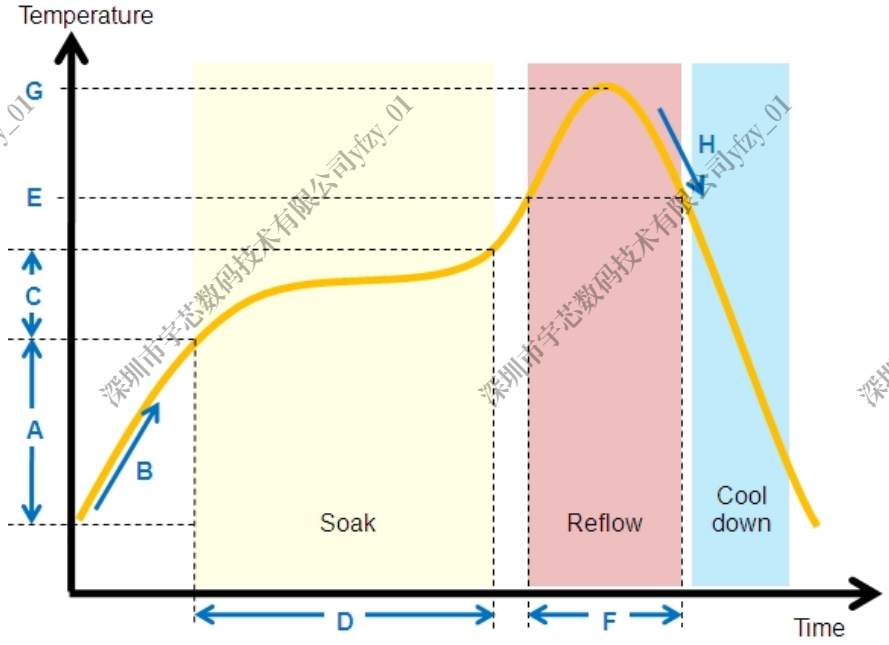


Figure 9-1. Lead-free Reflow Profile

Table 9-1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

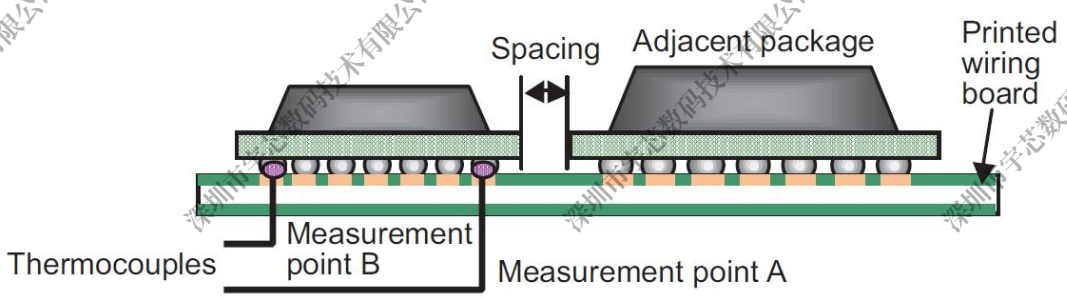


Figure 9-2. Measuring the Reflow Soldering Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10. FT and IQC Test

10.1. FT Test

FT test includes two parts, module verification and linux system testing. For module verification, it verifies the logic function of each module; for linux system testing, it mainly tests CPU, DDR, memory test and linpack, etc. The linux system testing can cover areas where module verification does not cover, with the goal of increasing coverage as much as possible.

10.2. IQC Test

IQC test system is used for sampling inspection before delivery, it is the final test for chip shipment before delivery to the customer. IQC test system includes QA test and QC test.

10.2.1. QA Test

QA test is a testing for each function module of chip based on Android system, which can judge whether chip can reach production standard by system total running results, single module testing fluency.

10.2.2. QC Test

QC test is used to test each module code booting from Nand flash, and run schedule by using PC control code, then read the return value of each module testing. If the return value is PASS, then continue to perform the next module testing; or else stop testing and remind the testing module FAIL.

11. Part Marking

Figure 11-1 shows the T507 marking.

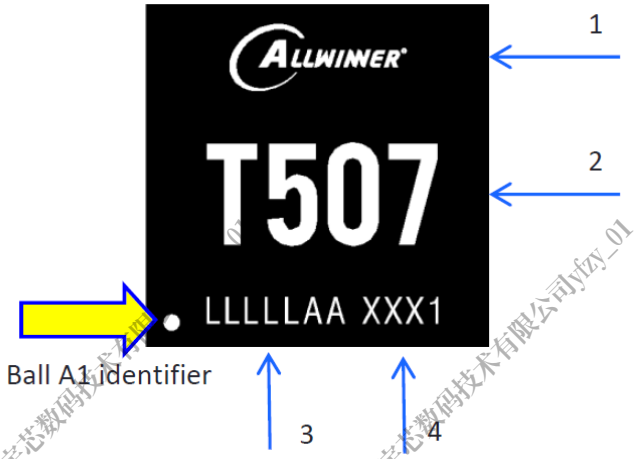


Figure 11-1. T507 Marking

Table 11-1 describes the T507 marking definitions.

Table 11-1. T507 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T507	Module number	Fixed
3	LLLLLAA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

Figure 11-2 shows the T507-H marking.

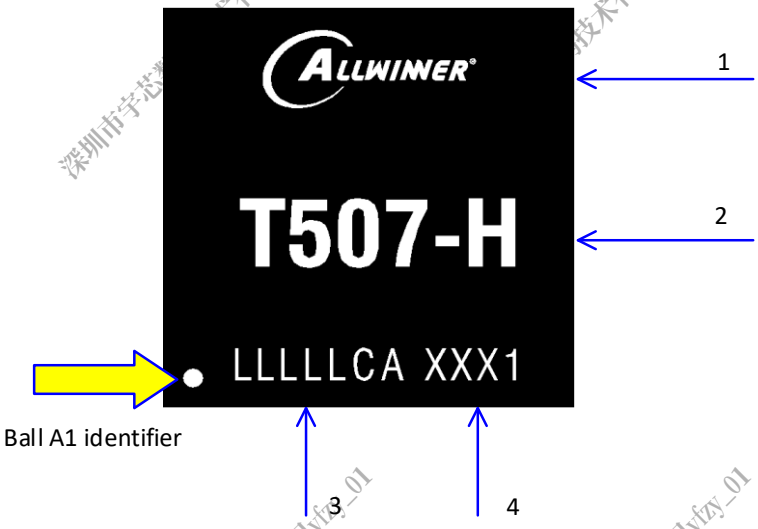


Figure 11-2. T507-H Marking

Table 11-2 describes the T507-H marking definitions.

Table 11-2. T507-H Marking Definitions

No.	Markingss	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T507-H	Module number	Fixed
3	LLLLLCA	Lot number	Dynamic
4	XXX1	Date code	Dynamic

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