

Features

- N-Channel, 5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- Fast Switching
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

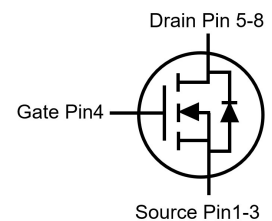
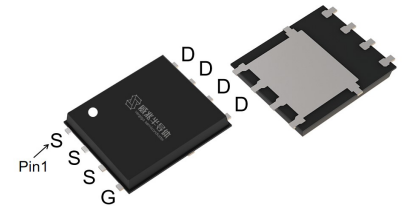


Halogen-Free

Part ID	Package Type	Marking	Packing
VS3698AP	PDFN5x6	3698AP	3000pcs/Reel

V_{DS}	30	V
$R_{DS(on),TYP}@ V_{GS}=10\text{ V}$	3.1	mΩ
$R_{DS(on),TYP}@ V_{GS}=4.5\text{ V}$	4.5	mΩ
I_D	105	A

PDFN5x6



Absolute aximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		30	V
I_S	Diode continuous forward current	$T_C=25\text{ °C}$	105	A
I_D	Continuous drain current@ $V_{GS}=10\text{ V}$	$T_C=25\text{ °C}$	105	A
		$T_C=100\text{ °C}$	68	A
I_{DM}	Pulse drain current tested ①	$T_C=25\text{ °C}$	320	A
P_D	Maximum power dissipation	$T_C=25\text{ °C}$	69	W
V_{GS}	Gate-Source voltage		±20	V
$T_{STG} T_J$	Storage and operating temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	40	°C/W

Drain-Source Avalanche Ratings

EAS	Avalanche Energy, Single Pulsed ②	256	mJ
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Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(	$V_{DS}=30V, V_{GS}=0V$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_j=125^{\circ}\text{C}$)	$V_{DS}=30V, V_{GS}=0V$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.8	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance③	$V_{GS}=10V, I_D=20A$	--	3.1	4.5	m Ω
$R_{DS(ON)}$	Drain-Source On-State Resistance③	$V_{GS}=4.5V, I_D=15A$	--	4.5	6.0	m Ω
Dynamic Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $f=1\text{MHz}$	--	2530	--	pF
C_{oss}	Output Capacitance		--	380	--	pF
C_{rss}	Reverse Transfer Capacitance		--	295	--	pF
R_g	Gate Resistance	$f=1\text{MHz}$		0.95		Ω
$Q_g(10V)$	Total Gate Charge	$V_{DS}=15V, I_D=20A,$ $V_{GS}=10V$	--	54	--	nC
$Q_g(4.5V)$	Total Gate Charge		--	29	--	nC
Q_{gs}	Gate-Source Charge		--	6	--	nC
Q_{gd}	Gate-Drain Charge		--	14	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15V,$ $I_D=10A,$ $R_G=3.5\Omega,$ $V_{GS}=10V$	--	8	--	ns
t_r	Turn-on Rise Time		--	5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	27	--	ns
t_f	Turn-Off Fall Time		--	11	--	ns
Source- Drain Diode Characteristics@ $T_j=25^{\circ}\text{C}$ (unless otherwise stated)						
V_{SD}	Forward on voltage	$I_{SD}=20A, V_{GS}=0V$	--	0.81	1.2	V
t_{rr}	Reverse Recovery Time	$T_j=25^{\circ}\text{C}, I_{sd}=20A,$ $di/dt=500A/\mu s$	--	43	--	ns
Q_{rr}	Reverse Recovery Charge		--	37	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 32A$, $V_{GS} = 10V$. Part not recommended for use above this value
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

Typical Characteristics

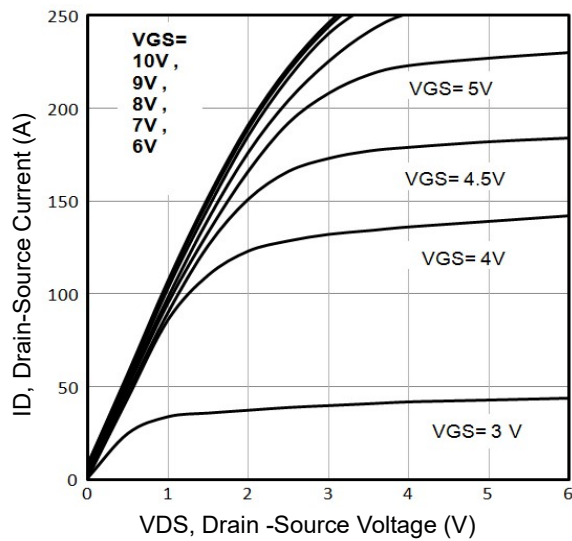


Fig1. Typical Output Characteristics

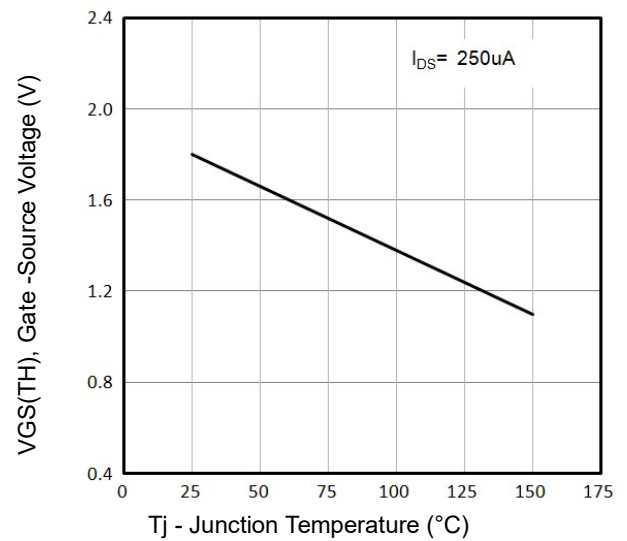


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

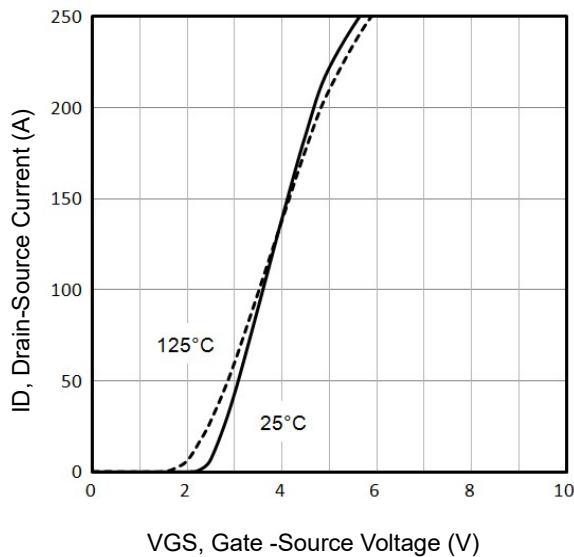


Fig3. Typical Transfer Characteristics

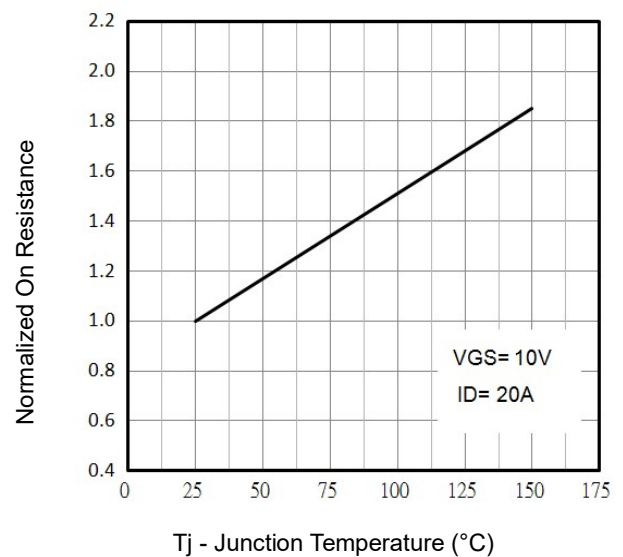


Fig4. Normalized On-Resistance Vs. T_j

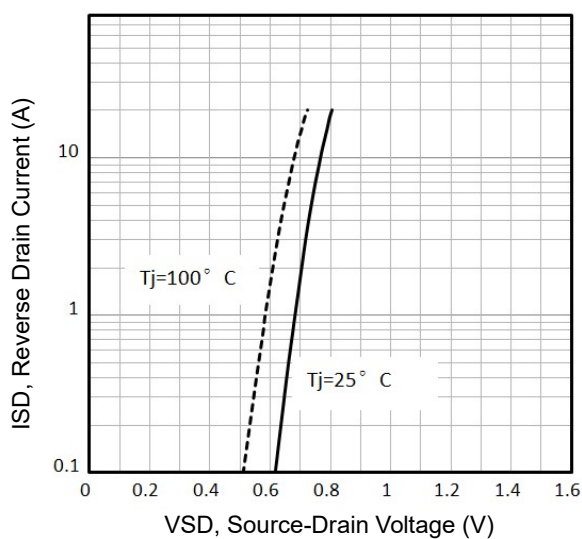


Fig5. Typical Source-Drain Diode Forward Voltage

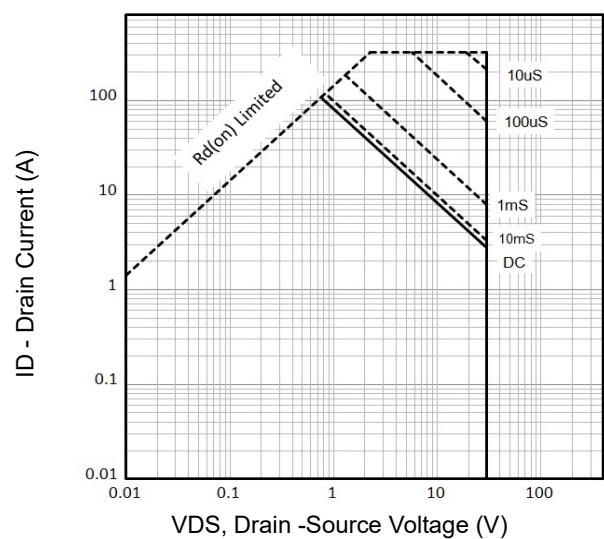


Fig6. Maximum Safe Operating Area

Typical Characteristics

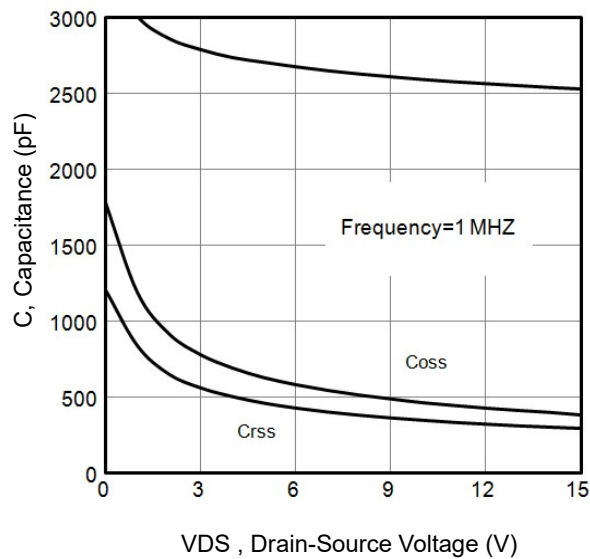


Fig7. Typical Capacitance Vs.Drain-Source Voltage

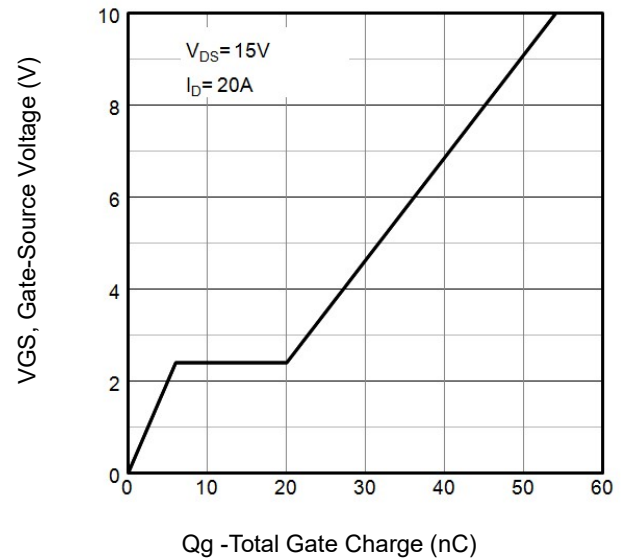


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

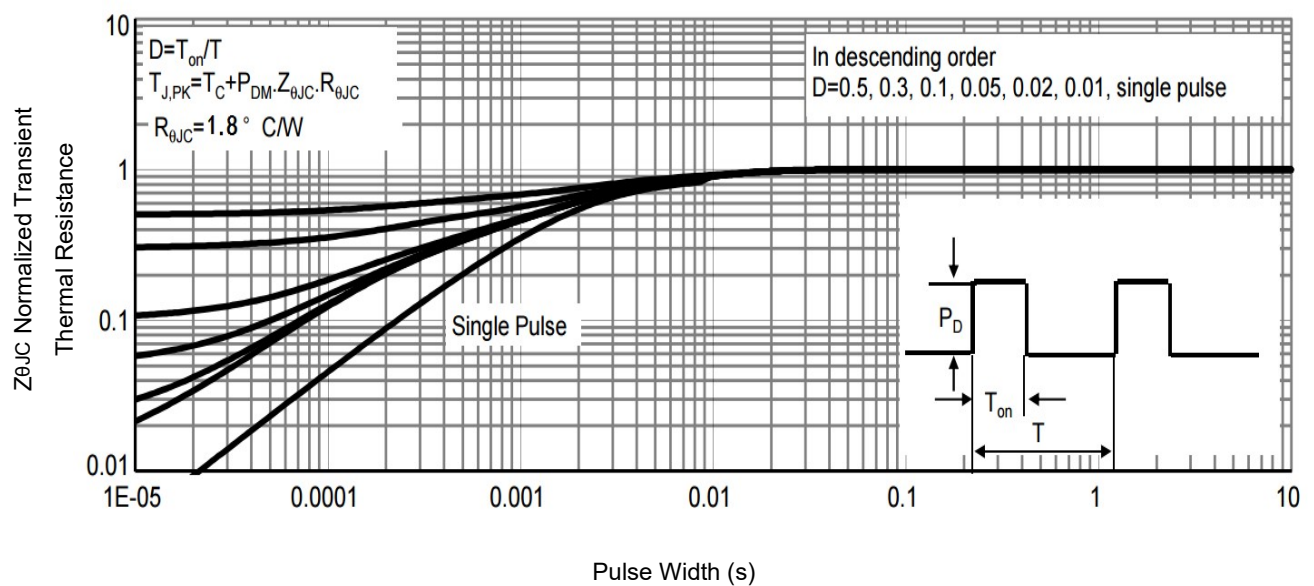


Fig9 . Normalized Maximum Transient Thermal Impedance

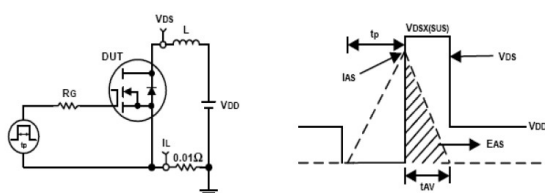


Fig10. Unclamped Inductive Test Circuit and waveforms

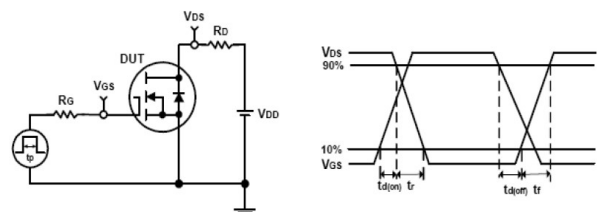
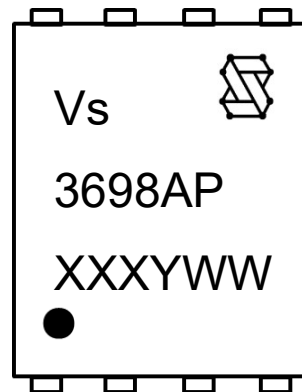


Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (3698AP)

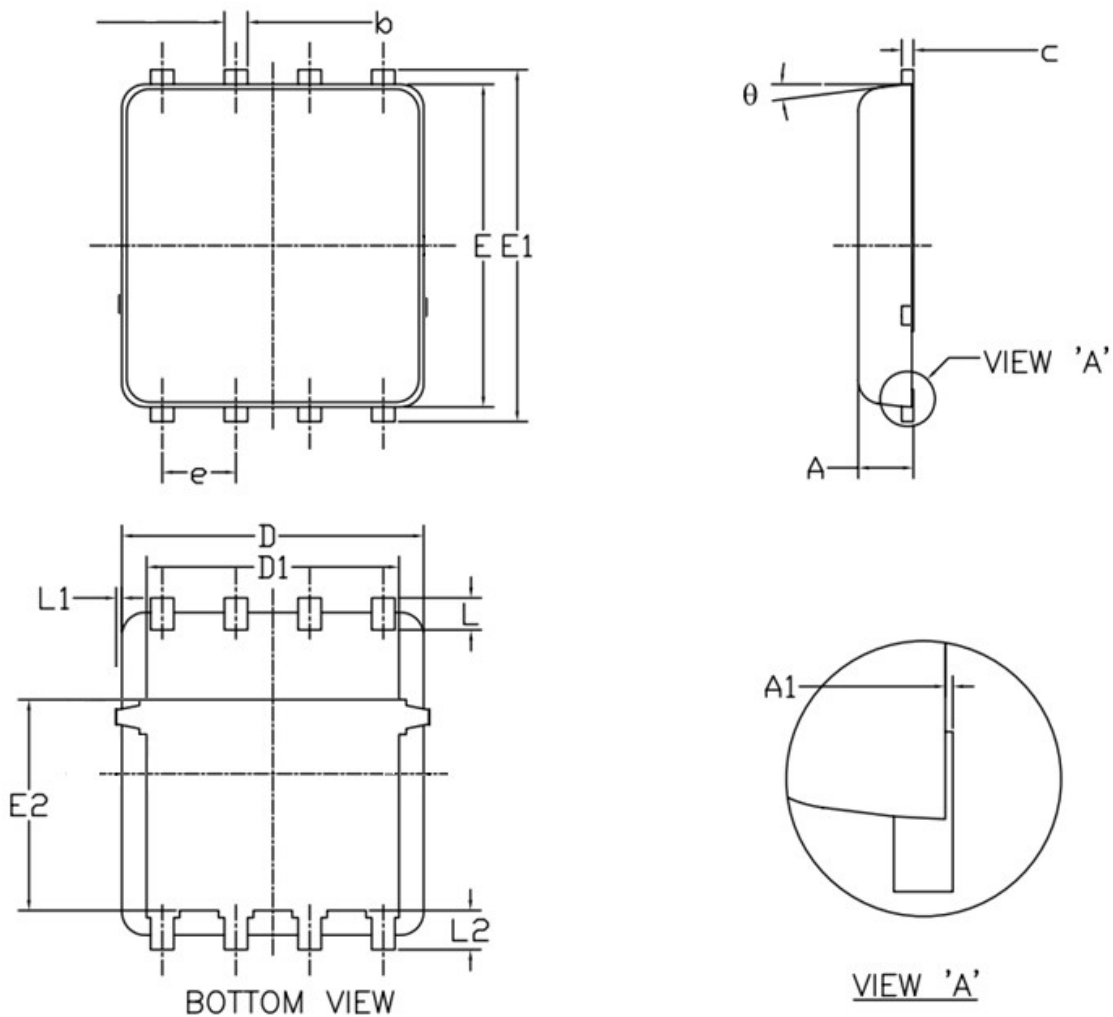
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service
Sales and Service:
sales@vgsemi.com
Vergiga Semiconductor CO., LTD
TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: www.vgsemi.com