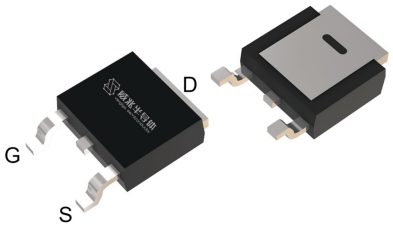
## Features

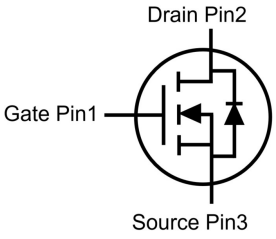
- N-Channel，5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}$=4.5 V
- Fast Switching
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

| | | |
|---|---|---|
| $V_{DS}$ | 30 | V |
| $R_{DS(on),TYP}$@ $V_{GS}$=10 V | 3.1 | mΩ |
| $R_{DS(on),TYP}$@ $V_{GS}$=4.5 V | 4.5 | mΩ |
| $I_D$ | 105 | A |

Pb-Free RoHS HF Halogen-Free

TO-252




| Part ID | Package Type | Marking | Packing |
|---|---|---|---|
| VS3698AD | TO-252 | 3698AD | 2500pcs/Reel |

## Maximum ratings, at $T_j$=25 °C, unless otherwise specified

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source breakdown voltage | | 30 | V |
| $I_S$ | Diode continuous forward current | $T_C$=25°C | 105 | A |
| $I_D$ | Continuous drain current@VGS=10V | $T_C$=25°C | 105 | A |
| | | $T_C$=100°C | 68 | A |
| $I_{DM}$ | Pulse drain current tested ① | $T_C$=25°C | 320 | A |
| $P_D$ | Maximum power dissipation | $T_C$=25°C | 83 | W |
| VGS | Gate-Source voltage | | ±20 | V |
| $T_{STG}$ $T_J$ | Storage and operating temperature range | | -55 to 175 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance-Junction to Case | 1.8 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient | 40 | °C/W |
| **Drain-Source Avalanche Ratings** | | | |
| EAS | Avalanche Energy, Single Pulsed ② | 256 | mJ |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics @ $T_j$= 25°C (unless otherwise stated)** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V $I_D$=250μA | 30 | -- | -- | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V,$V_{GS}$=0V | -- | -- | 1 | μA |
| | Zero Gate Voltage Drain Current($T_j$=125℃) | $V_{DS}$=30V,$V_{GS}$=0V | -- | -- | 100 | μA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$=±20V,$V_{DS}$=0V | -- | -- | ±100 | nA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$,$I_D$=250μA | 1.0 | 1.8 | 2.5 | V |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance③ | $V_{GS}$=10V, $I_D$=20A | -- | 3.1 | 4.5 | mΩ |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance③ | $V_{GS}$=4.5V, $I_D$=15A | -- | 4.5 | 6.0 | mΩ |
| **Dynamic Electrical Characteristics @ $T_j$= 25°C (unless otherwise stated)** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=15V,$V_{GS}$=0V, f=1MHz | -- | 2530 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 380 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 295 | -- | pF |
| $R_g$ | Gate Resistance | f=1MHz | | 0.95 | | Ω |
| $Q_g$ | Total Gate Charge | $V_{DS}$=15V,$I_D$=20A, $V_{GS}$=10V | -- | 54 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 6 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 14 | -- | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$=15V, $I_D$=10A, $R_G$=3.5Ω, $V_{GS}$=10V | -- | 8 | -- | ns |
| $t_r$ | Turn-on Rise Time | | -- | 5 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 27 | -- | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 11 | -- | ns |
| **Source- Drain Diode Characteristics@ $T_j$= 25°C (unless otherwise stated)** | | | | | | |
| $V_{SD}$ | Forward on voltage | $I_{SD}$=20A,$V_{GS}$=0V | -- | 0.81 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $T_j$=25℃,$I_{sd}$=20A, di/dt=500A/μs | -- | 43 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 37 | -- | nC |

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.5mH,$R_G$ = 25Ω, $I_{AS}$ = 32A, $V_{GS}$ =10V. Part not recommended for use above this value

③ Pulse width ≤ 300μs; duty cycle≤ 2%.

## Typical Characteristics

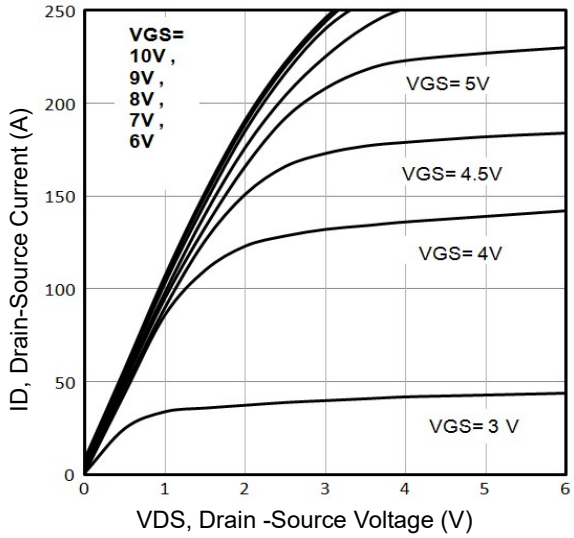



**Fig1.** Typical Output Characteristics

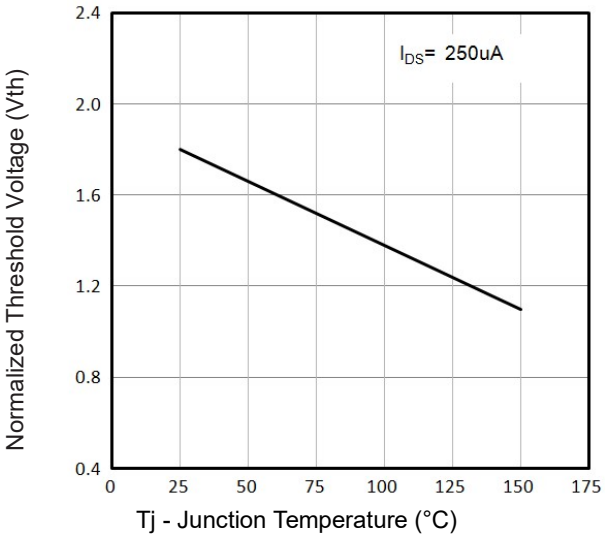



**Fig2.** $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

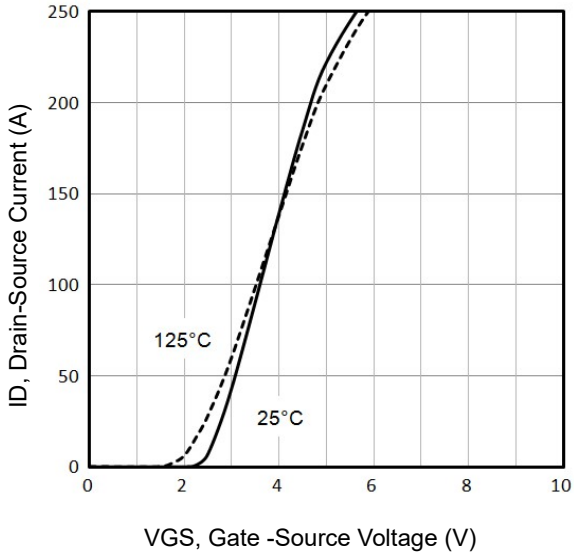



**Fig3.** Typical Transfer Characteristics

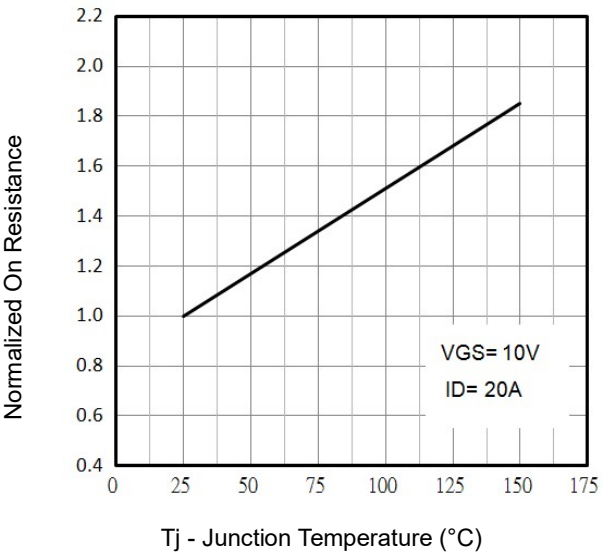



**Fig4.** Normalized On-Resistance Vs. Tj

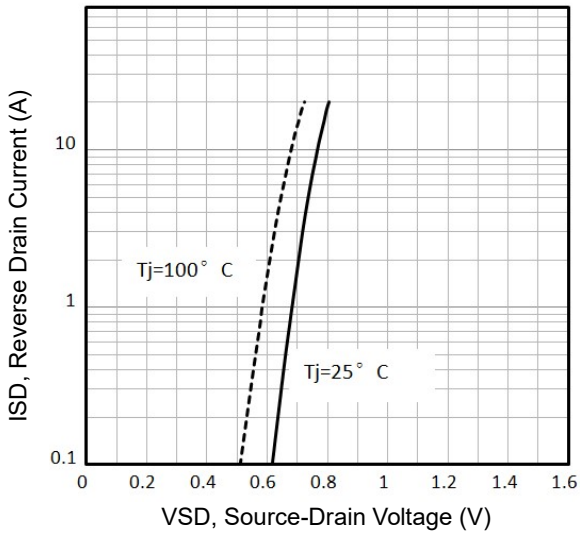



**Fig5.** Typical Source-Drain Diode Forward Voltage

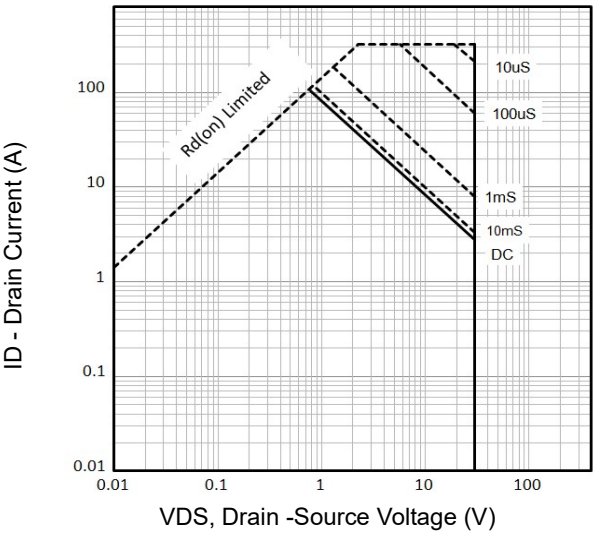



**Fig6.** Maximum Safe Operating Area

## Typical Characteristics

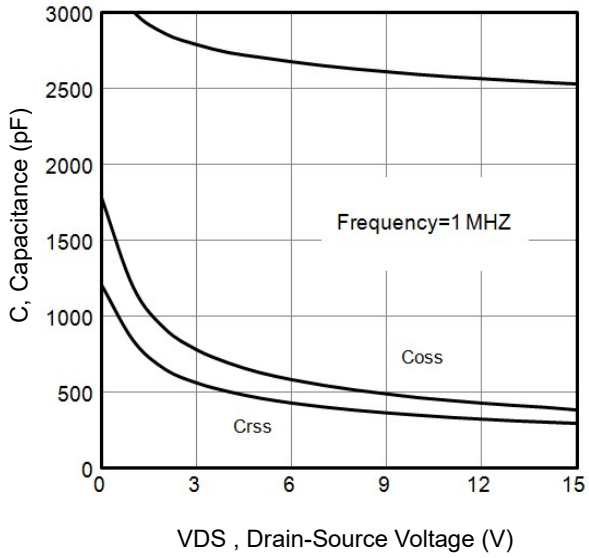



**Fig7.** Typical Capacitance Vs.Drain-Source Voltage

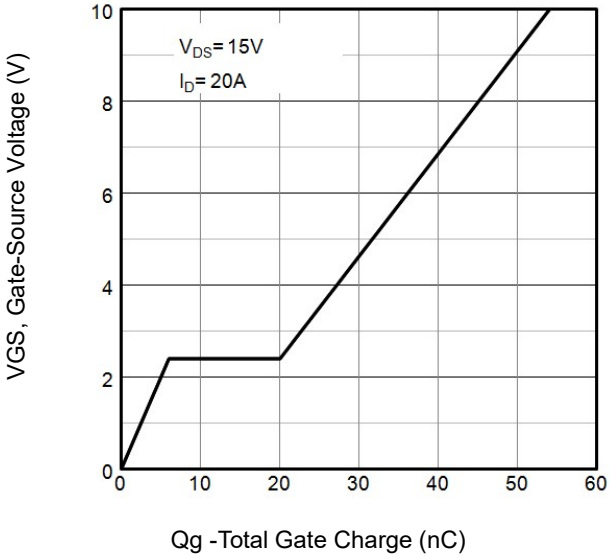



**Fig8.** Typical Gate Charge Vs.Gate-Source Voltage

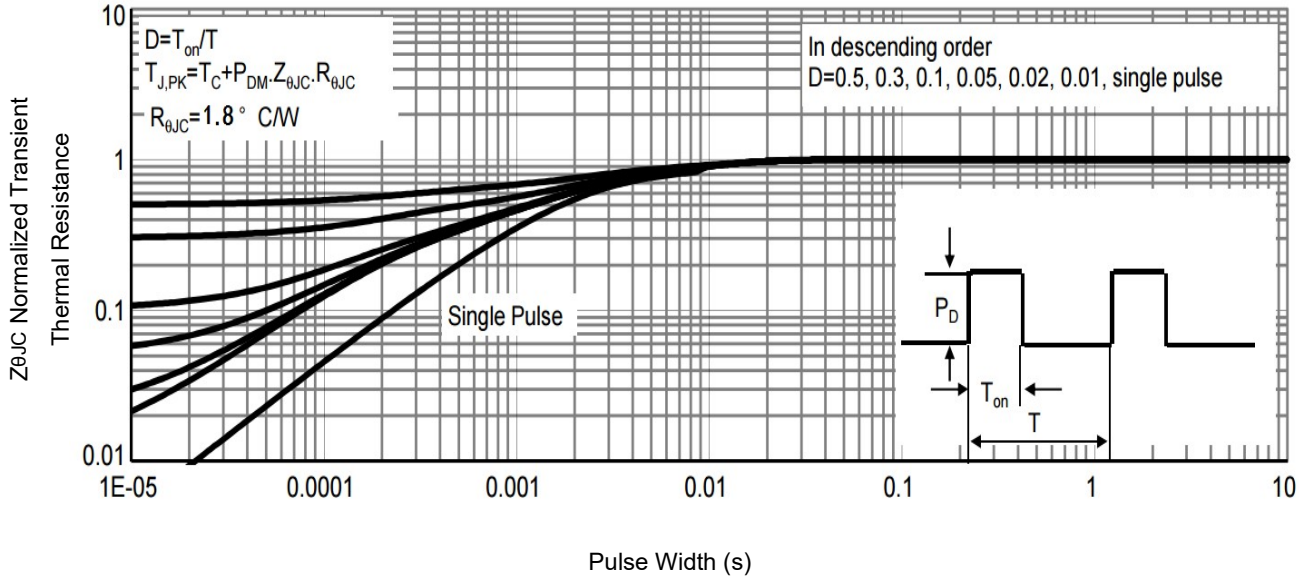



**Fig9 .** Normalized Maximum Transient Thermal Impedance

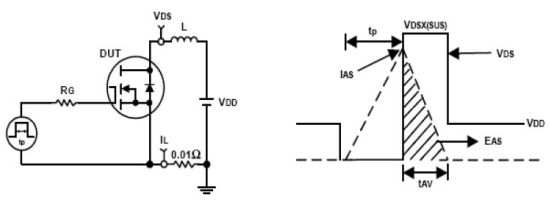



**Fig10.** Unclamped Inductive Test Circuit and waveforms

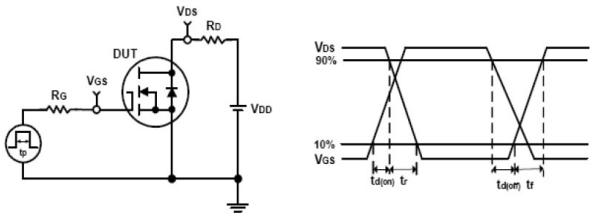
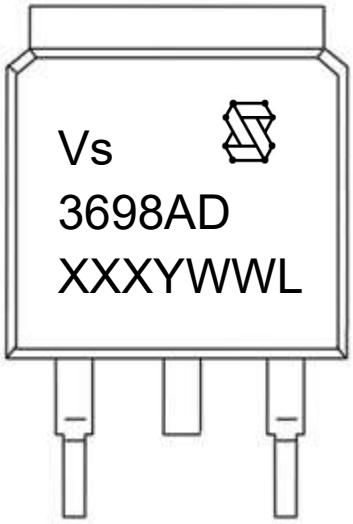



**Fig11.** Switching Time Test Circuit and waveforms

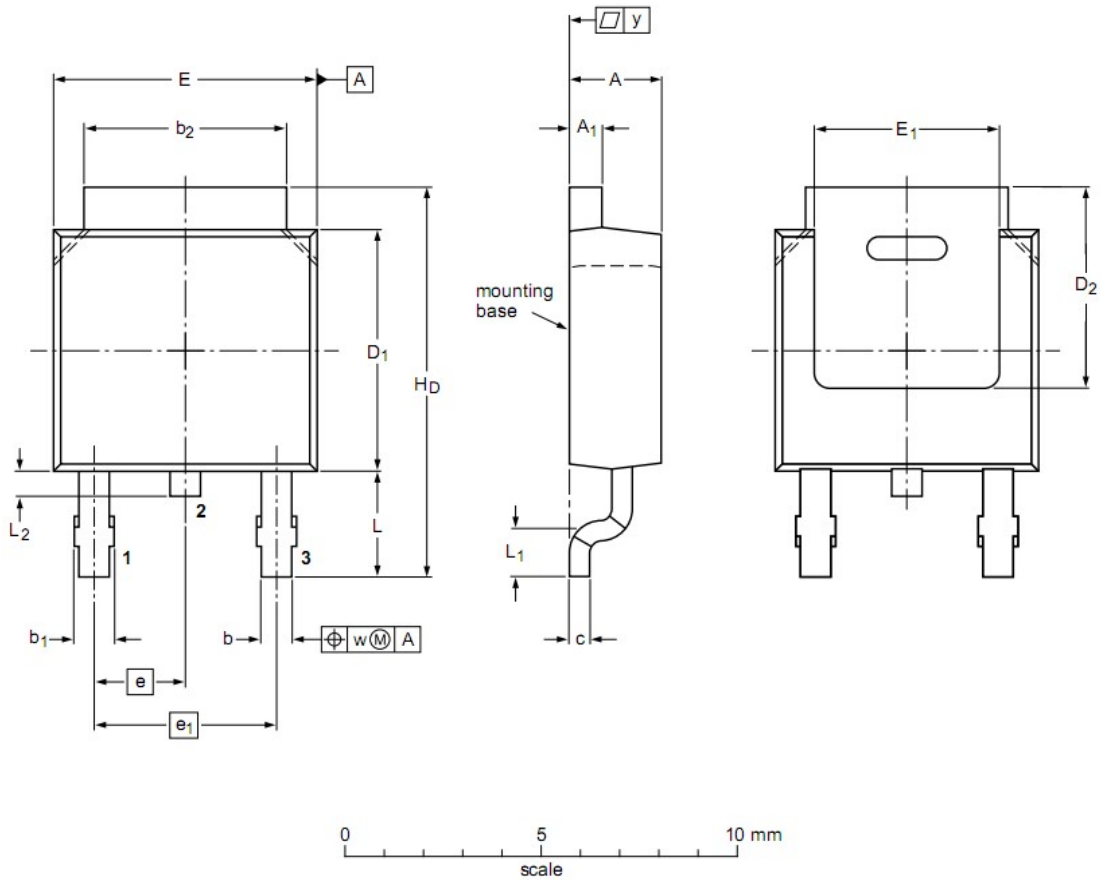
## Marking Information




1st line: Vergiga Code（Vs）， Vergiga Logo
2nd line: Part Number（3698AD）
3rd line: Date code （XXXYWWL）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code , refer to table below
WW: Week Code (01 to 53)

| Code | C | D | E | F | G | H | J | K | L | M | N | P | Q | R | S | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Year | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2030 |

## TO-252 Package Outline Data




| Symbol | Dimensions (unit: mm) | | |
|---|---|---|---|
| | Min | Typ | Max |
| **A** | 2.20 | 2.30 | 2.38 |
| **$A_1$** | 0.46 | 0.50 | 0.63 |
| **b** | 0.64 | 0.76 | 0.89 |
| **$b_1$** | 0.77 | 0.85 | 1.14 |
| **$b_2$** | 5.00 | 5.33 | 5.46 |
| **c** | 0.458 | 0.508 | 0.558 |
| **$D_1$** | 5.98 | 6.10 | 6.223 |
| **$D_2$** | 5.21 | -- | -- |
| **E** | 6.40 | 6.60 | 6.731 |
| **$E_1$** | 4.40 | -- | -- |
| **e** | 2.286 BSC | | |
| **$e_1$** | -- | 4.57 | -- |
| **$H_D$** | 9.40 | 10.00 | 10.40 |
| **L** | 2.743 REF | | |
| **$L_1$** | 1.40 | 1.52 | 1.77 |
| **$L_2$** | 0.50 | 0.80 | 1.01 |
| **w** | -- | 0.20 | -- |
| **y** | -- | -- | 0.20 |

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

## Customer Service

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