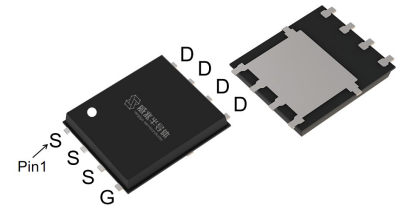


Features

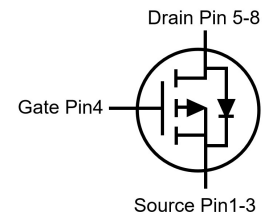
- P-Channel, -5V Logic Level Control
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=-4.5V$
- Fast Switching
- Enhancement mode
- 100% Avalanche Tested
- Pb-free lead plating; RoHS compliant

V_{DS}	-30	V
$R_{DS(on),TYP@ V_{GS}=-10V}$	10	m Ω
$R_{DS(on),TYP@ V_{GS}=-4.5V}$	17	m Ω
I_D	-45	A

PDFN5x6



Part ID	Package Type	Marking	Packing
VS3510AP	PDFN5x6	3510AP	3000pcs/reel



Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage	-30	V
V_{GS}	Gate-Source voltage	± 25	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	-45 A
I_D	Continuous drain current @ $V_{GS}=-10V$	$T_C = 25^\circ\text{C}$	-45 A
		$T_C = 100^\circ\text{C}$	-29 A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	-180 A
I_{DSM}	Continuous drain current @ $V_{GS}=-10V$	$T_A = 25^\circ\text{C}$	-15 A
		$T_A = 70^\circ\text{C}$	-12 A
E_{AS}	Avalanche energy, single pulsed ②	56	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	37 W
		$T_C = 100^\circ\text{C}$	15 W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	4 W
		$T_A = 70^\circ\text{C}$	2.6 W
$T_{STG,TJ}$	Storage and junction temperature range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	30	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-30	--	--	V
IDSS	Zero Gate Voltage Drain Current(T _J =25°C)	V _{DS} =-30V, V _{GS} =0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T _J =125°C)	V _{DS} =-30V, V _{GS} =0V	--	--	-100	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±25V, V _{DS} =0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.8	-2.4	V
RDS(on)	Drain-Source On-State Resistance ④	V _{GS} =-10V, I _D =-20A	--	10	13	mΩ
RDS(on)	Drain-Source On-State Resistance ④	V _{GS} =-4.5V, I _D =-15A	--	17	22	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
Ciss	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	1700	1870	2000	pF
Coss	Output Capacitance		200	300	380	pF
Crss	Reverse Transfer Capacitance		100	200	260	pF
Rg	Gate Resistance	f=1MHz	--	4.5	--	Ω
Qg	Total Gate Charge	V _{DS} =-15V, I _D =-20A, V _{GS} =-10V	--	39	--	nC
Qgs	Gate-Source Charge		--	7	--	nC
Qgd	Gate-Drain Charge		--	13	--	nC
Switching Characteristics						
Td(on)	Turn-on Delay Time	V _{DD} =-15V, I _D =-20A, R _G =3Ω, V _{GS} =-10V	--	10.1	--	ns
Tr	Turn-on Rise Time		--	10.6	--	ns
Td(off)	Turn-Off Delay Time		--	31	--	ns
Tf	Turn-Off Fall Time		--	10	--	ns
Source- Drain Diode Characteristics @ T_J = 25°C (unless otherwise stated)						
VSD	Forward on voltage	I _{SD} =-20A, V _{GS} =0V	--	-0.9	-1.2	V
Trr	Reverse Recovery Time	I _{sd} =-20A, V _{GS} =0V di/dt=-500A/μs	--	16	--	ns
Qrr	Reverse Recovery Charge		--	42	--	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = -15A, V_{GS} = -10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Characteristics

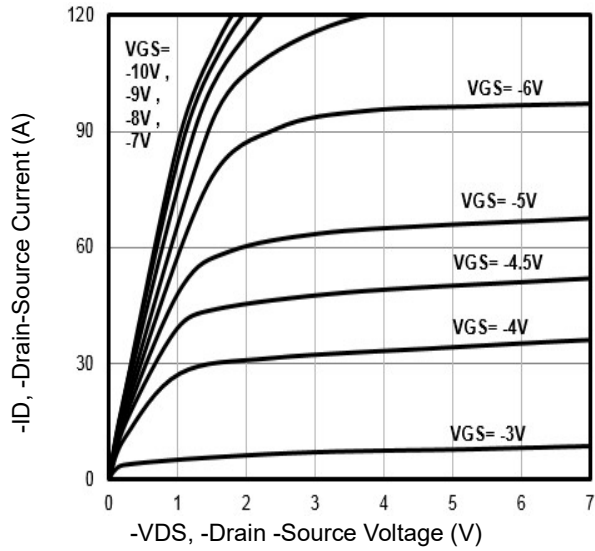


Fig1. Typical Output Characteristics

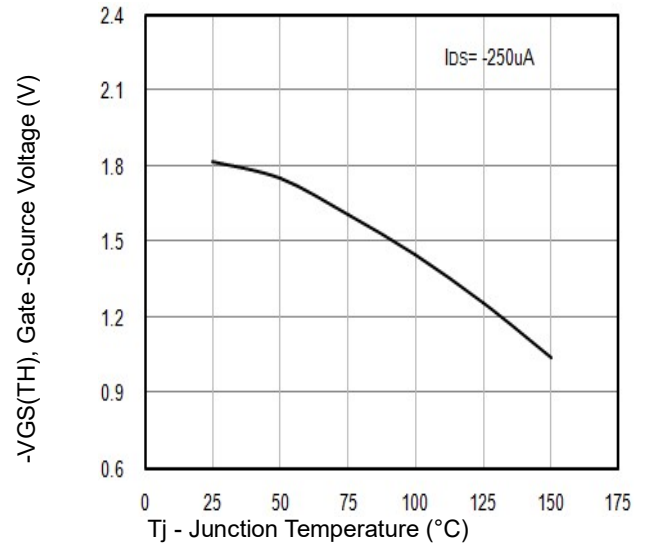


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

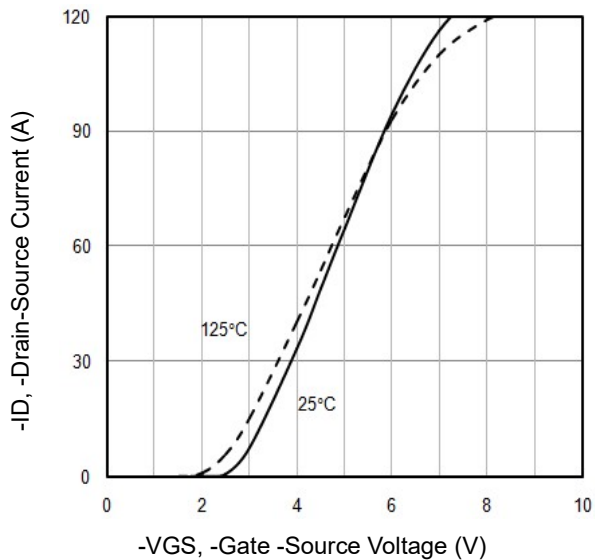


Fig3. Typical Transfer Characteristics

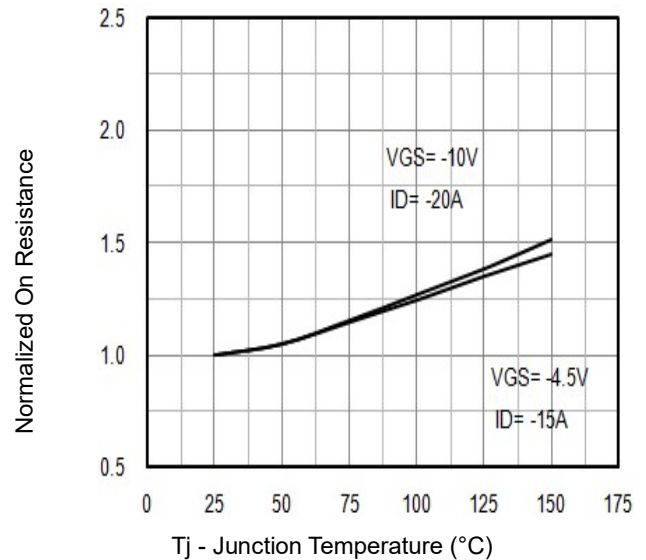


Fig4. Normalized On-Resistance Vs. T_j

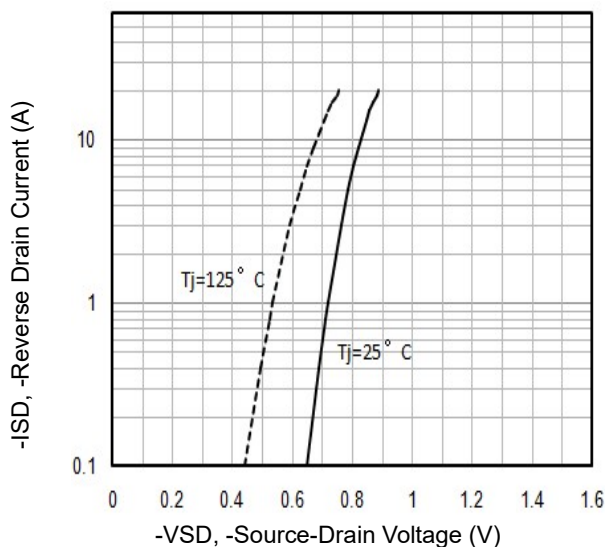


Fig5. Typical Source-Drain Diode Forward Voltage

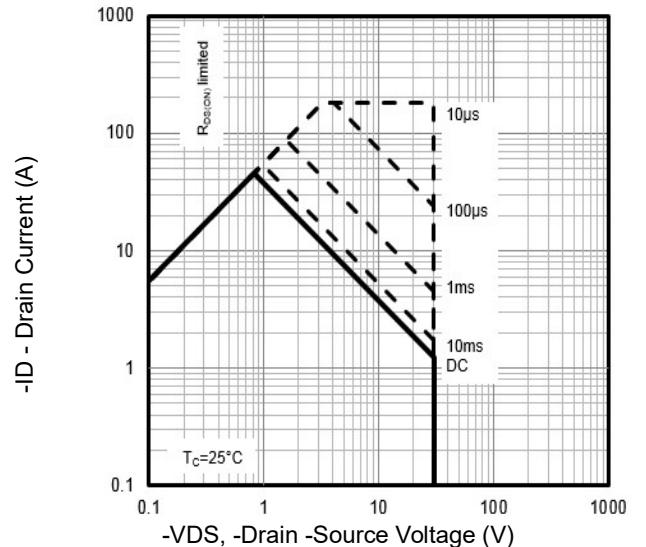


Fig6. Maximum Safe Operating Area

Typical Characteristics

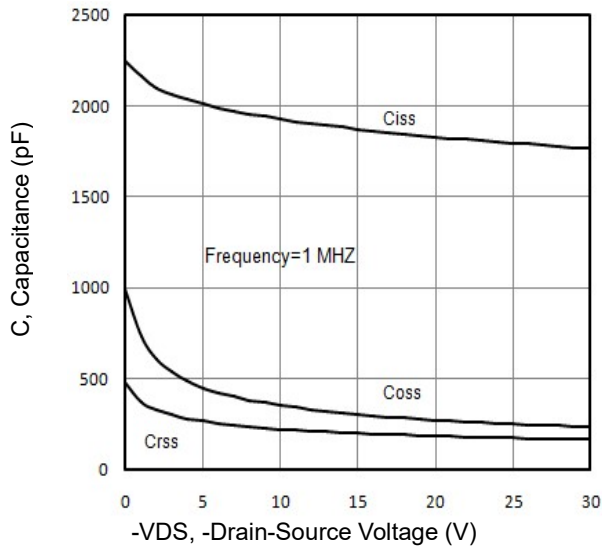


Fig7. Typical Capacitance Vs. Drain-Source Voltage

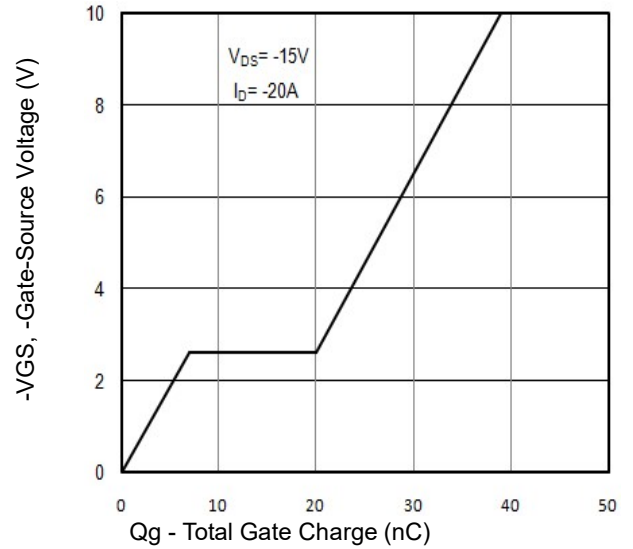


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

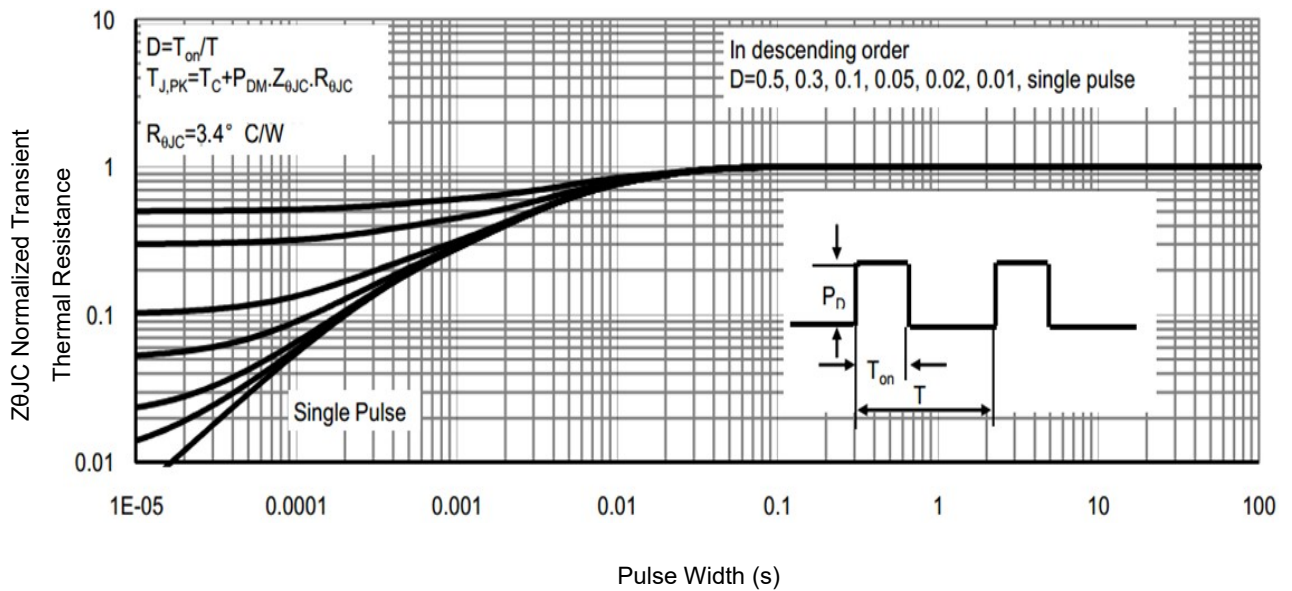


Fig9. Normalized Maximum Transient Thermal Impedance

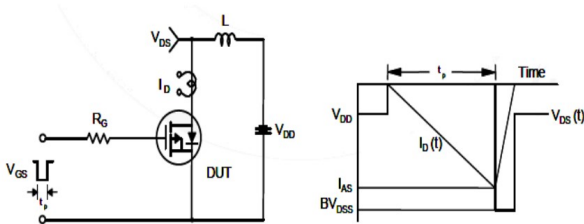


Fig10. Unclamped Inductive Test Circuit and Waveforms

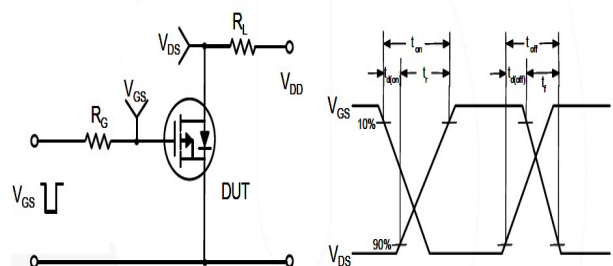
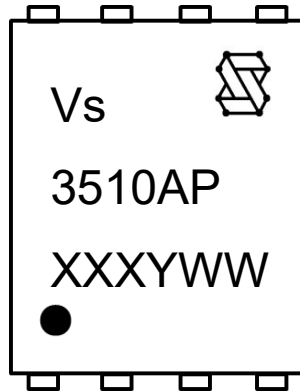


Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (3510AP)

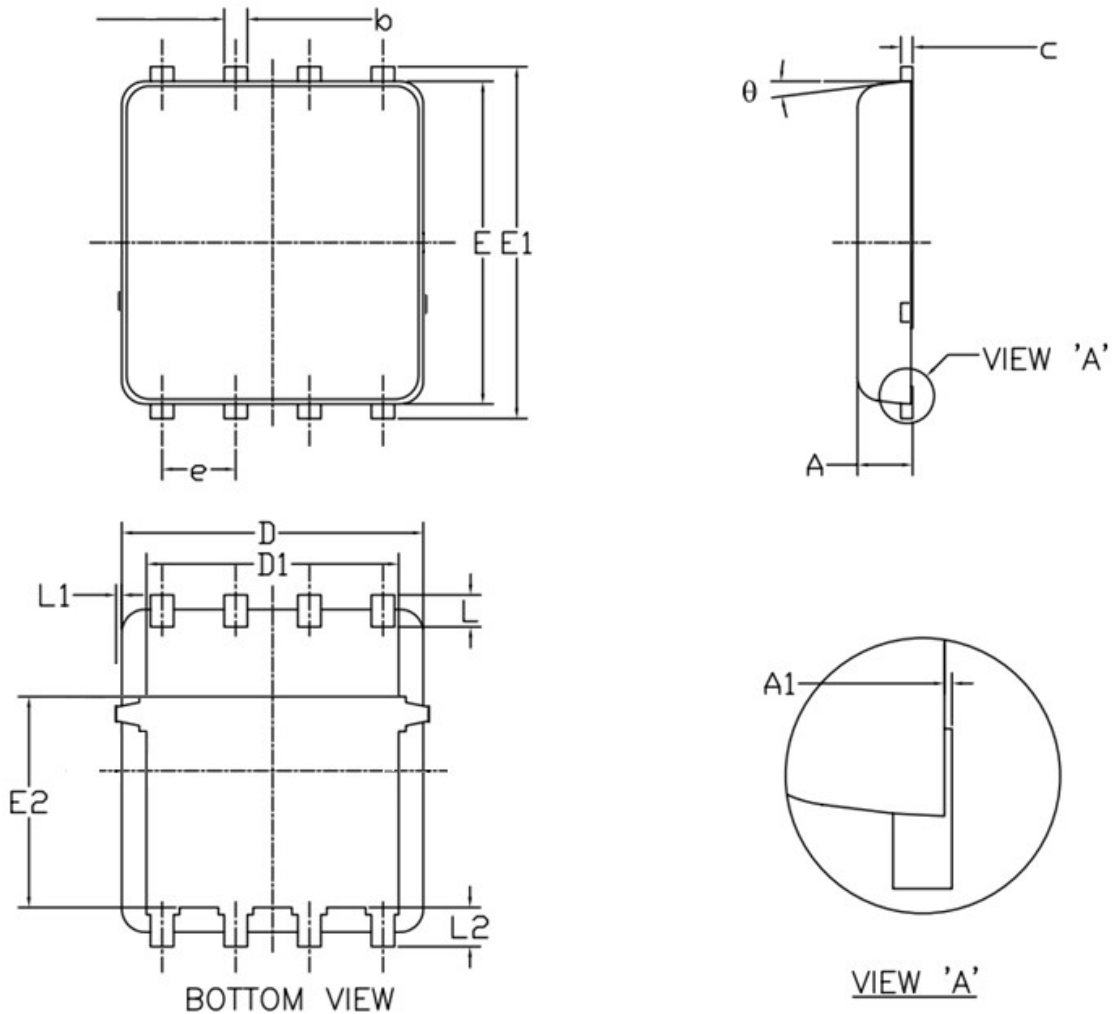
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code, code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

PDFN5x6 Type M Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

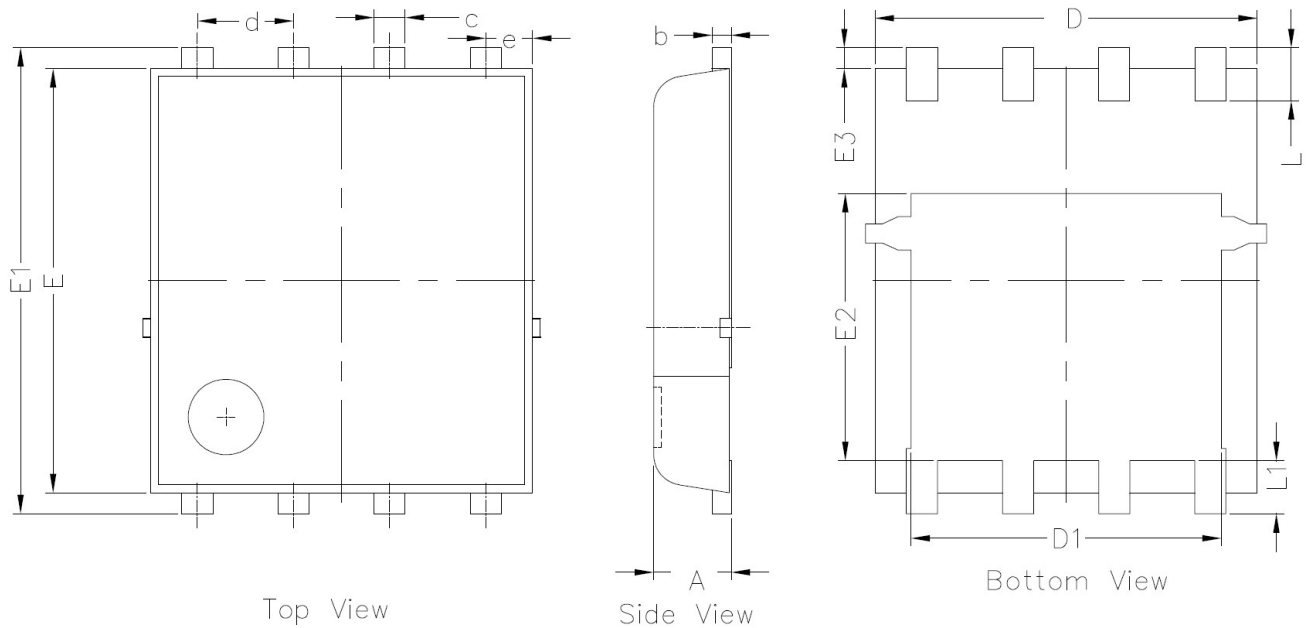
Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

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Vergiga Semiconductor CO., LTD
TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: www.vergiga.com

PDFN5x6 Type JJ Package Outline Data


Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.900	1.000	1.100
b	0.246	0.254	0.312
c	0.310	0.410	0.510
d	1.27 BSC		
D	4.950	5.050	5.150
D1	4.000	4.100	4.200
E	5.500	5.600	5.700
E1	6.050	6.150	6.250
E2	3.425	3.525	3.625
E3	0.175	0.275	0.375
L	0.500	0.600	0.700
L1	0.600	0.700	0.800

Notes:

- 1.Refer to JEDEC MO-240 variation AA.
- 2.Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
- 3.Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

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