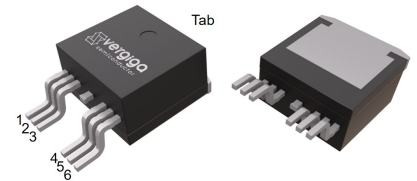


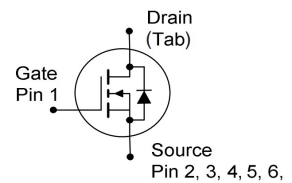
Features

- Enhancement mode
- Very low on-resistance
- Fast Switching and High efficiency
- 100% Avalanche Tested

V_{DS}	40	V
$R_{DS(on),TYP@ V_{GS}=10V}$	1.1	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	1.5	mΩ
$I_D(\text{Package Limited})$	175	A


TO-263-6L


Part ID	Package Type	Marking	Packing
VS4603DM6	TO-263-6L	4603DM	800pcs/Reel



Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		40	V
V_{GS}	Gate-Source voltage		± 20	V
I_S	Diode continuous forward current (Wire bond limited)	$T_C = 25^\circ\text{C}$	175	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 25^\circ\text{C}$	175	A
I_D	Continuous drain current @ $V_{GS}=10V$ (Wire bond limited)	$T_C = 100^\circ\text{C}$	175	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	1100	A
I_{DSM}	Continuous drain current @ $V_{GS}=10V$	$T_A = 25^\circ\text{C}$	33	A
		$T_A = 70^\circ\text{C}$	26	A
E_{AS}	Avalanche energy, single pulsed ②		506	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	300	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	2	W
T_{STG}, T_J	Storage and Junction Temperature Range		-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	75	$^\circ\text{C/W}$

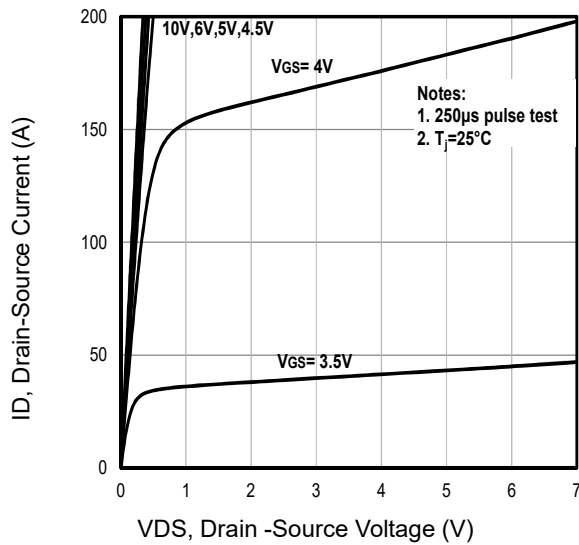
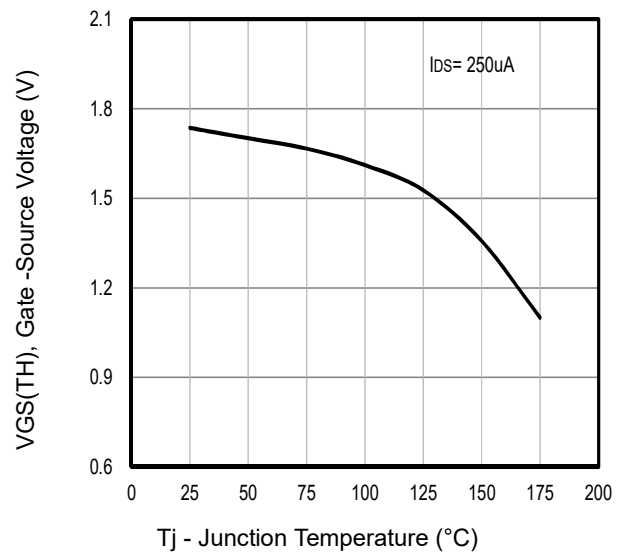
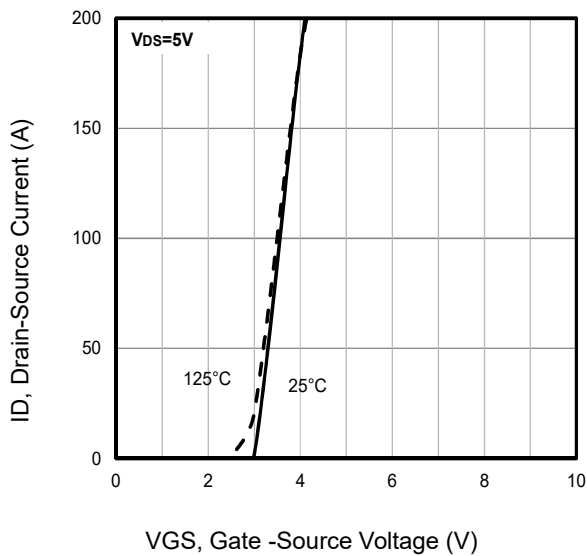
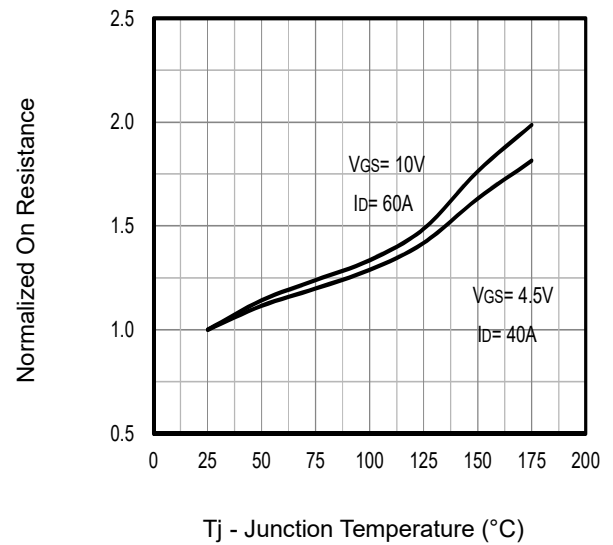
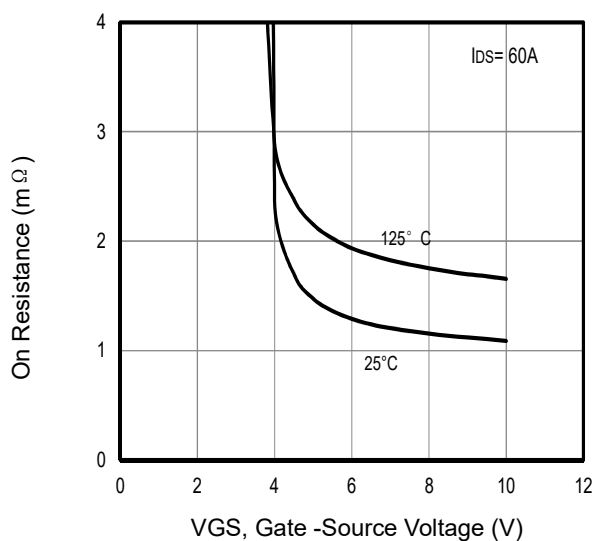
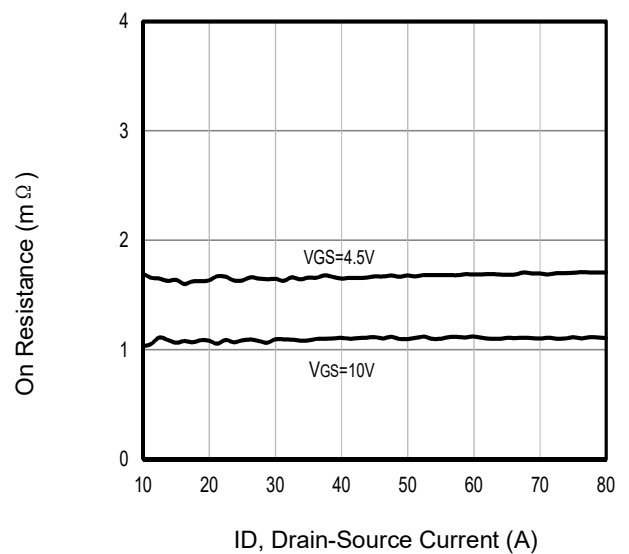
Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =40V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =40V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	1.3	1.8	2.4	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =60A	--	1.1	1.4	mΩ
		(T _j =100°C)	--	1.4	--	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =40A	--	1.5	2	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =20V,V _{GS} =0V, f=1MHz	11410	15210	20230	pF
C _{oss}	Output Capacitance		930	1245	1655	pF
C _{rss}	Reverse Transfer Capacitance		580	770	1025	pF
R _g	Gate Resistance	f=1MHz	0.2	0.5	3	Ω
Q _g (10V)	Total Gate Charge	V _{DS} =20V,I _D =60A, V _{GS} =10V	--	204	271	nC
Q _g (4.5V)	Total Gate Charge		--	97	129	nC
Q _{gs}	Gate-Source Charge		--	45	60	nC
Q _{gd}	Gate-Drain Charge		--	38	57	nC
Switching Characteristics						
T _d (on)	Turn-on Delay Time	V _{DD} =20V, I _D =60A, R _G =3Ω, V _{GS} =10V	--	26	--	ns
T _r	Turn-on Rise Time		--	115	--	ns
T _d (off)	Turn-Off Delay Time		--	102	--	ns
T _f	Turn-Off Fall Time		--	62	--	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =40A,V _{GS} =0V	--	0.8	1.2	V
T _{rr}	Reverse Recovery Time	I _{sd} =60A, V _{GS} =0V	--	31	62	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	28	56	nC

NOTE:

- ① Single pulse; pulse width $\leq 100\mu s$.
- ② Limited by T_{Jmax} , starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 45A$, $V_{GS} = 10V$. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C .
- ④ Pulse width $\leq 380\mu s$; duty cycle $\leq 2\%$.

Typical Characteristics


Fig1. Typical Output Characteristics

Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

Fig3. Typical Transfer Characteristics

Fig4. Normalized On-Resistance Vs. T_j

Fig5. On Resistance Vs Gate-Source Voltage

Fig6. On Resistance Vs Drain Current and Gate Voltage

Typical Characteristics

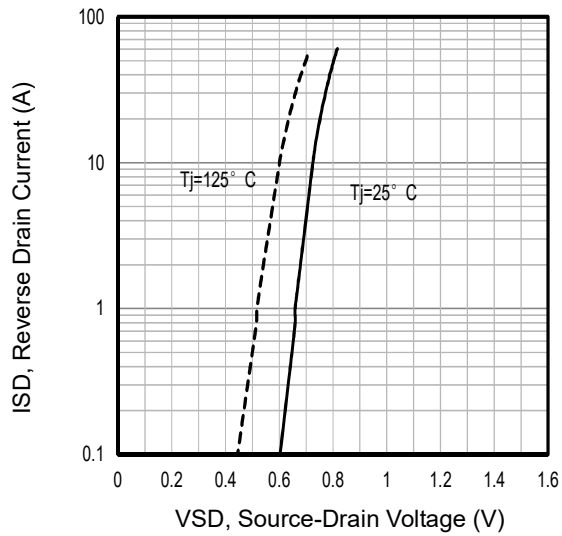


Fig7. Typical Source-Drain Diode Forward Voltage

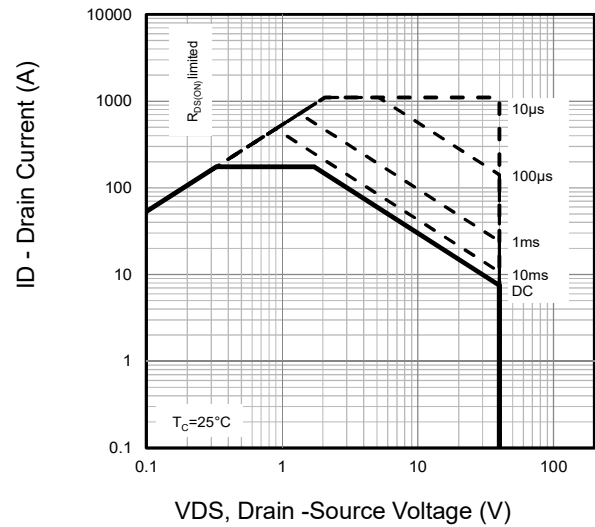


Fig8. Maximum Safe Operating Area

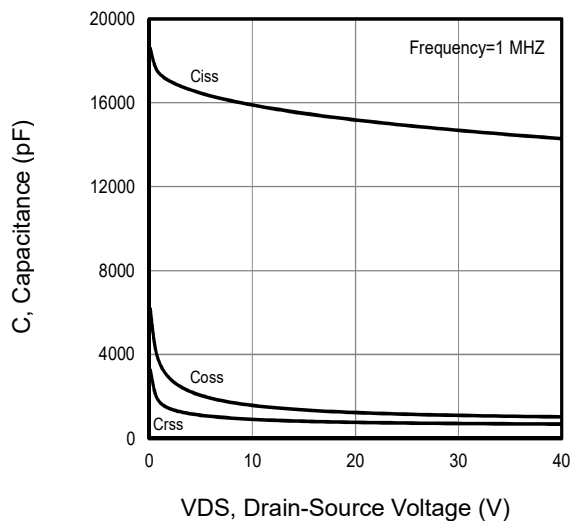


Fig9. Typical Capacitance Vs. Drain-Source Voltage

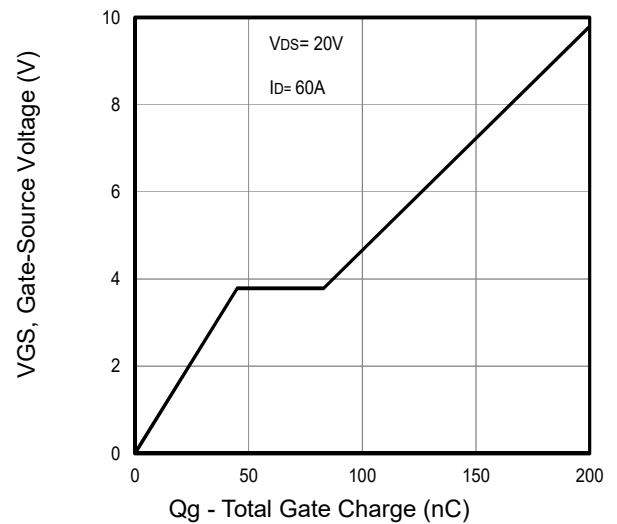


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

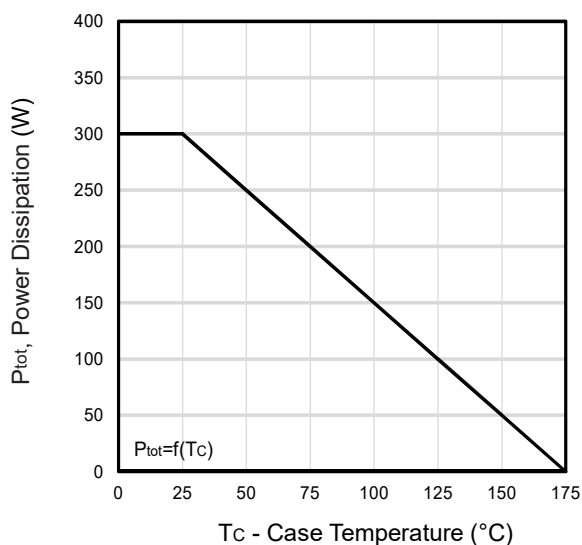


Fig11. Power Dissipation Vs. Case Temperature

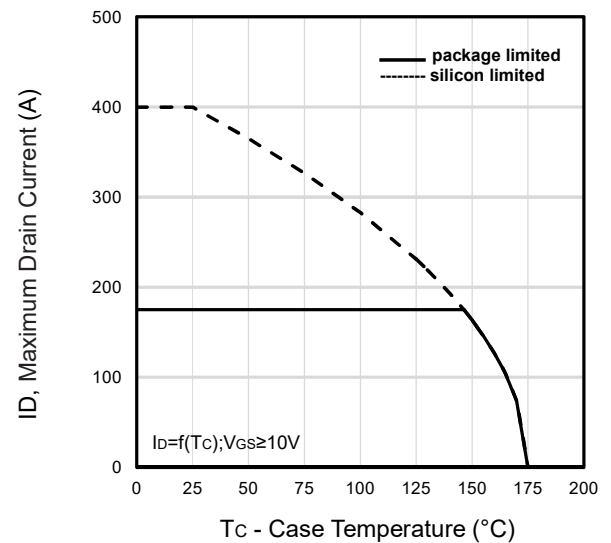


Fig12. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

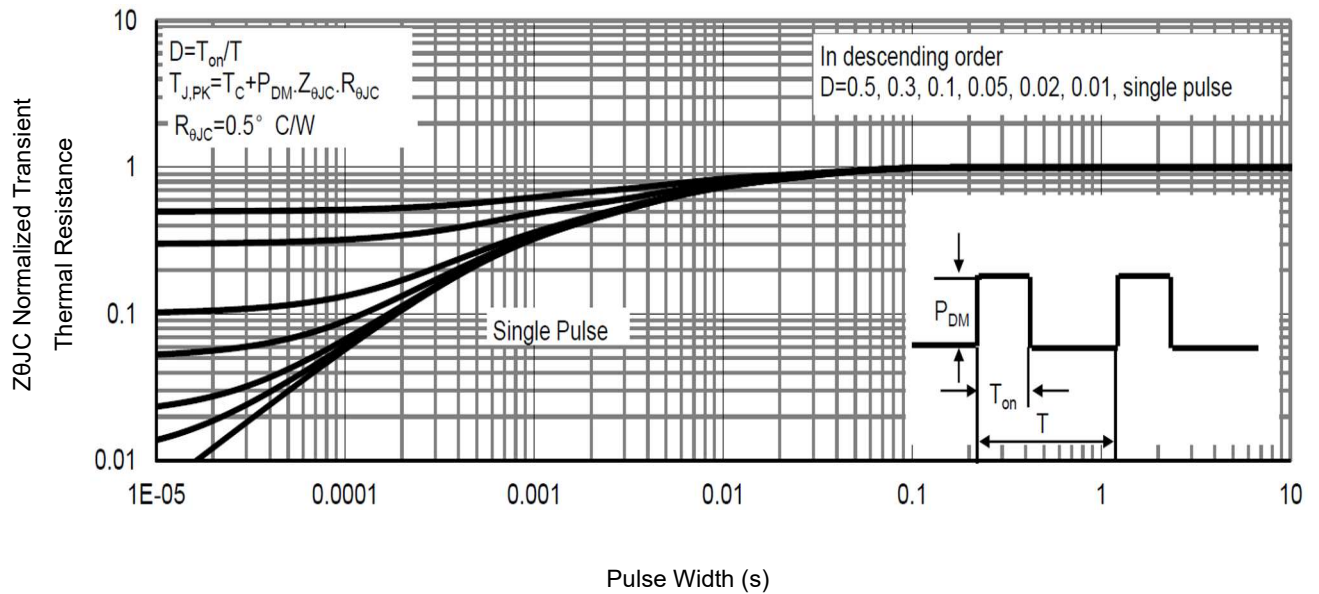


Fig11 . Normalized Maximum Transient Thermal Impedance

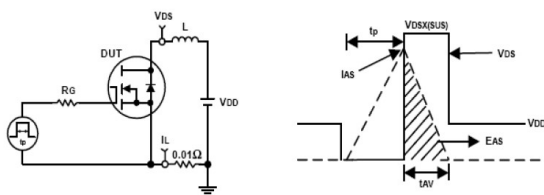


Fig12. Unclamped Inductive Test Circuit and waveforms

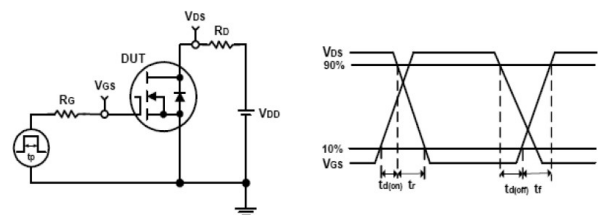
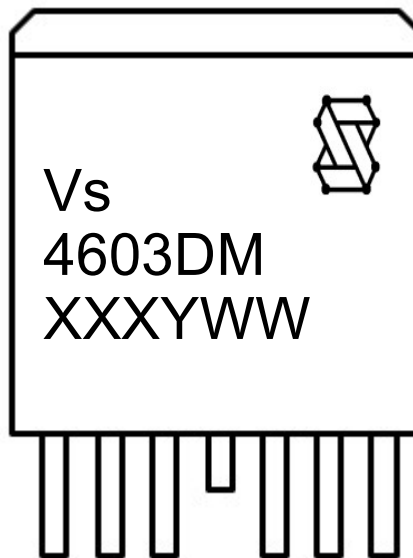


Fig13. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (4603DM)

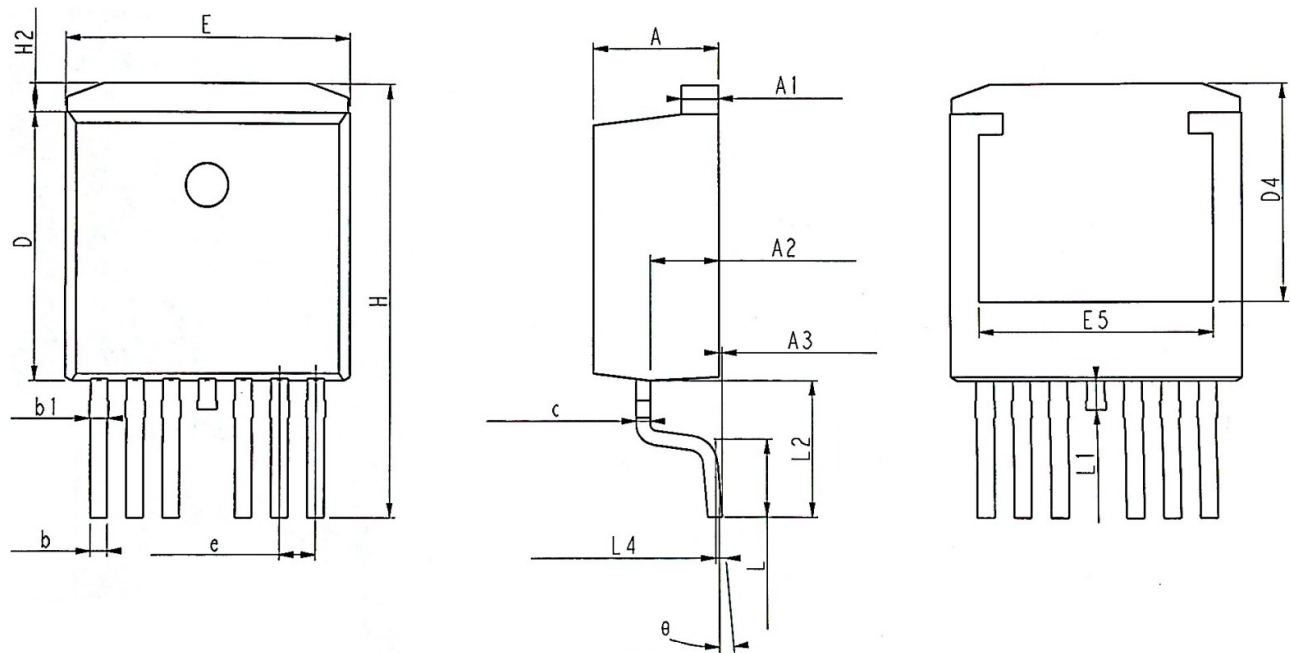
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-263-6L Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.25	4.40	4.55
A1	1.20	1.30	1.40
A2	2.25	2.40	2.55
A3	0.01	0.13	0.25
b	0.50	0.60	0.70
b1	0.58	0.68	0.84
c	0.40	0.50	0.60
D	9.05	9.25	9.45
D4	6.90		
e	1.27 BSC		
E	9.80	10.00	10.20
E5	7.25		
H	14.65	15.00	15.35
H2	0.80	1.00	1.20
L1	0.85	1.00	1.15
L2	4.20	4.70	5.20
L4	0.25 BSC		
θ	2 °	5 °	8 °

Notes:

1. Dimension "D" & "E" do NOT include mold flash, mold flash shall not exceed 0.127mm per side.

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