MC20901

5 Channel
FPGA Bridge IC

for

MIPI D-PHY Systems

and

SLVS to LVDS Conversion

DATASHEET

Version 1.08

December 2016

Meticom GmbH

Revision History

MC20901		
Version	**Date of Issue**	**Change**
1.00	May 31 2013	• First Draft
1.01	June 05 2013	• Minor changes in drawings and tables
1.02	June 07 2013	• format title 5.1 • table of contents
1.03	June 13, 2013	• format issues
1.04	March 14, 2014	• BTA description details added
1.05	April 4, 2014	• Package drawing update • Application note added - input to output signal diagram
1.06	August 19, 2014	• Table 3: VCM-IN and |Vin-Diff| values updated • Table 4: Propagation delay and jitter values updated • Package dimensions updated
1.07	August 1, 2016	• Chapter 6.8 Figure number corrected • Figure 8: Signal name error corrected • 'Preliminary' status of data sheet removed
1.08	December 22, 2016	• Figure 6 and 7: pin polarity corrected

Table of Contents

1 General Description

The MC20901 is a high performance 5 Channel FPGA bridge IC, which converts MIPI D-PHY compliant input streams into LVDS high speed and CMOS low speed output data streams.
The MC20901 can also convert an SLVS signal into an LVDS signal.

The MC20901 outputs can be directly connected to FPGAs or DSPs.

Data rates range from 0 Mbps to 2.5 Gbps in HS (High Speed) mode and up to 20 Mbps in LPDT (Low Power Data Transmission) mode.

2 Key Features

- Input is compliant to MIPI D-PHY interfaces using the DSI, CSI-1 and CSI-2 standards
    - HS mode data rate: up to 2.5 Gbps
    - LPDT mode data rate: up to 20 Mbps
- Conversion of SLVS input to LVDS output
    - SLVS data rate: up to 2.5 Gbps
- BTA (Bus Turnaround option for Channel A or E)
- Pin swap option (all channels simultaneously)
- 5 Channel device (e.g. 4x DATA, 1x CLK)
- D-PHY input termination automatically switched depending on HS or LP mode
- No additional level shifters needed
- Arbitrary power up sequence
- Available as a bare die
    - RoHS compliant, Pb-free
- Available in a TQLMP-48 package
    - 7mm * 7mm * 0.9mm
    - 0.5mm pitch
    - RoHS compliant, Pb-free

3 Block Diagram

3.1 Block Diagram

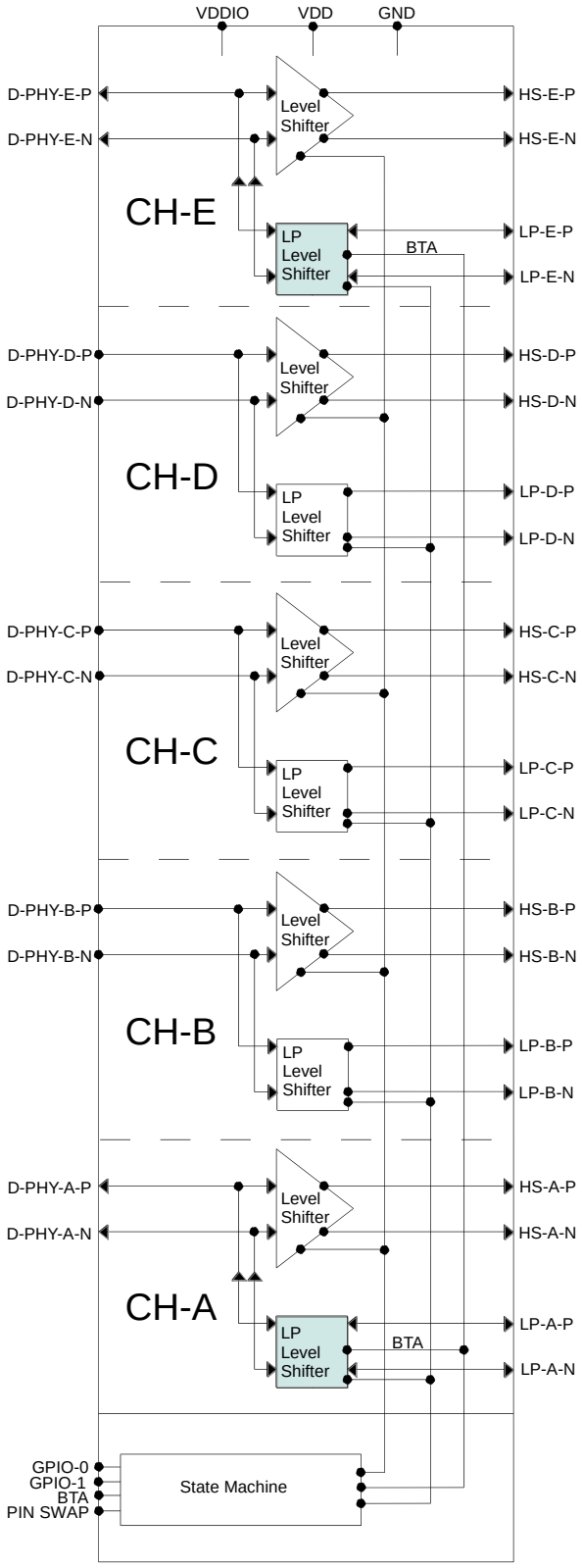


Figure 1: Functional Block Diagram of the MC20901

4 Parametrics

4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{DDIO}	Supply voltage		-0.5	3.6	V
V_{DD}	Supply voltage		-0.5	2.0	V
T_{STG}	Storage temperature		-55	125	°C
T_J	Junction temperature		-55	125	°C
V_{ESD}	Electrostatic discharge voltage capability	(HBM; 100 pF, 1.5 kΩ)	2.0		kV
$V_{ESD\text{-}Dout}$	Electrostatic discharge voltage capability at differential I/Os	(HBM; 100 pF, 1.5 kΩ)	500		V

Table 1: Absolute Maximum Ratings

Notes:

Absolute Maximum Ratings may not be exceeded to the device without causing permanent damage or degradation. Exposures to these values for extended periods may affect device reliability. If the device is operated beyond the range of Operating Conditions functionality is not guaranteed.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDIO}	Supply voltage		2.3	2.5	2.7	V
V_{DD}	Supply voltage		1.1	1.2	1.3	V
GND	Ground			0		V
$V_{noise,VDD}$	Maximum allowed supply noise on V_{DD}	see Figure 2			100	mV_{pp}
T_A	Ambient temperature		-40	25	100	ºC

Table 2: Operating Conditions

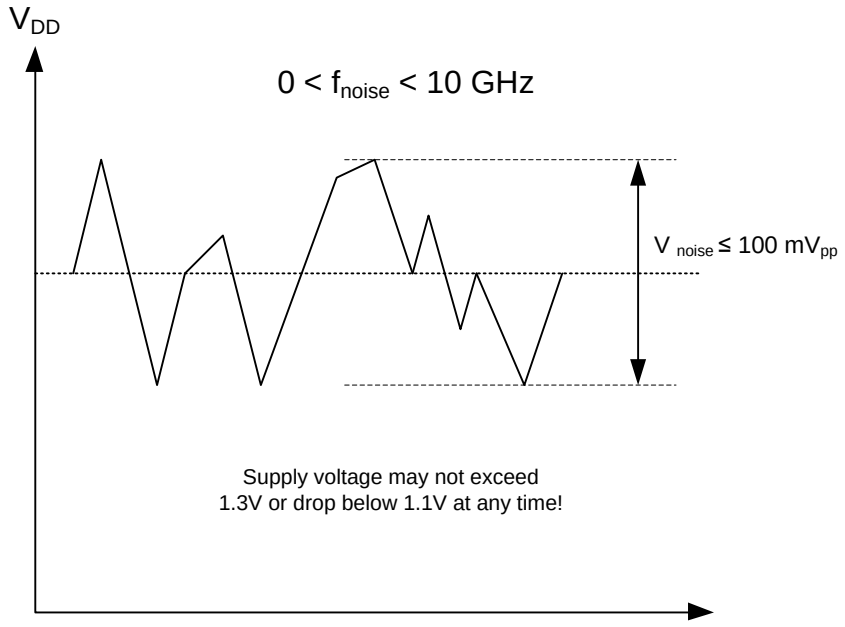


Figure 2: Maximum Allowed Supply Noise on V_{DD}

4.3 DC Characteristics

(At recommended operating conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD25HS}	HS mode supply current VDDIO	@2.5Gbps	27	33.5	40	mA
I_{DD12HS}	HS mode supply current VDD	@2.5Gbps	0.9	1.3	1.6	mA
I_{DD25LP}	LP mode supply current VDDIO	@20Mbps	27	33.5	40	mA
I_{DD12LP}	LP mode supply current VDD	@20Mbps	0.6	1.25	2	mA
Single Ended Outputs (LP-X-P, LP-X-N) *1						
V_{OH}	LP high level output voltage	Tracks VDDIO	2.3	2.5	2.7	V
V_{OL}	LP low level output voltage			0	0.2	V
Single Ended Inputs (GPIO-0, GPIO-1, BTA, PINSWAP)						
V_{IH}	high level input voltage		0.7		VDDIO	V
V_{IL}	low level input voltage		0		0.2	V
HS Outputs (HS-X-P, HS-X-N) *1						
V_{CM-OUT}	Output common mode voltage	Tracks VDD	1.09	1.2	1.31	V
$\|V_{DO-Diff}\|$	Differential output voltage		250	300	350	mVp
Z_{OD}	Output impedance	Differential	80	100	120	Ω
Differential Inputs ($D_{PHY-X-P}$, $D_{PHY-X-N}$) *1						
V_{IH}	LP high level input voltage		0.88		1.35	V
V_{IL}	LP low level input voltage		0		0.55	V
I_{IH}	High level Input current	Input termination off			100	nA
I_{IL}	Low level input current	Input termination off			100	nA
C_{IN}	Input capacitance	Including package		1	1.5	pF
V_{CM-IN}			70	200	330	mV
$\|V_{IN-Diff}\|$		@ up to 1.5Gbps	70	200	400	mV
		@ above 1.5Gbps	140	200	400	mV
Z_{IN}		Differential	80	100	120	Ω

*1 X means the Channels A to E

Table 3: DC Characteristics

4.4 AC Characteristics

(At recommended operating conditions)

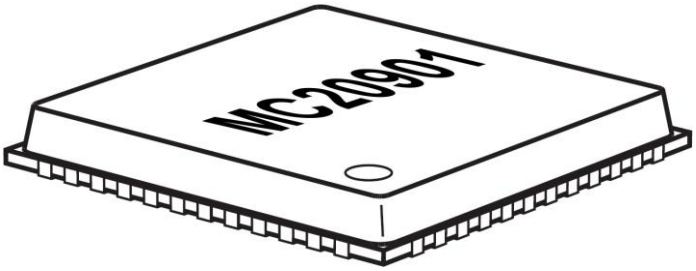
Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
t_{PU}	Power up time				10	µs	
t_{HS}	Min delay HS sequence to HS data				2	ns	
Single Ended Outputs (LP-X-P, LP-X-N) **)							
BR_{LP}	Maximum LP output bit rate		20			Mbps	
HS Outputs (HS-X-P, HS-X-N) **)							
BR_{HS}	Maximum supported output bit rate		2.5			Gbps	
T_r/T_f	Output data transition time	20%-80%		90	140	ps	
S_{22}	Output return loss	@ 500 MHz			15	dB	
J_D	Deterministic output jitter				30	ps	
J_R	Generated random jitter			0.35	0.7	ps_{rms}	
J_{PSRR}	Jitter caused by PSRR	Supply noise @ VDD		1	2	ps/mV	
T_{DEL}	HS propagation delay	DPHY input to HS output	300	500	900	ps	
T_{SKEW}	HS Propagation delay mismatch	3 sigma mismatch between channels A,B,C,D,E	-	-	50	ps	
Differential Inputs ($D_{PHY-X-P}$, $D_{PHY-X-N}$) **)							
BR_{HS}	Maximum supported input bit rate		2.5			Gbps	
S_{11}	Input return loss	@ 500 MHz			15	dB	

**) X means the Channels A to E

Table 4: AC Characteristics

5 Package Information

5.1 TQLMP-48 Package



(drawing not to scale)

- Package Type: Thin Quad Leadless Molded Package (TQLMP)
- Package dimensions: 7.0 x 7.0 x 0.75 mm
- Pin pitch: 0.5 mm

5.2 Pin Description

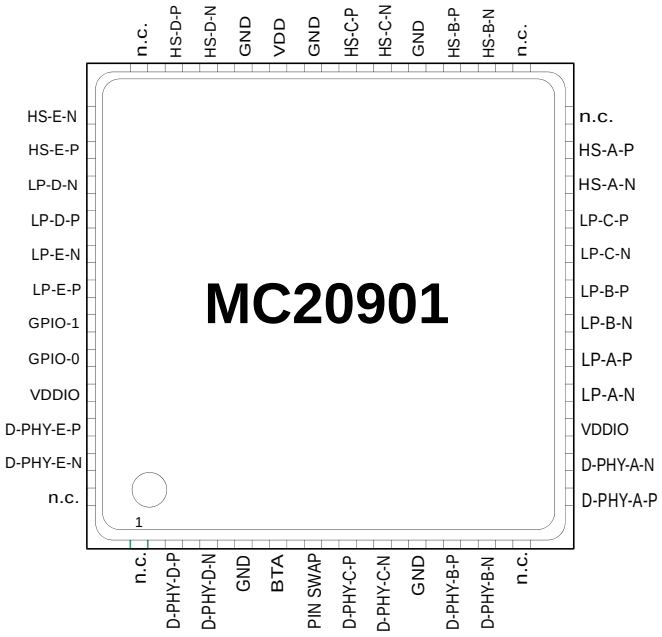
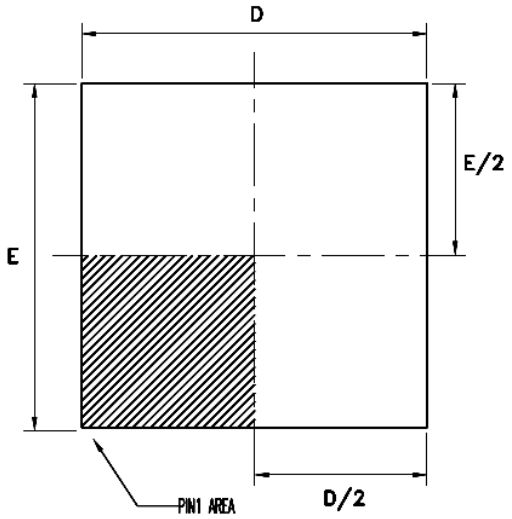


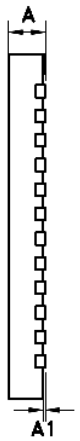
Figure 3: Pin Assignment MC20901

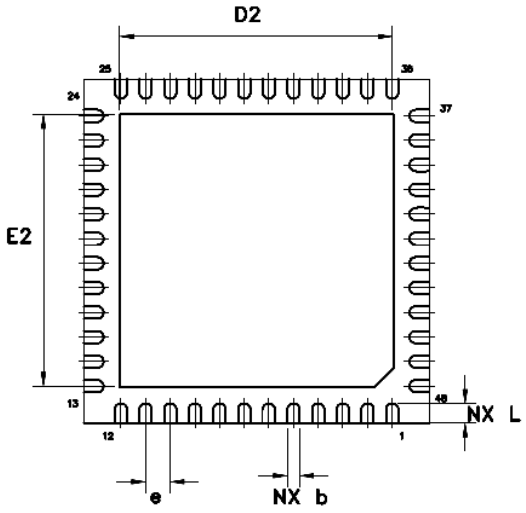
Pin Name	Pin No.	I/O	Type	Description
VDD	32	P	Supply	Supply voltage for the SLVS input driver and internal logic
VDDIO	15, 45	P	Supply	Supply voltage for the LVDS output stage and internal level shifters
GND	4, 9, 28, 31, 33	-	-	*Global ground*
D-PHY-A-P	13	I/O	SLVS/CMOS	MIPI D-PHY compliant positive input or SLVS positive input, channel A, output for BTA
D-PHY-A-N	14	I/O	SLVS/CMOS	MIPI D-PHY compliant negative input or SLVS negative input, channel A, output for BTA
HS-A-P	23	O	LVDS	Positive LVDS high speed output, channel A
HS-A-N	22	O	LVDS	Negative LVDS high speed output, channel A
LP-A-P	17	I/O	CMOS	Positive CMOS low power data output, channel A, input for BTA
LP-A-N	16	I/O	CMOS	Negative CMOS low power data output, channel A, input for BTA
D-PHY-B-P	10	I	SLVS/CMOS	MIPI D-PHY compliant positive input or SLVS positive input, channel B
D-PHY-B-N	11	I	SLVS/CMOS	MIPI D-PHY compliant negative input or SLVS negative input, channel B
HS-B-P	27	O	LVDS	Positive LVDS high speed output, channel B
HS-B-N	26	O	LVDS	Negative LVDS high speed output, channel B
LP-B-P	19	O	CMOS	Positive CMOS low power data output, channel B
LP-B-N	18	O	CMOS	Negative CMOS low power data output, channel B
D-PHY-C-P	7	I	SLVS/CMOS	MIPI D-PHY compliant positive input or SLVS positive input, channel C
D-PHY-C-N	8	I	SLVS/CMOS	MIPI D-PHY compliant negative input or SLVS negative input, channel C
HS-C-P	30	O	LVDS	Positive LVDS high speed output, channel C
HS-C-N	29	O	LVDS	Negative LVDS high speed output, channel C
LP-C-P	21	O	CMOS	Positive CMOS low power data output, channel C
LP-C-N	20	O	CMOS	Negative CMOS low power data output, channel C
D-PHY-D-P	2	I	SLVS/CMOS	MIPI D-PHY compliant positive input or SLVS positive input, channel D
D-PHY-D-N	3	I	SLVS/CMOS	MIPI D-PHY compliant negative input or SLVS negative input, channel D
HS-D-P	35	O	LVDS	Positive LVDS high speed output, channel D
HS-D-N	34	O	LVDS	Negative LVDS high speed output, channel D
LP-D-P	40	O	CMOS	Positive CMOS low power data output, channel D
LP-D-N	39	O	CMOS	Negative CMOS low power data output, channel D
D-PHY-E-P	46	I/O	SLVS/CMOS	MIPI D-PHY compliant positive input or SLVS positive input, channel E, output for BTA
D-PHY-E-N	47	I/O	SLVS/CMOS	MIPI D-PHY compliant negative input or SLVS negative input, channel E, output for BTA
HS-E-P	38	O	LVDS	Positive LVDS high speed output, channel E
HS-E-N	37	O	LVDS	Negative LVDS high speed output, channel E
LP-E-P	42	I/O	CMOS	Positive CMOS low power data output, channel E, input for BTA
LP-E-N	41	I/O	CMOS	Negative CMOS low power data output, channel E, input for BTA
GPIO-0	44	I	CMOS	General purpose configuration input 0
GPIO-1	43	I	CMOS	General purpose configuration input 1
BTA	5	I	CMOS	Bus turnaround control pin
PINSWAP	6	I	CMOS	Pin swap function control pin
N.C.	1,12,24,25,36,48	-	-	Do not connect
Thermal Pad		-	-	Thermal Pad may be connected to GND or left floating (n.c.)

Table 5: Pin Description

5.3 Package Information







JEDEC#	MO-220 / VKKD			
TYPE	48 LEAD			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.70	0.80	27.56	31.50
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	6.9	7.1	271.65	279.53
E	6.9	7.1	271.65	279.53
D2	5.5	5.6	216.54	220.47
E2	5.5	5.6	216.54	220.47
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	12			
NE	12			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

Figure 4: Mechanical Dimensions TQLMP-48

6 Application Notes

6.1 Application Overview

The MC20901 can be used with D-PHY sources (e.g. cameras) as shown in the picture below. In this example D-PHY compliant source signals coming from the camera are converted into standard LVDS and CMOS signals, which can then be fed directly into an FPGA or DSP for signal processing.

The diagram also shows the MC20902, which performs the reverse function of the MC20901.

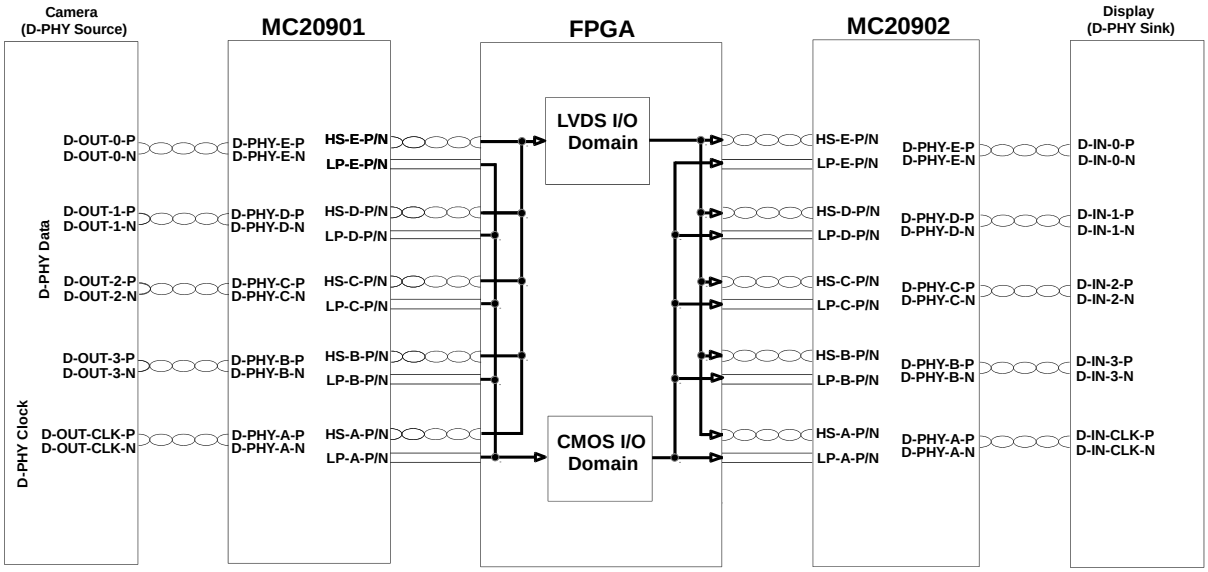


Figure 5: Application Diagram

6.2 D-PHY to FPGA Bridge Application

In this example one D-PHY clock lane and four D-PHY data lanes in regular configuration are shown.

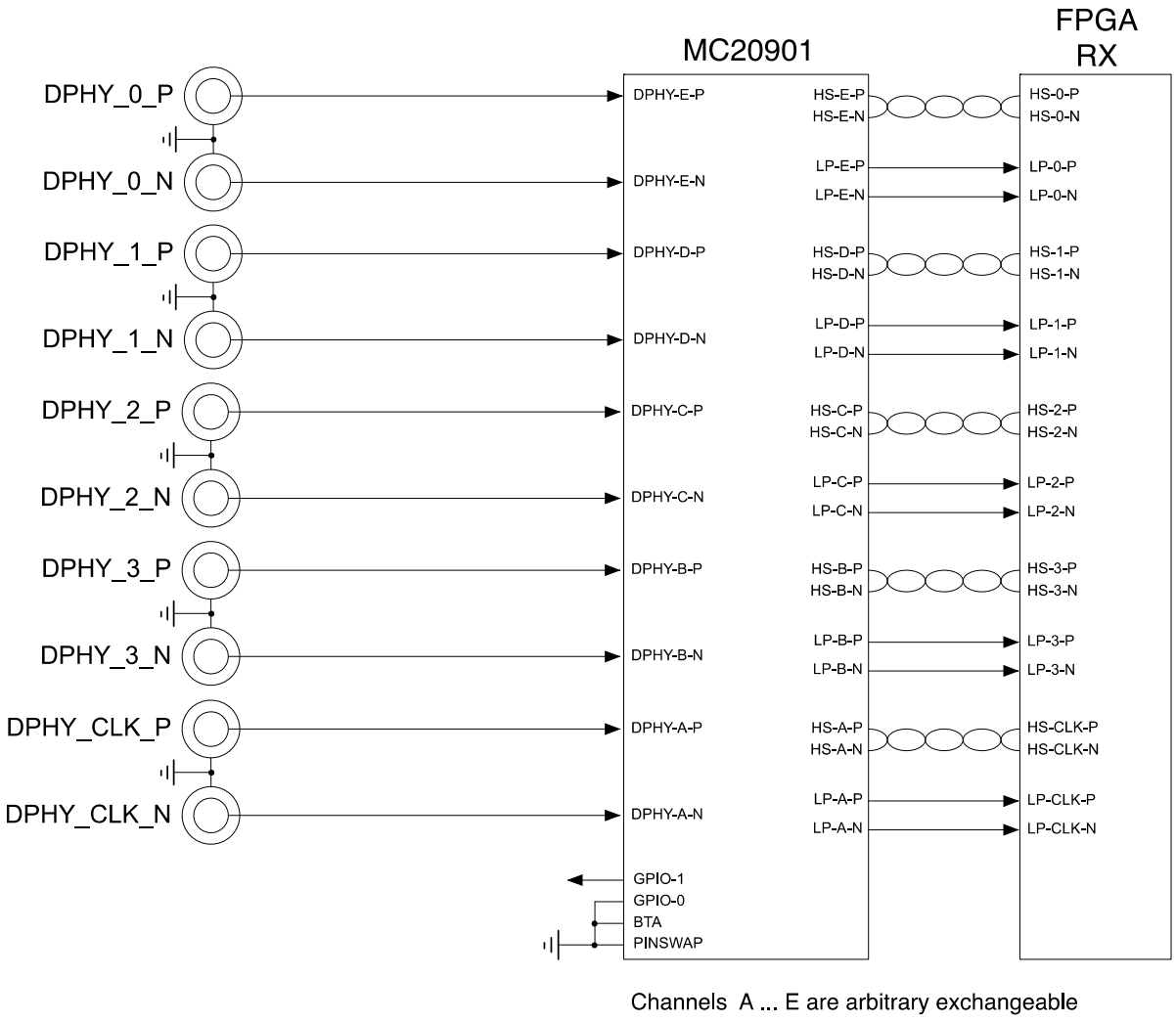


Figure 6: D-PHY to FPGA Bridge Application

6.3 D-PHY to FPGA Bridge Application with Bus Turnaround

In this example one D-PHY clock lane and four D-PHY data lane are shown.
Via pin settings, the IC is configured for bus turnaround on channel E (D-PHY_0)

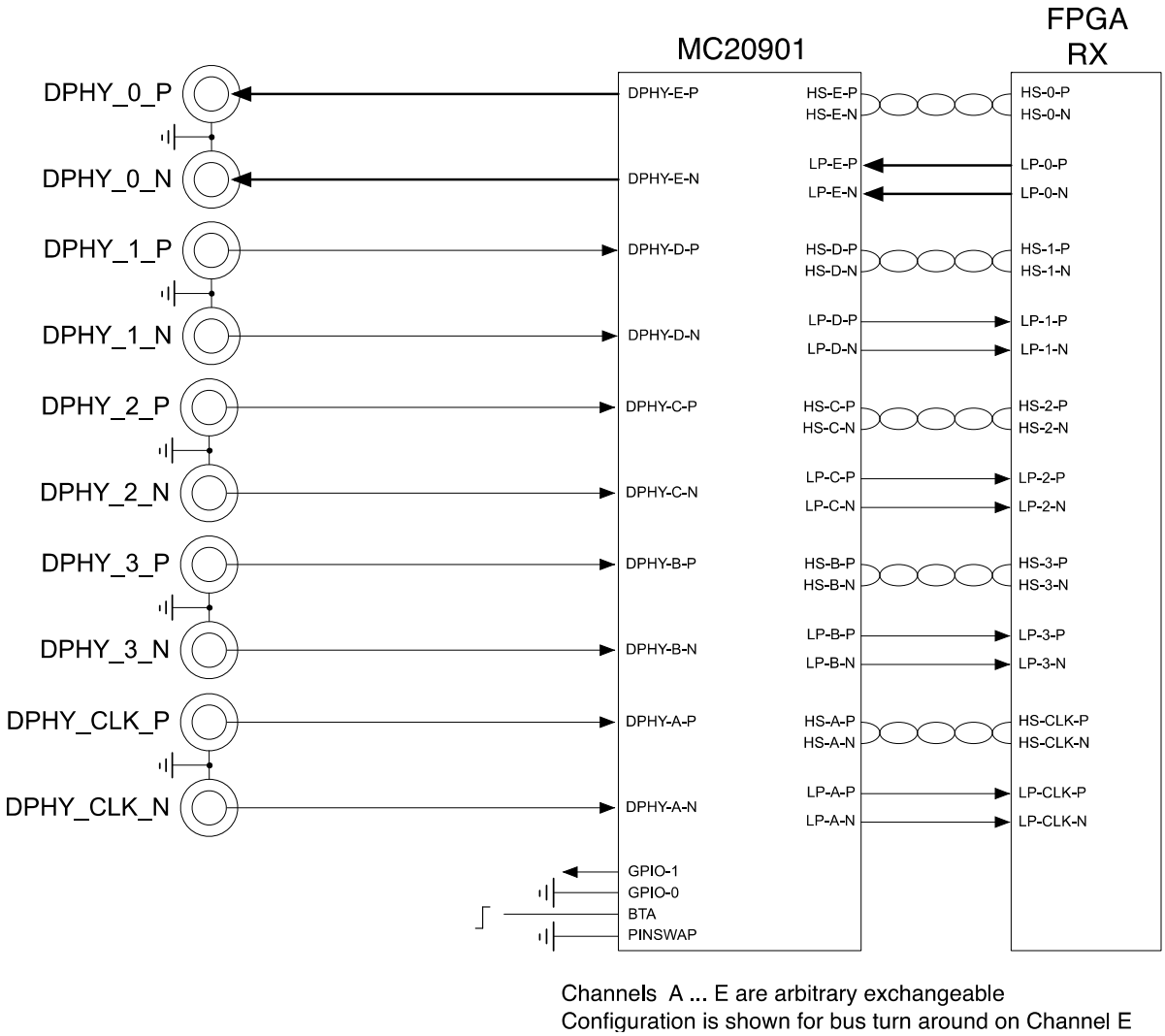


Figure 7: D-PHY to FPGA Bridge Application with Bus Turnaround

6.4 Signal Levels

6.4.1 HS-X-P and HS-X-N LVDS Outputs *[1]

The common mode voltage is V_{DD}. The differential swing is typically 300mV.

6.4.2 LP-X-P and LP-X-N CMOS Outputs *[1]

These signals are in the V_{DDIO} domain.

6.4.3 DPHY-X-P and DPHY-X-N Inputs *[1]

These signals are compliant with the MIPI D-PHY specification.

6.4.4 GPIO-0, GPIO-1, BTA, PINSWAP CMOS Inputs

These signals are in the V_{DDIO} domain.

*[1] X means the Channels A to E

6.5 Configuration Using GPIO-0 and GPIO-1

GPIO-1	GPIO-0	Description
0	0	IC power down
0	1	SLVS to LVDS conversion mode activated
1	0	D-PHY mode, Bus Turnaround capability assigned to channel E
1	1	D-PHY mode, Bus Turnaround capability assigned to channel A

Table 6: GPIO Selection Bits

6.6 Configuration Using BTA

BTA	Description
0	Bus Turnaround not enabled
1	Bus Turnaround enabled on the channel selected according to Table 6. The direction of LP data transmission is changing instantaneously.

Table 7: BTA input Bits

A low level at BTA Pin means that the LP pins are treated as output pins (normal operation).
A high level at the BTA pin means that the LP pins for the selected channel (see Table 6) are acting as input pins. In this configuration the incoming LP signals at the selected channel
(LP-X-P and LP-X-N) are outputted at the according D-PHY pins DPHY-X-P and DPHY-X-N.

6.7 Configuration Using PINSWAP

PINSWAP	Description
0	Pin Swap off
1	Pin Swap D-PHY-X (swaps D-PHY-X-P and D-PHY-X-N pins) Please note: Pin swap is not active if BTA=1
floating	Pin Swap HS-X (swaps HS-X-P and HS-X-N pins)

Table 8: PINSWAP input Bits

6.8 Input to Output Signal Diagram

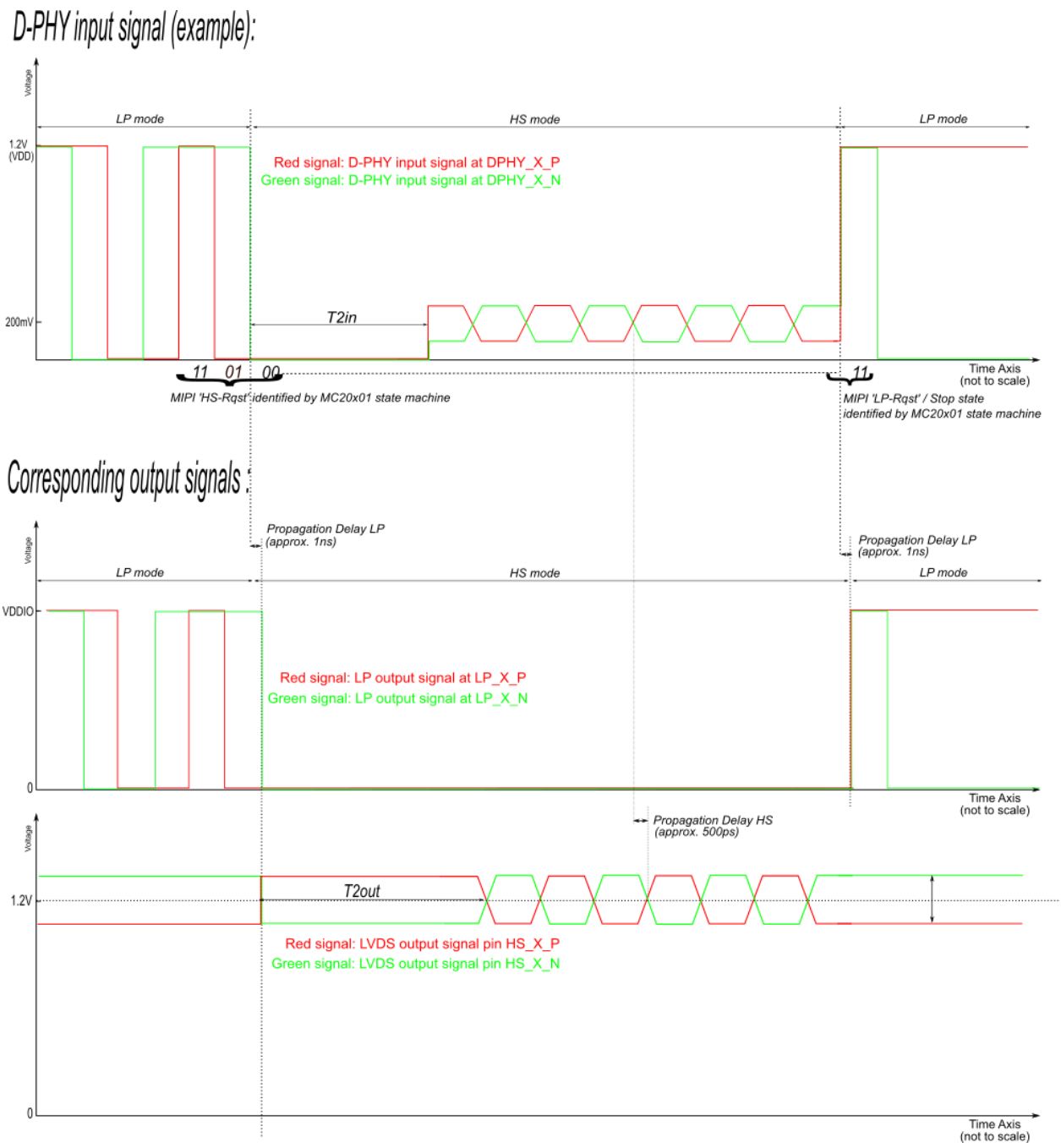


Figure 8: Input to Output Signal Diagram

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