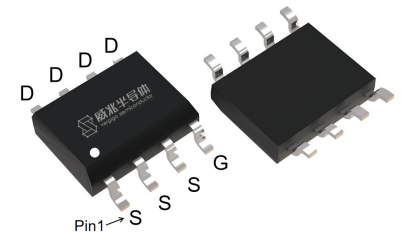


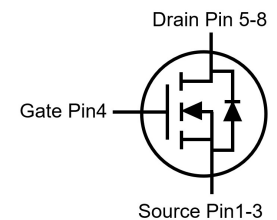
## Features

- Enhancement mode
- VitoMOS<sup>®</sup> II Technology
- Fast Switching and High efficiency
- 100% Avalanche Tested

$V_{DS}$	60	V
$R_{DS(on),TYP@ V_{GS}=10V}$	6.5	mΩ
$R_{DS(on),TYP@ V_{GS}=4.5V}$	9.5	mΩ
$I_D(\text{Silicon Limited})$	13	A

**SOP8**


Part ID	Package Type	Marking	Packing
VS6662GS	SOP8	6662GS	3000pcs/Reel



## Maximum ratings, at $T_A=25\text{ }^\circ\text{C}$ , unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	60	V	
$V_{GS}$	Gate-Source voltage	$\pm 20$	V	
$I_S$	Diode continuous forward current	$T_A = 25\text{ }^\circ\text{C}$	13	A
$I_D$	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_A = 25\text{ }^\circ\text{C}$	13	A
$I_D$	Continuous drain current @ $V_{GS}=10V$ (Silicon limited)	$T_A = 70\text{ }^\circ\text{C}$	10	A
$I_{DM}$	Pulse drain current tested ①	$T_A = 70\text{ }^\circ\text{C}$	52	A
$E_{AS}$	Avalanche energy, single pulsed ②	25	mJ	
$P_D$	Maximum power dissipation	$T_A = 25\text{ }^\circ\text{C}$	2.5	W
		$T_A = 70\text{ }^\circ\text{C}$	1.6	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 150	$^\circ\text{C}$	

## Thermal Characteristics

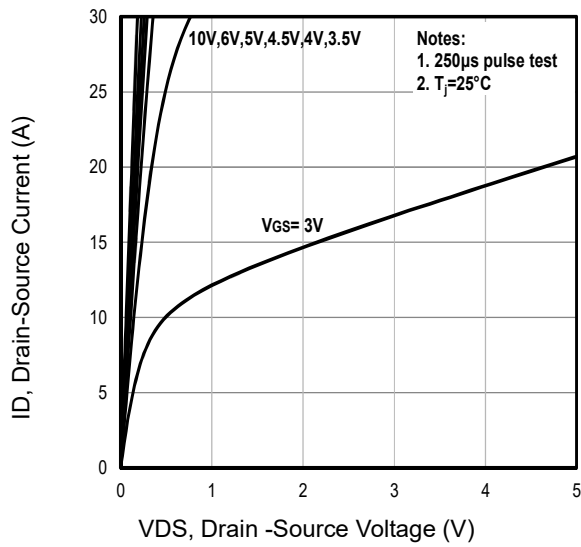
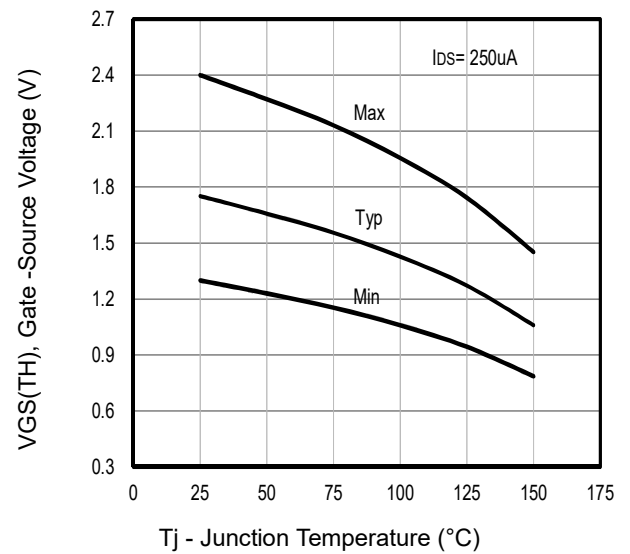
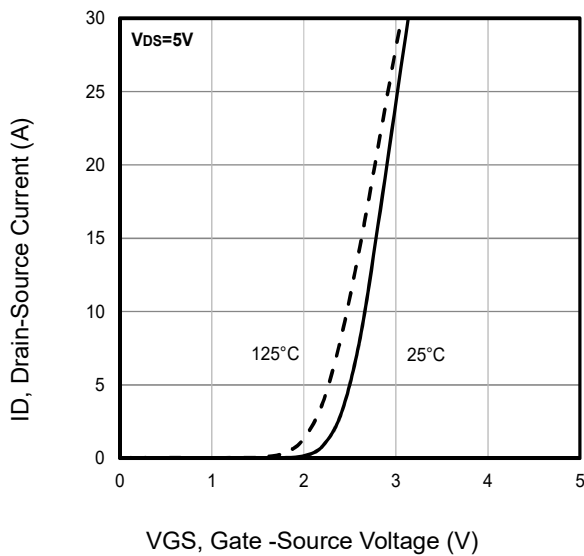
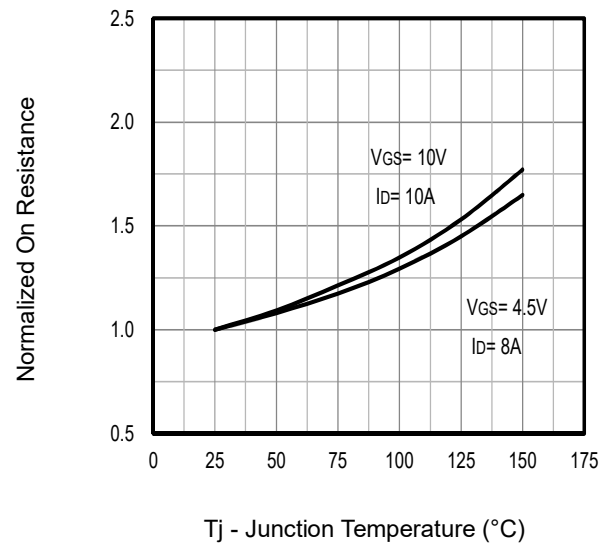
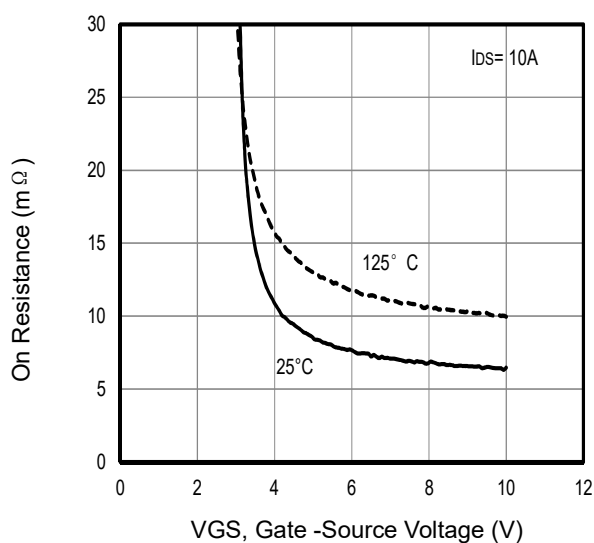
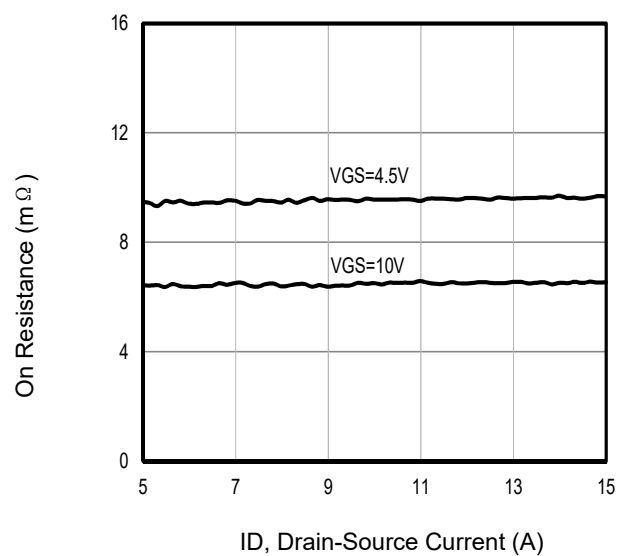
Symbol	Parameter	Typical	Max	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	24	29	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient③	$t \leq 10s$	42	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient③	Steady State	75	$^\circ\text{C/W}$

**Electrical Characteristics**

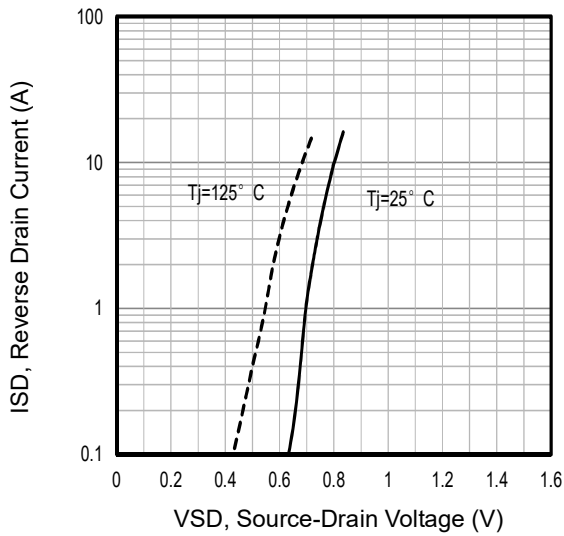
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
<b>Static Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current(T <sub>j</sub> =25°C)	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T <sub>j</sub> =125°C)	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	--	--	100	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	--	--	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3	1.75	2.4	V
R <sub>DS(on)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	--	6.5	8.5	mΩ
		T <sub>j</sub> =100°C	--	8.8	--	mΩ
R <sub>DS(on)</sub>	Drain-Source On-State Resistance ④	V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	--	9.5	12	mΩ
<b>Dynamic Electrical Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, f=1MHz	525	1050	1840	pF
C <sub>oss</sub>	Output Capacitance		170	345	600	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		15	35	65	pF
R <sub>g</sub>	Gate Resistance	f=1MHz	0.2	0.8	5	Ω
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V	--	22	39	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		--	12	21	nC
Q <sub>gs</sub>	Gate-Source Charge		--	3.2	5.6	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	5.8	10	nC
<b>Switching Characteristics</b>						
T <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =30V, I <sub>D</sub> =10A, R <sub>G</sub> =3Ω, V <sub>GS</sub> =10V	--	6.2	--	ns
T <sub>r</sub>	Turn-on Rise Time		--	16	--	ns
T <sub>d(off)</sub>	Turn-Off Delay Time		--	19	--	ns
T <sub>f</sub>	Turn-Off Fall Time		--	6.4	--	ns
<b>Source- Drain Diode Characteristics @ T<sub>j</sub> = 25°C (unless otherwise stated)</b>						
V <sub>SD</sub>	Forward on voltage	I <sub>SD</sub> =10A, V <sub>GS</sub> =0V	--	0.8	1.2	V
T <sub>rr</sub>	Reverse Recovery Time	I <sub>SD</sub> =10A, V <sub>GS</sub> =0V	--	23	46	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	--	11	22	nC

NOTE:

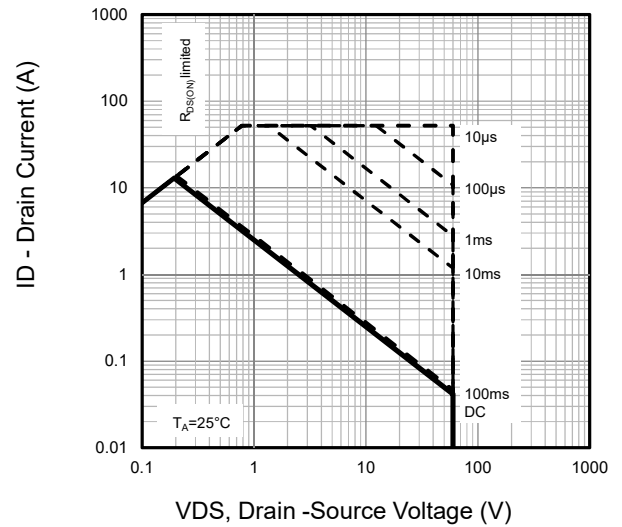
- ① Single pulse; pulse width ≤ 100μs.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.5mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 10A, V<sub>GS</sub> = 10V. Part not recommended for use above this value
- ③ The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board.
- ④ Pulse width ≤ 380μs; duty cycle ≤ 2%.

**Typical Characteristics**

**Fig1.** Typical Output Characteristics

**Fig2.** Typical  $V_{GS(TH)}$  Gate-Source Voltage Vs.  $T_j$ 

**Fig3.** Typical Transfer Characteristics

**Fig4.** Typical Normalized On-Resistance Vs.  $T_j$ 

**Fig5.** Typical On Resistance Vs Gate-Source Voltage

**Fig6.** Typical On Resistance Vs Drain Current and Gate Voltage

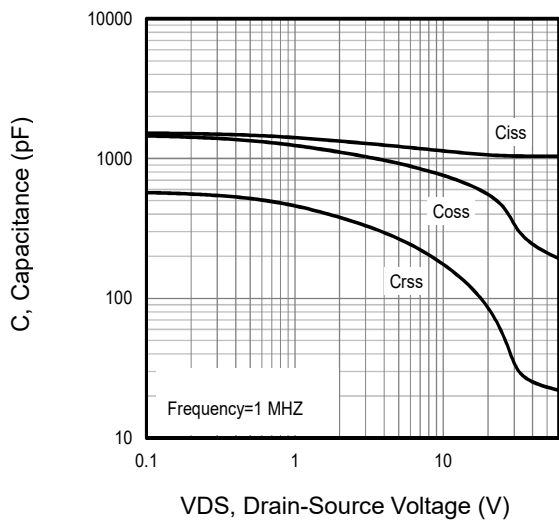
**Typical Characteristics**



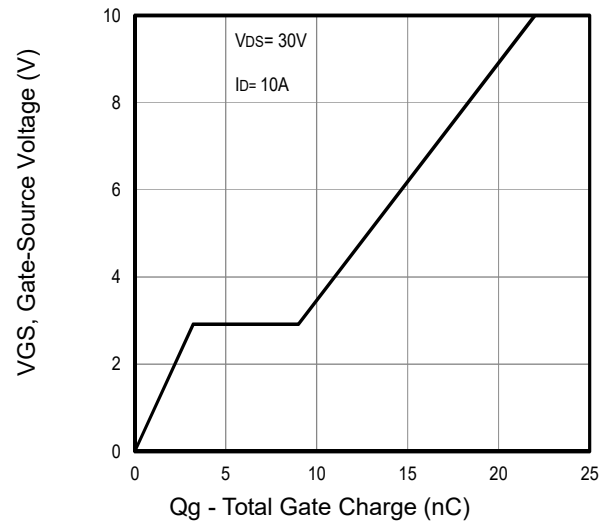
**Fig7.** Typical Source-Drain Diode Forward Voltage



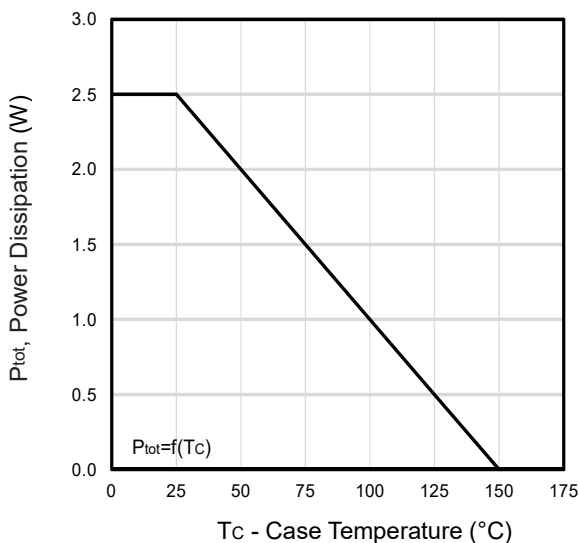
**Fig8.** Maximum Safe Operating Area



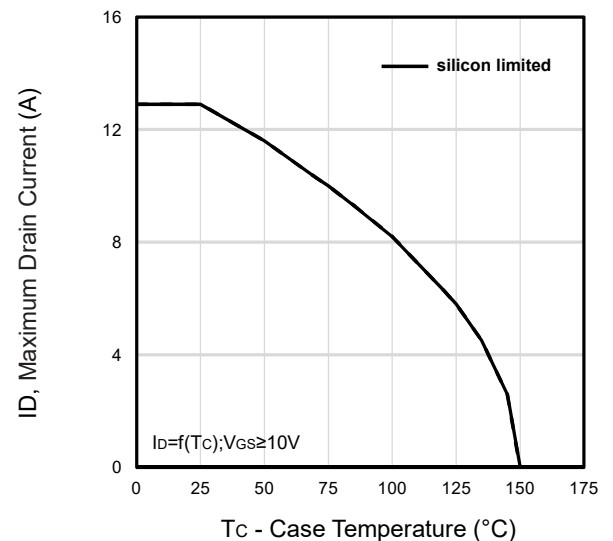
**Fig9.** Typical Capacitance Vs. Drain-Source Voltage



**Fig10.** Typical Gate Charge Vs. Gate-Source Voltage

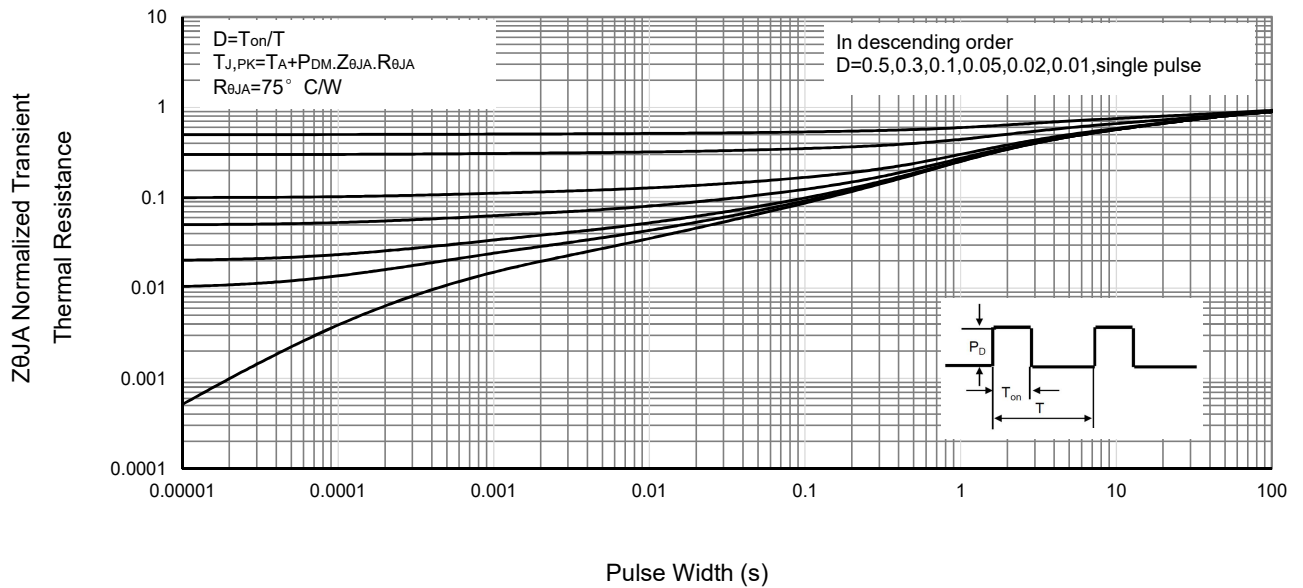


**Fig11.** Power Dissipation Vs. Case Temperature

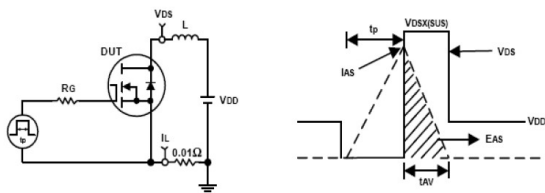


**Fig12.** Maximum Drain Current Vs. Case Temperature

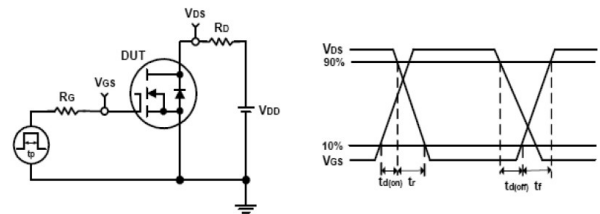
**Typical Characteristics**



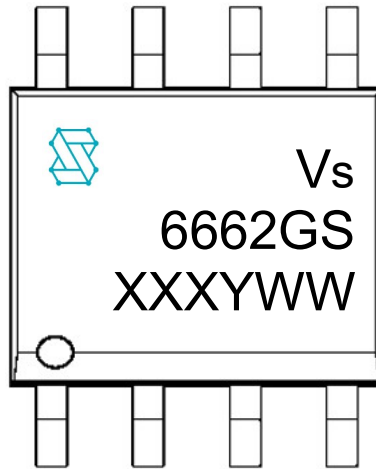
**Fig13 . Normalized Maximum Transient Thermal Impedance**



**Fig14. Unclamped Inductive Test Circuit and waveforms**



**Fig15. Switching Time Test Circuit and waveforms**

**Marking Information**


1<sup>st</sup> line: Vergiga Code (Vs), Vergiga Logo

2<sup>nd</sup> line: Part Number (6662GS)

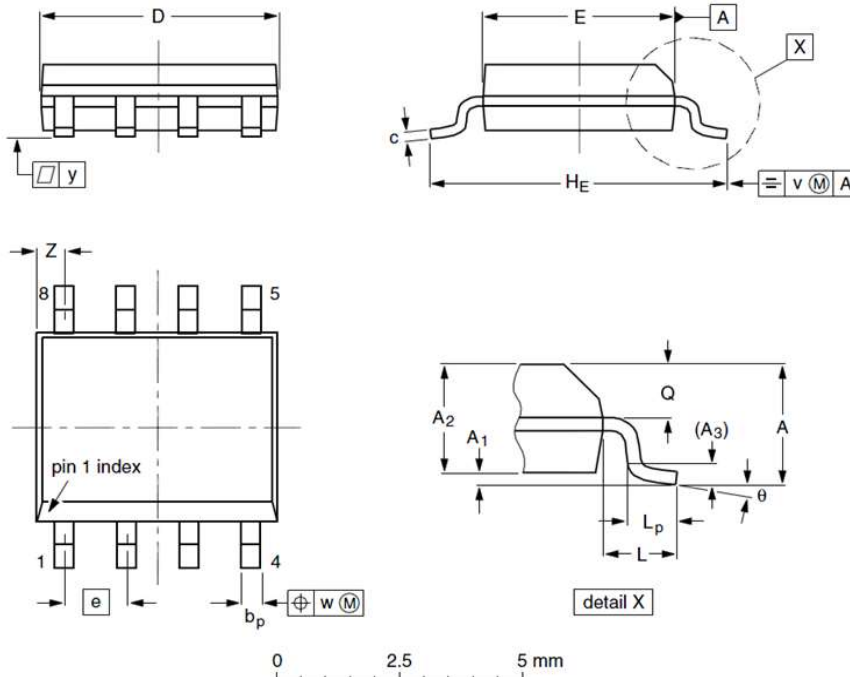
3<sup>rd</sup> line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

**SOP8 Package Outline Data**


Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A <sub>1</sub>	0.10	0.18	0.25
A <sub>2</sub>	1.25	1.35	1.50
A <sub>3</sub>	--	0.25	--
b <sub>p</sub>	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H <sub>E</sub>	5.80	6.00	6.20
L	--	1.05	--
L <sub>p</sub>	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

**Notes:**

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "b<sub>p</sub>" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "b<sub>p</sub>" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

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