NSiP83086

Signal Isolated RS-485 Transceiver With Integrated DC to DC Converter

Datasheet (EN) 0.4

Product Overview

NSiP83086 is a high reliability isolated full duplex RS-485 transceiver with integrated DC to DC converter. The NSiP83086 isolated DC-DC converter use on chip transformer. The feedback PWM signal is sent to primary side by a digital isolator based on Novosense capacity isolation technology. Both devices are safety certified by UL1577 support 5kVrms insulation withstand voltages, while the high integrated solution can help to simplify system design and improve reliability.

The Bus pins of NSiP83086 are protected from ±10kV system level ESD to GND2 on Bus side. The device feature fail-safe circuitry, which guarantee a logic-high receiver output when the receiver inputs are open or shorted. The device have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus.

Key Features

- Up to 5000Vrms Insulation voltage
- Isopower integrated isolated dc-to-dc converter
- I/O voltage range supports 1.8~5.5V MCU
- Power supply voltage:

  VDD:4.5V to 5.5V

  VDDL:1.8V to 5.5V
- Over current and over temperature protection
- High CMTI: ±150kV/us
- Data rate:16Mbps
- Up to 256 transceivers on the bus
- High system level EMC performance:

  Bus Pins meet IEC61000-4-2 ±10kV ESD
- Isolation Barrier Life: >60 years
- Operation temperature: -40℃~105℃
- RoHS-compliant packages:

  SOW20

Safety Regulatory Approvals

- UL recognition: up to 5000Vrms for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

Device Information

Part Number	*Package*	*Body Size*
NSiP83086-DSWTR	SOW20	12.80mm × 7.50mm

Functional Block Diagrams

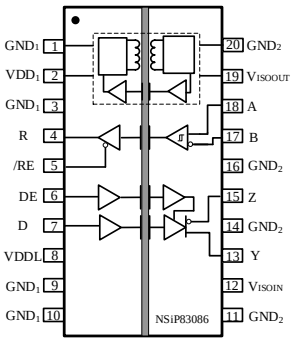

Figure 1. NSiP83086 Block Diagrams

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1. Pin Configuration And Functions

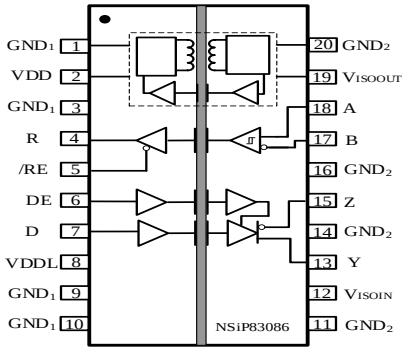


Figure 1.1 NSiP83086 Package

Table1.1 NSiP83086 Pin Configuration and Description

NSiP83086 PIN NO.	SYMBOL	FUNCTION
1	GND1	Ground 1, the ground reference for Isolator Side 1
2	VDD	Power Supply for Isolator Side 1 ,It is recommended this pin have a 10 µF capacitor to GND1 (Pin1,pin3)
3	GND1	Ground 1, the ground reference for Isolator Side 1
4	R	Receive output
5	/RE	Receive enable input. This is an active low input.
6	DE	Driver enable input. This is an active high input
7	D	Driver transmit data input.
8	VDDL	I/O Power Supply input. Side1 I/O logic level.
9	GND1	Ground 1, the ground reference for Isolator Side 1
10	GND1	Ground 1, the ground reference for Isolator Side 1
11	GND2	Ground 2, the ground reference for Isolator Side 2
12	VISOIN	Isolated power supply input. This pin must be connected externally to VISOOUT. It is recommended this pin have a 0.1 µF capacitor to GND2 (Pin12). Connect this pin through a ferrite bead and short trace length to VISOIN for operation.
13	Y	Noninverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND2	Ground 2, the ground reference for Isolator Side 2
15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.

16	GND2	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input.
18	A	Noninverting Receiver Input.
19	VISOOUT	Isolated Power Supply Output. This pin must be connected externally to VISOIN. It is recommended that a ferrite bead reservoir capacitor of 10 µF and a decoupling capacitor of 0.1 µF be fitted between Pin 19 and Pin 20.
20	GND2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD，VDDL	-0.5		6	V	
Maximum Input Voltage	/RE, DE, D	-0.4		VDDL+0.4	V	
Driver Output/Receiver Input Voltage	V_A, V_B, V_Y, V_Z	-7		12	V	
R output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			4.6	kV	
Operating Temperature	Topr	-40		105	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	*Symbol*	*min*	*typ*	*max*	*unit*
Power Supply Voltage	VDD	4.5		5.5	V
Operating Temperature	Topr	-40		105	℃
Logic High Level Input Voltage	V_{IH}	0.7*VDDL		VCC	V
Logic Low Level Input Voltage	V_{IL}	0		0.3*VDDL	V
Data rate	DR			16	Mbps

4. Thermal Information

Parameters	*Symbol*	*Value*	*Unit*

IC Junction-to-Air Thermal Resistance	θ_{JA}	56.8	°C/W
Junction-to-case (top) thermal resistance	$\theta_{jc(top)}$	15.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	28.5	°C/W

5. Specifications

5.1. DC Electrical Characteristics

(VDD=4.5V~5.5V, VDDL=1.8~5.5V,Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power supply voltage	VDD	4.5		5.5	V	
	VDDL	1.8		5.5	V	
Supply current Data rate ⩽16Mbps	I_{DD}		89		mA	VDD=5V, R_L=120 Ω
			137		mA	VDD=5V, R_L=54 Ω
	I_{DDL}		42		uA	
Isolated supply voltage	V_{ISOOUT}		5		V	
Thermal-Shutdown Threshold	T_{TS}		165		℃	
Thermal-Shutdown Hysteresis	T_{TSH}		15		℃	
Common Mode Transient Immunity	CMTI	±100	±150		kV/us	
Logic Side						
Input High Voltage	V_{IH}	0.7*V_{DDL}			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.3*V_{DDL}	V	DE, D, /RE
Input Pull up Current	I_{PU}			20	uA	DE,/RE
Input Pull down Current	I_{PD}	-20			uA	DI
Output Voltage High	V_{OH}	0.8*V_{DDL}			V	I_{OH} = -4mA
Output Voltage Low	V_{OL}			0.2*V_{DDL}	V	I_{OL} = 4mA
Output Short-Circuit Current	I_{OSR}			150	mA	0 ≤ V_R ≤VDD
Three-State Output Current	I_{OZ}	-15			uA	0 ≤ V_R ≤ VDD , /RE = high

Input Capacitance	C_{IN}		2		pF	DE, D, /RE
Driver						
Differential Output Voltage	$\lvert V_{OD} \rvert$			5.5	V	No Load
		2.7		5.5	V	Figure 5.6,R_L=120Ω ,VDD2=5V
		2.1		5.5	V	Figure 5.6, R_L=54Ω (RS-485),VDD2=5V
Change in magnitude of the differential output voltage	$\Delta\lvert V_{OD} \rvert$			0.2	V	Figure 5.6, R_L=100Ω or R_L=54Ω
Common-Mode Output Voltage	$\lvert V_{OC} \rvert$			3	V	Figure 5.6, R_L=100Ω or R_L=54Ω
Change in Magnitude of Common-Mode Voltage	$\Delta\lvert V_{OC} \rvert$			0.2	V	Figure 5.6, R_L=100Ω or R_L=54Ω
Driver Short-Circuit Output Current	I_{OSD}			250	mA	$0 \le V_{OUT} \le +12$ V
		-250			mA	$-7V \le V_{OUT} \le 5.5V$
Output Leakage Current (Y and Z) Full-Duplex	I_O			200	uA	DE=GND, VIN=12V
		-200			uA	DE=GND, VIN=-7V
Receiver						
Input Current (A and B)	I_A , I_B			200	uA	DE=GND, VDD_2=GND, V_{IN}=12V
		-200			uA	DE=GND, VDD_2=GND, V_{IN}=-7V
Receiver Differential Threshold Voltage	V_{TH}	-200	-125	-10	mV	$-7V \le V_{CM} \le 12V$
Receiver Input Hysteresis	ΔV_{TH}		15		mV	V_A+V_B=0
Receiver Input Resistance	R_{IN}	96			kΩ	$-7V \le V_{CM} \le 12V$, DE=low

5.2. NSIP83086 Switching Electrical Characteristics

(VDD=4.5V~5.5V,VDDL=1.8~5.5V, Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Driver						
Maximum Data Rate	f_{MAX}	16			Mbps	

Driver Propagation Delay	t_{PLH}		12	18	ns	See Figure 5.7, R_L=54Ω, C_L=50pF
	t_{PHL}		13.5	20.25	ns	See Figure 5.7, R_L=54Ω, C_L=50pF
Driver Pulse Width Distortion, $\|t_{PHL} - t_{PLH}\|$	PWD		1.5		ns	See Figure 5.7, R_L=54Ω, C_L=50pF
Driver Output Falling Time or Rising time	t_F		2.95	4.425	ns	See Figure 5.7, R_L=54Ω, C_L=50pF
	t_R		2.6	3.9	ns	See Figure 5.7, R_L=54Ω, C_L=50pF
Driver Enable to Output High	t_{ZH}		18.5	27.75	ns	See Figure 5.8, R_L=110Ω, C_L=50pF
Driver Enable to Output Low	t_{ZL}		19.1	28.65	ns	See Figure 5.8, R_L=110Ω, C_L=50pF
Driver Disable to Output High	t_{HZ}		20.8	31.2	ns	See Figure 5.8, R_L=110Ω, C_L=50pF
Driver Disable to Output Low	t_{LZ}		20.1	30.15	ns	See Figure 5.8, R_L=110Ω, C_L=50pF
Receiver						
Maximum Data Rate	f_{MAX}	16			Mbps	
Receiver Propagation Delay	t_{PLH}		16.2	24.3	ns	See Figure 5.9, C_L=15pF
	t_{PHL}		22.2	33.3	ns	See Figure 5.9, C_L=15pF
Receiver Pulse Width Distortion, $\|t_{PHL} - t_{PLH}\|$	PWD		6.0		ns	See Figure 5.9, C_L=15pF
Receiver Output Falling Time or Rising time	t_F		2.3	3.45	ns	See Figure 5.9, C_L=15pF
	t_R		2.1	3.15	ns	See Figure 5.9, C_L=15pF
Receiver Enable to Output High	t_{ZH}		13.8	20.7	ns	See Figure 5.10, R_L=1kΩ, C_L=15pF
Receiver Enable to Output Low	t_{ZL}		12.6	18.9	ns	See Figure 5.10, R_L=1kΩ, C_L=15pF

Receiver Disable to Output High	t_{HZ}		14	21	ns	See Figure 5.10, R_L=1kΩ, C_L=15pF
Receiver Disable to Output Low	t_{LZ}		13.4	20.1	ns	See Figure 5.10, R_L=1kΩ, C_L=15pF

5.3. Typical Performance Characteristics

Figure 5.1 NSiP83086 supply current vs Temperature

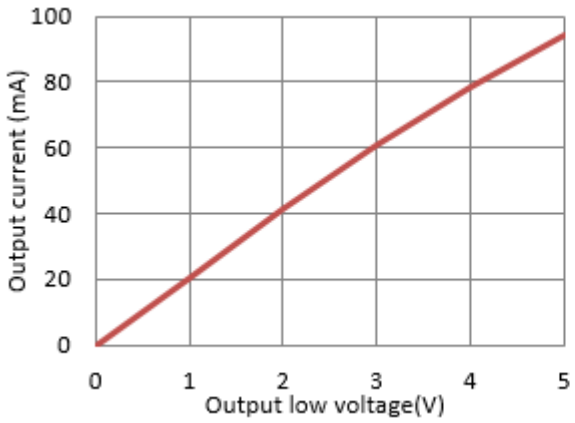


Figure5.2 Receiver output current vs Output low voltage

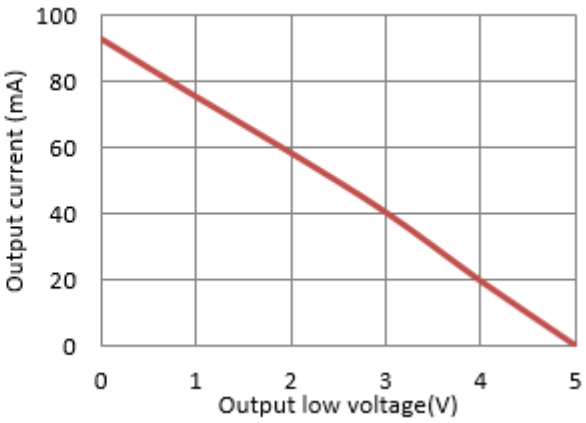


Figure 5.3 Receiver output current vs Output High voltage

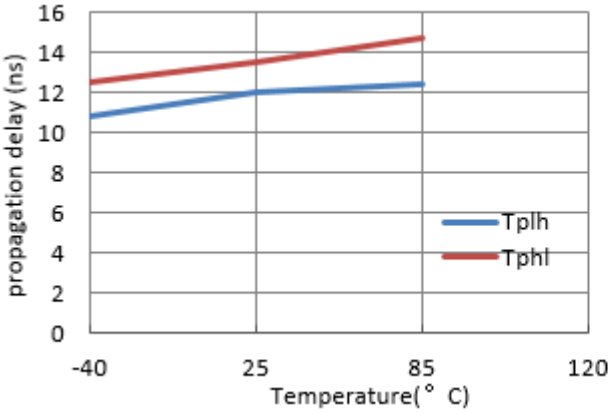


Figure 5.4 Transmitter Propagation Delay vs Temperature

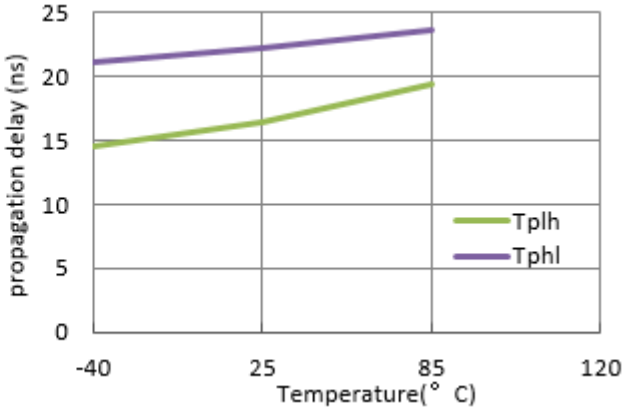


Figure 5.5 Receiver Propagation Delay vs Temperature

5.4. Parameter Measurement Information

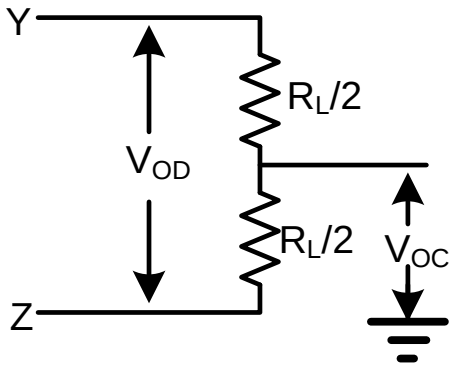


Figure 5.6 Driver DC Test Load

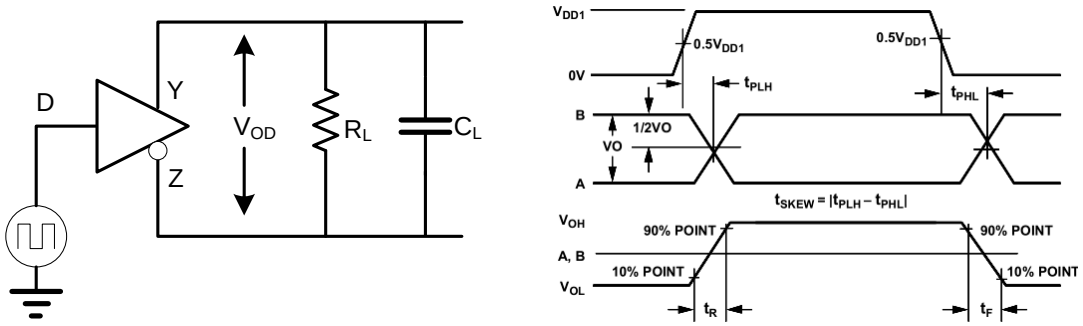


Figure5.7 Driver Timing Test Circuit and waveform

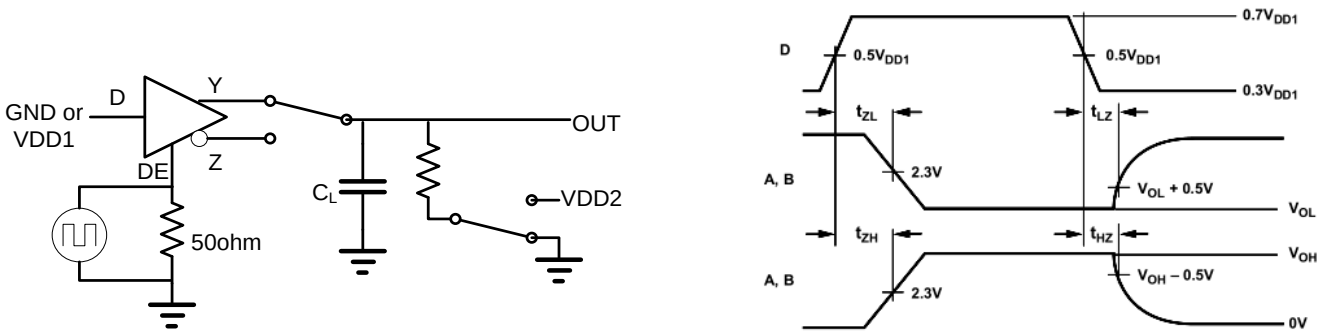


Figure5.8 Driver Enable Disable Timing Test Circuit and waveform

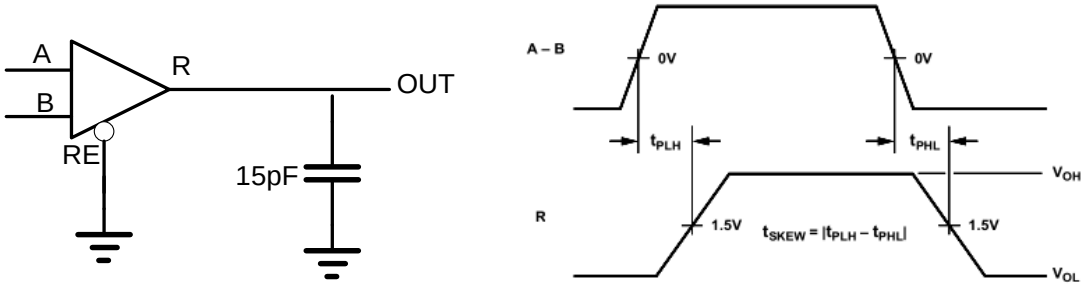


Figure 5.9 Receiver Propagation Delay Test Circuit and waveform

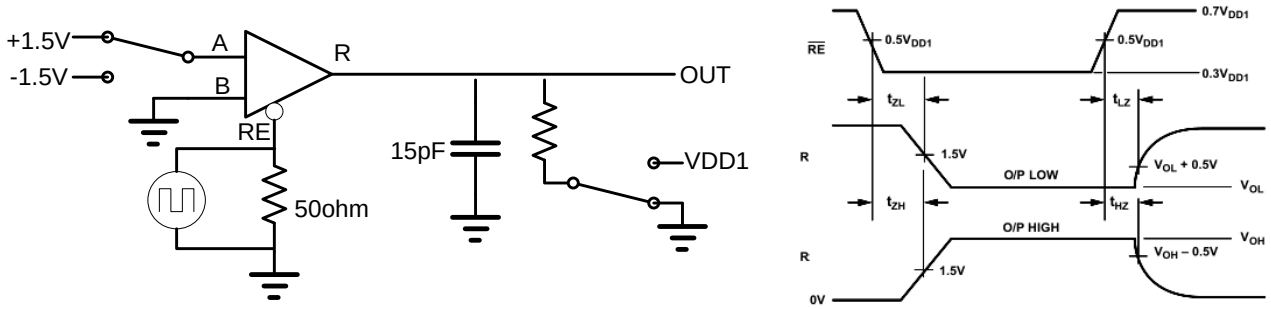


Figure 5.10 Receiver Enable Disable Timing Test Circuit and waveform

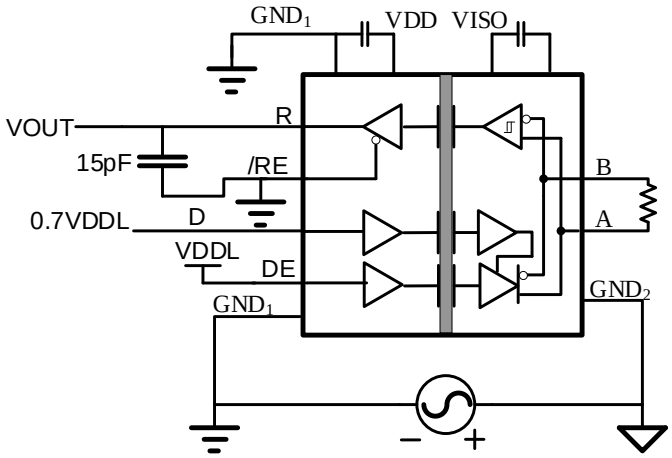


Figure5.11 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation And Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	L(I01)	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20	um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>400	**V**	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		Ⅱ		

6.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to IV	
For Rated Mains Voltage ≤ 400Vrms			I to IV	
Climatic Classification			10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive isolation voltage	AC Voltage(Bipolar)	V_{IORM}	1166	Vpeak
	AC Voltage(TDDB)	V_{IORM}	824	Vrms
	DC Voltage	V_{IORM}	1166	Vdc
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1749	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST}=1.3\times V_{IOSM}$	V_{IOSM}	4615	Vpeak
Isolation resistance	V_{IO} =500V	R_{IO}	$>10^9$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	pF
Input capacitance		C_I	2	pF
Total Power Dissipation at 25℃		Ps	1499	mW

Safety input, output, or supply current	θ_{JA} = 140 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	Is		mA
	θ_{JA} = 84 °C/W, V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C		237	mA
Case Temperature		Ts	150	℃

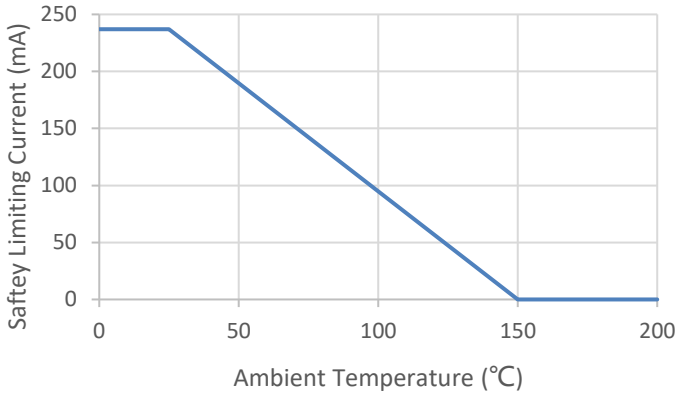


Figure 6.1 NSiP83086 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSiP83086 are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000Vrms Isolation voltage	Single Protection, 5000Vrms Isolation voltage	Basic Insulation 1166Vpeak, V_{IOSM}=4615Vpeak	Basic insulation at 800V_{RMS} (1166Vpeak) Reinforced insulation at 400V_{RMS} (565Vpeak)
File (pending)	File (pending)	File (pending)	File (pending)

[1] In accordance with UL 1577, each NSiP83086 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

[2] In accordance with DIN VDE V 0884-11, each NSi8100W/NSi8101W is proof tested by applying an insulation test voltage ≥ 1273 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

7. Function Description

NSiP83086 is a high reliability isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. Both devices are safety certified by UL1577 support 5kV_{RMS} insulation withstand voltages.

7.1. True Fail-Safe Receiver Inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (V_A-V_B) is greater than or equal to -10mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

7.2. Truth Tables[1]

Table 7.1 Driver Function Table

VDD status	*Input (D)*	*Enable Input (DE)*	*Outputs* *Y*	*Z*
PU	H	H	H	L
PU	L	H	L	H
PU	X	L	Z	Z
PU	X	OPEN	Z	Z
PU	OPEN	H	H	L
PD	X	X	Z	Z

Table 7.2 Reciever Function Table[1]

VDD status	*Differential Input (V_A-V_B)*	*Enable Input (/RE)*	*Output (R)*
PU	≥-10mV	L/Open	H
PU	≤-200mV	L/Open	L
PU	Open/Short	L/Open	H
PU	X	H	Z
PU	Idle	L	H
PD	X	X	Z

[1] PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance;

7.3. Emi Considerations

The NSiP83086 devices are using on chip transformer, so the power transfer must operate at high frequency allow higher efficiency transfer using the small transformer. This will cause emissions which need to pay attention to PCB layout if the application allow low emission. Please see the application note if needed.

7.4. Output Short And Over Temperature Protection

The NSiP83086 devices are protected against output short. When the devices detect the output is short, the device will be in Hiccup mode and the transfer power will be limited. So the temperature of the device will be low, and the device is protected.

The NSiP83086 devices are also protected against over temperature. When the devices detect the chip is over 165℃, the device will be shut down until the temperature of the device is below 145℃.

8. Application Note

8.1. 256 Transceivers On The Bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

8.2. ESD Protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly. The Bus pins have extra protection against static electricity to both the logic side (VDD1 side) and bus side (VDD2 side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ± 8kV HBM.
- ±10kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±6kV HBM.
- ±7kV using the Contact Discharge method specified in IEC 61000-4-2

8.3. Layout Considerations

The NSiP83086 requires a 10 µF bypass capacitor between VDD1 and GND1, 10uF bypass capacitor between VDD2 and GND2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end is terminated with a resistor, whose value matches the characteristic impedance of the cable. It's good practice to have the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

8.4. Typical Application

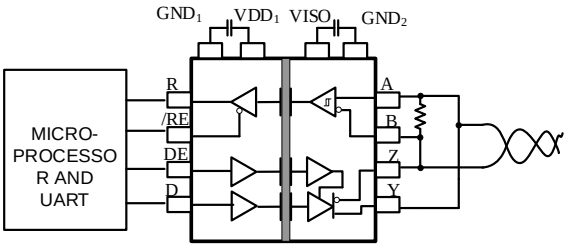


Figure 8.1 NSiP83086 use as Half-Duplex RS-485 application

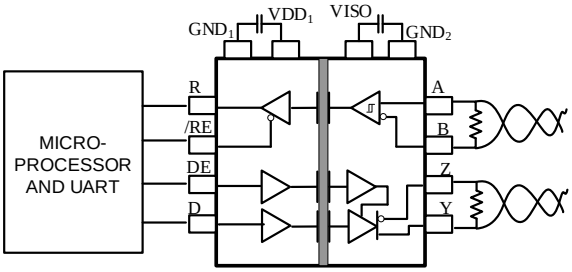


Figure 8.2 NSiP83086 typical application circuit

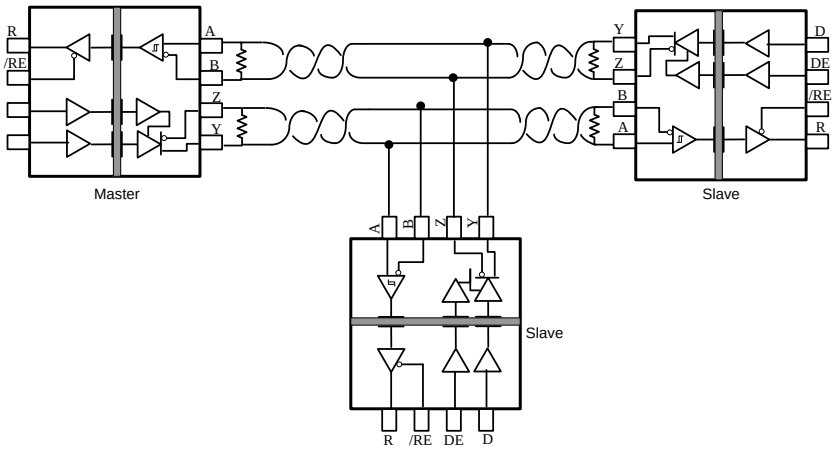
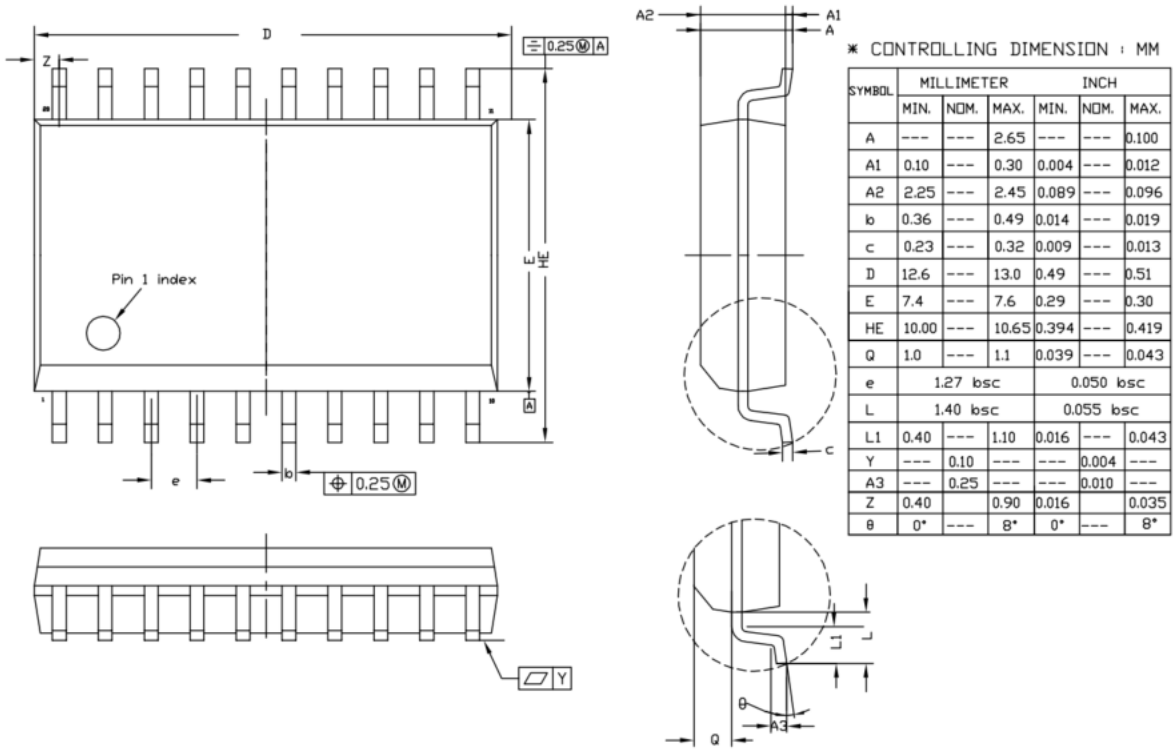


Figure 8.3 Typical isolated Full-Duplex RS-485 application

9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	2.65	---	---	0.100
A1	0.10	---	0.30	0.004	---	0.012
A2	2.25	---	2.45	0.089	---	0.096
b	0.36	---	0.49	0.014	---	0.019
c	0.23	---	0.32	0.009	---	0.013
D	12.6	---	13.0	0.49	---	0.51
E	7.4	---	7.6	0.29	---	0.30
HE	10.00	---	10.65	0.394	---	0.419
Q	1.0	---	1.1	0.039	---	0.043
e	1.27 bsc			0.050 bsc		
L	1.40 bsc			0.055 bsc		
L1	0.40	---	1.10	0.016	---	0.043
Y	---	0.10	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
Z	0.40		0.90	0.016		0.035
θ	0°	---	8°	0°	---	8°

Figure 9.1 SOW20 Package Shape and Dimension in millimeters

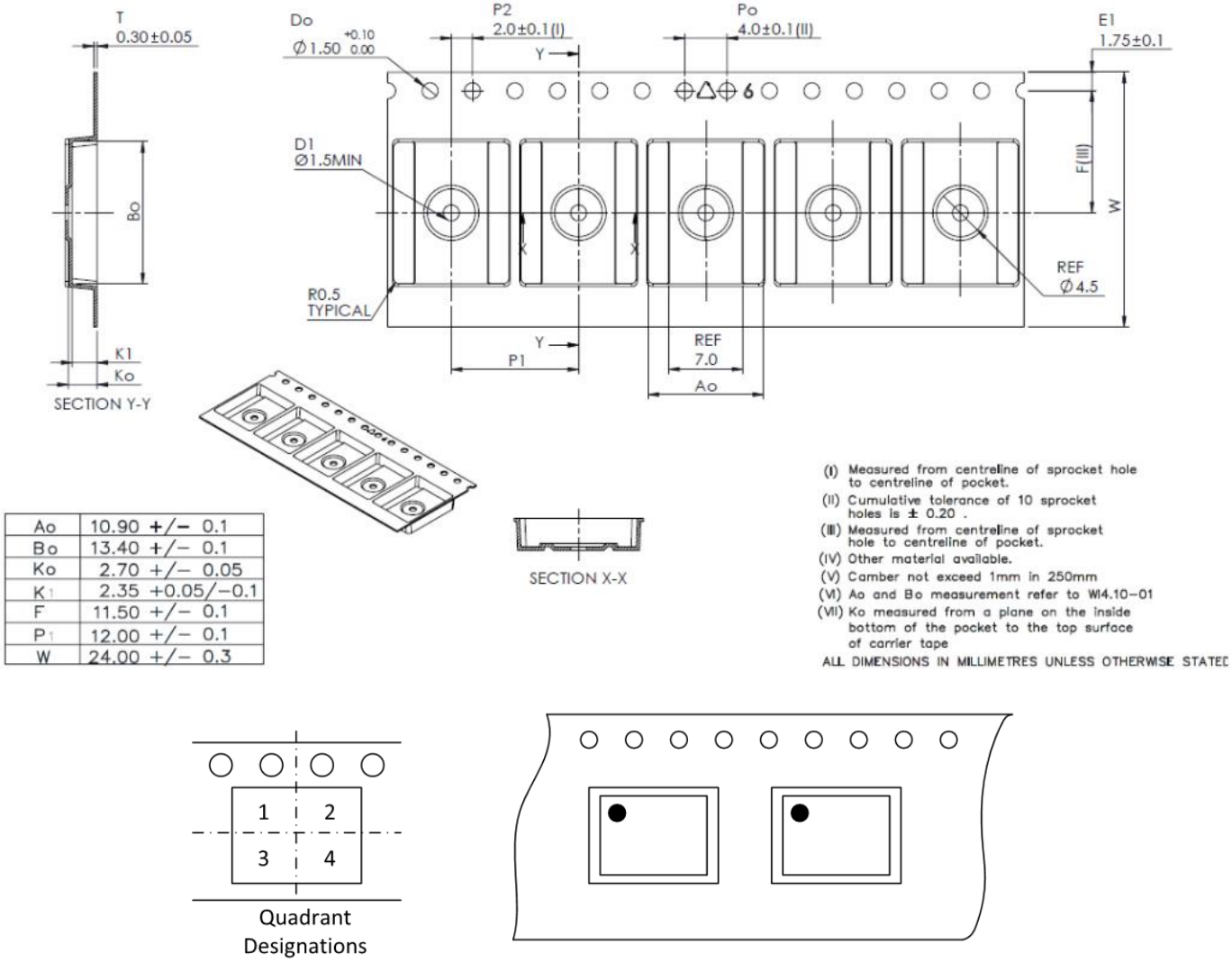
10. Order Information

Part No.	*Isolation Rating(kV_{RMS})*	*Duplex*	*Max Data Rate (Mbps)*	*MSL*	*Temperature*	*No. of Nodes*	*Package*	*SPQ*
NSiP83086-DSWTR	5	Full	16	2	-40 to 105℃	256	SOW20	1000
NOTE: All packages are Rhos-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.								

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSiP83086	Click here	Click here	Click here	Click here

12. Tape And Reel Information



Ao	10.90 +/− 0.1
Bo	13.40 +/− 0.1
Ko	2.70 +/− 0.05
K1	2.35 +0.05/−0.1
F	11.50 +/− 0.1
P1	12.00 +/− 0.1
W	24.00 +/− 0.3

Figure 12.1 Tape and Reel Information of SOW20

13. Revision History

Revision	Description	Date
0.0	Initial version	2021/3/28
0.1	Added MSL information	2021/4/19
0.2	Added VDDL information	2021/8/27
0.3	Removed NSIP83085 information	2021/9/15
0.4	Modified the body size info on 1st page	2021/11/2