

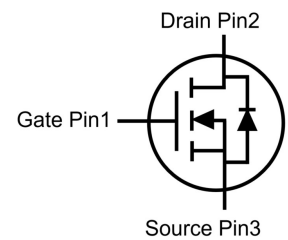
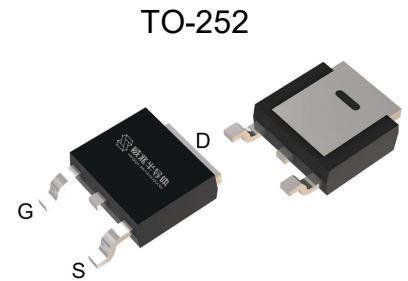
Features

- Enhancement mode
- VitoMOS® II Technology
- Fast Switching and High efficiency
- 100% Avalanche Tested



Halogen-Free

Part ID	Package Type	Marking	Packing
VSD011N10HS-G	TO-252	011N10H	2500pcs/Reel



Maximum ratings, at $T_A=25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
V_{GS}	Gate-Source voltage		± 25	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	55	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 25^\circ\text{C}$	55	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$ (Silicon limited)	$T_C = 100^\circ\text{C}$	39	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	220	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	7	A
		$T_A = 70^\circ\text{C}$	6	A
E_{AS}	Avalanche energy, single pulsed ②		49	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	73	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	1.3	W
T_{STG}, T_J	Storage and Junction Temperature Range		-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.05	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	120	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current(T _j =25°C)	V _{DS} =100V,V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current(T _j =125°C)	V _{DS} =100V,V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±25V,V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2.3	2.8	3.4	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =30A	--	12	16	mΩ
		(T _j =100°C)	--	15.5	--	mΩ
Dynamic Electrical Characteristics @ T _j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V,V _{GS} =0V, f=1MHz	1200	1600	2130	pF
C _{oss}	Output Capacitance		415	550	730	pF
C _{rss}	Reverse Transfer Capacitance		15	25	40	pF
R _g	Gate Resistance	f=1MHz	0.2	0.5	3	Ω
Q _g	Total Gate Charge	V _{DS} =50V,I _D =30A, V _{GS} =10V	--	24	32	nC
Q _{gs}	Gate-Source Charge		--	8.2	11	nC
Q _{gd}	Gate-Drain Charge		--	5.2	7.8	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =50V, I _D =30A, R _G =3Ω, V _{GS} =10V	--	10	--	ns
T _r	Turn-on Rise Time		--	27	--	ns
T _{d(off)}	Turn-Off Delay Time		--	17	--	ns
T _f	Turn-Off Fall Time		--	6	--	ns
Source- Drain Diode Characteristics@ T _j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =30A,V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time	I _{sd} =30A, V _{GS} =0V	--	37	74	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	36	72	nC

NOTE:

- ① Repetitive rating; pulse width limited by max junction temperature.
- ② Limited by T_{jmax}, starting T_j = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 14A, V_{GS} =10V. Part not recommended for use above this value
- ③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.
- ④ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

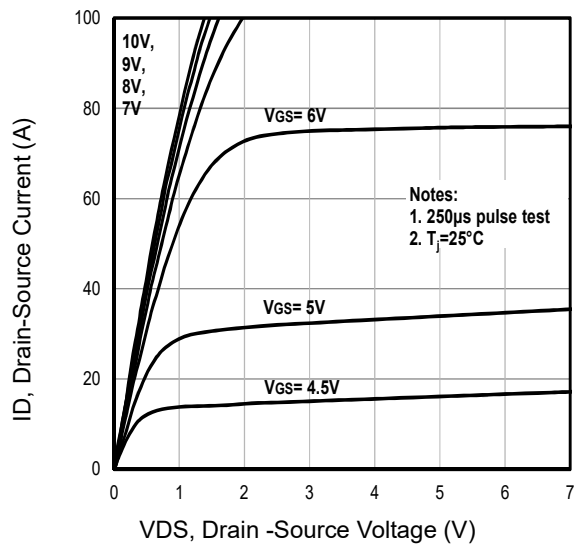


Fig1. Typical Output Characteristics

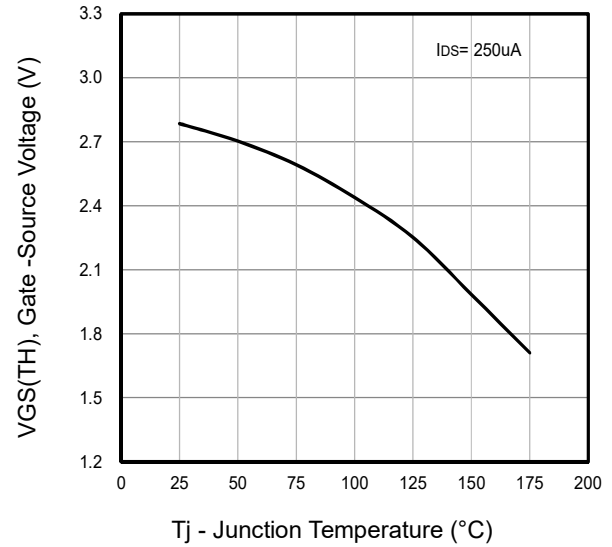


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

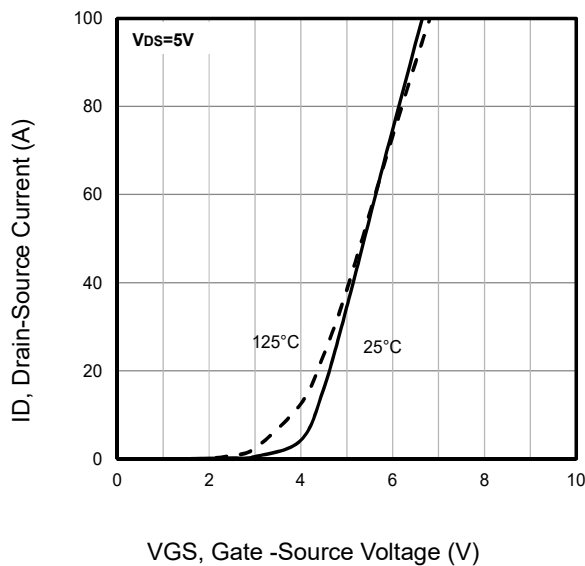


Fig3. Typical Transfer Characteristics

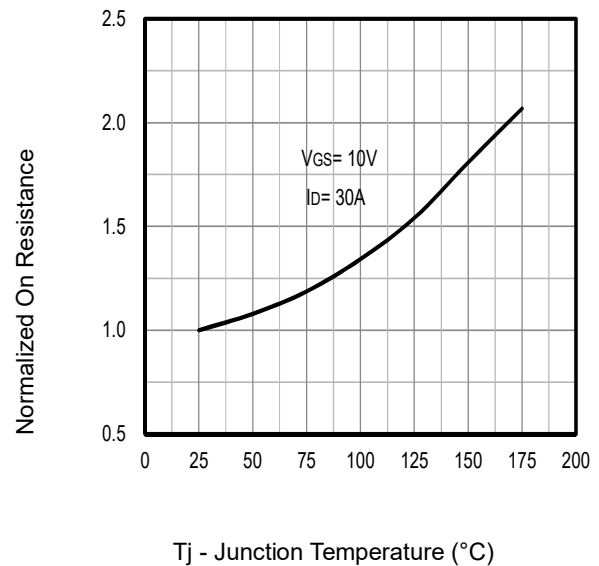


Fig4. Normalized On-Resistance Vs. Temperature

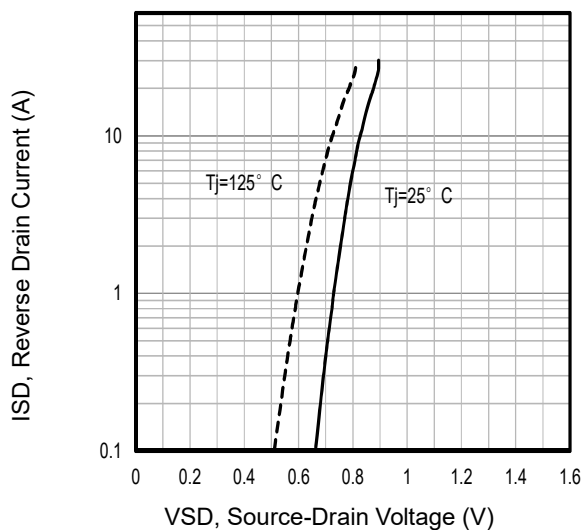


Fig5. Typical Source-Drain Diode Forward Voltage

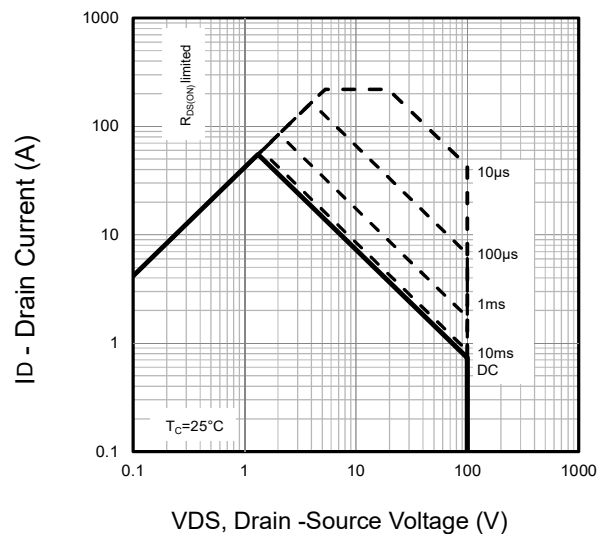


Fig6. Maximum Safe Operating Area

Typical Characteristics

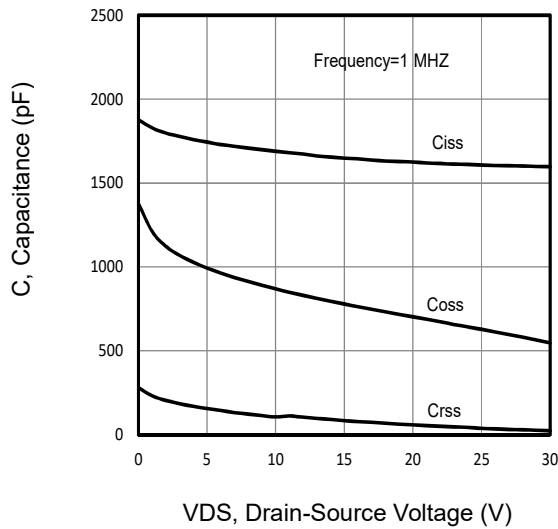


Fig7. Typical Capacitance Vs. Drain-Source Voltage

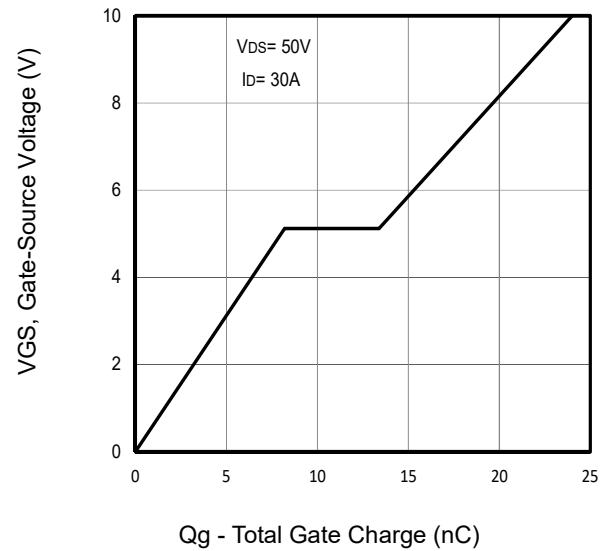


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

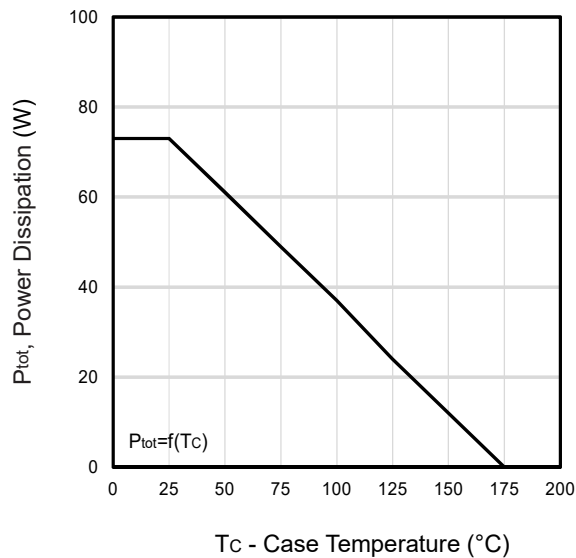


Fig9. Power Dissipation Vs. Case Temperature

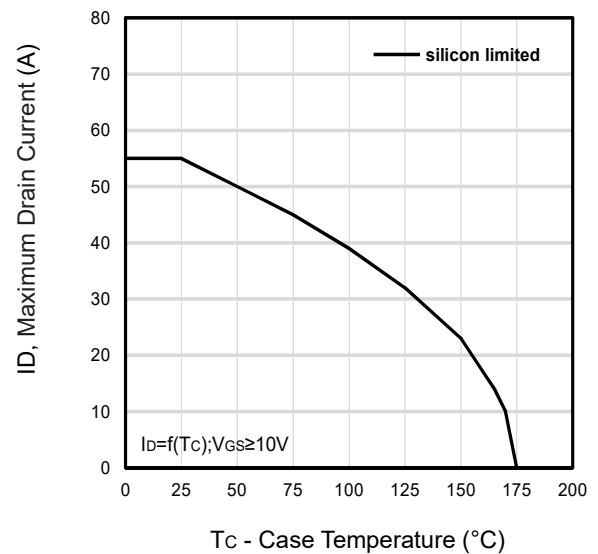


Fig10. Maximum Drain Current Vs. Case Temperature

Typical Characteristics

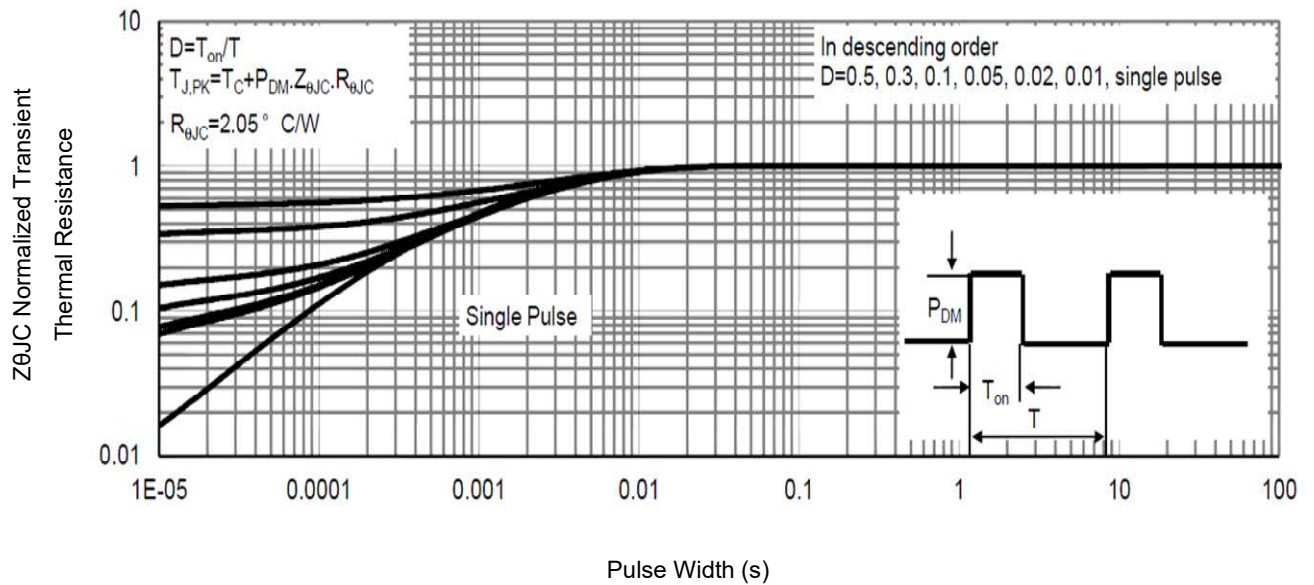


Fig11 . Normalized Maximum Transient Thermal Impedance

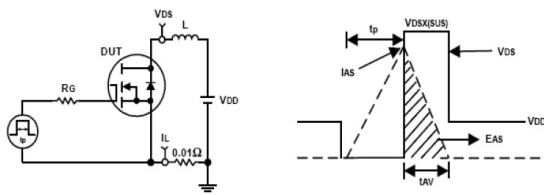


Fig12. Unclamped Inductive Test Circuit and waveforms

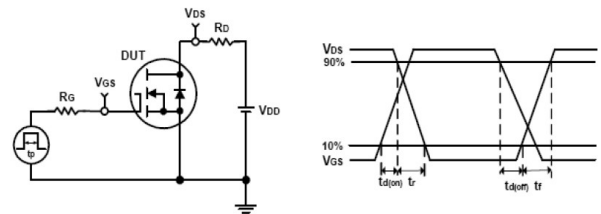
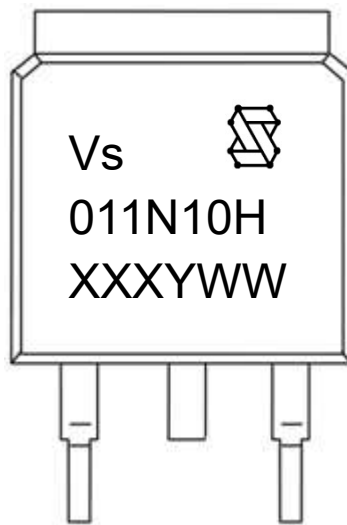


Fig13. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs), Vergiga Logo

2nd line: Part Number (011N10H)

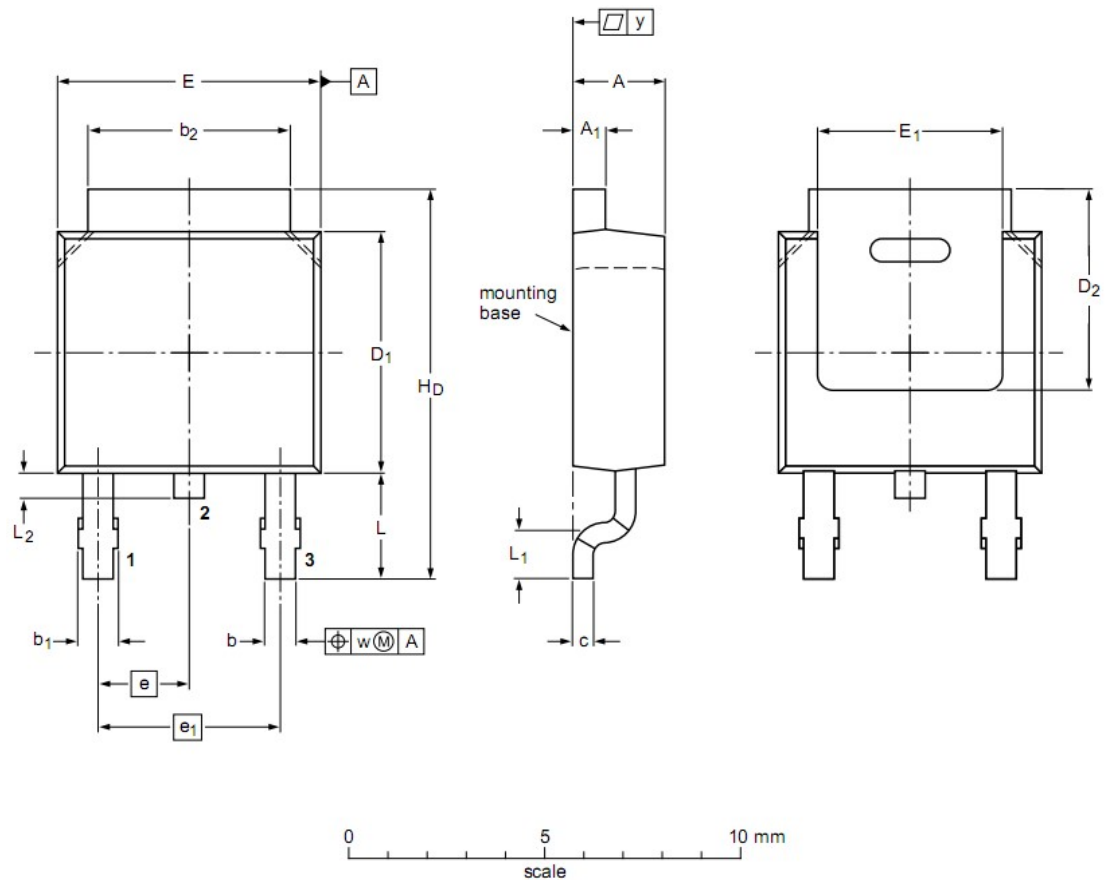
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TO-252 Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A₁	0.46	0.50	0.63
b	0.64	0.76	0.89
b₁	0.77	0.85	1.14
b₂	5.00	5.33	5.46
c	0.458	0.508	0.558
D₁	5.98	6.10	6.223
D₂	5.21	--	--
E	6.40	6.60	6.731
E₁	4.40	--	--
e	2.286 BSC		
e₁	--	4.57	--
H_D	9.40	10.00	10.40
L	2.743 REF		
L₁	1.40	1.52	1.77
L₂	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D₁" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

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