MC96F8204 Datasheet

CMOS Single-chip 8-bit MCU with 12-bit ADC, Flash 4KB, SRAM 256B

Version 1.12

Features

Core

- 8-bit CISC M8051 core
  (8051 Compatible, 2 clocks per cycle)

4 Kbytes On-Chip FLASH

- In-System Programming (ISP)
- Endurance: 10,000 times (Sector 0 – 119)
  100,000 times (Sector 120 – 127)
- Retention: 10 years

256 bytes IRAM

General Purpose I/O (GPIO)

- Normal I/O: 18 Ports (P0, P1, P2[1:0])

Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watch Dog Timer (WDT) 8-bit × 1-ch
  5kHz internal RC oscillator for WDT
- 8-bit × 1-ch (T0), 16-bit × 2-ch (T1/T2)

Programmable Pulse Generation

- Pulse generation (by T1/T2)

Watch Timer

- 3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz

USART

- 8-bit UART × 1-ch, 8-bit SPI × 1-ch

I2C

- 8-bit × 1-ch

12-bit A/D Converter

- 16 Input channels

16-bit CRC/Checksum Generator

- Auto and User CRC/Checksum mode

Power On Reset

- Reset release level (1.4V)

Low Voltage Reset

14 levels detect (1.60/ 2.05/ 2.15/ 2.25/ 2.37/ 2.50/ 2.65/ 2.82/ 3.01/ 3.22/ 3.47/ 3.76/ 4.10/ 4.51V)

Low Voltage Indicator

13 levels detect (2.05/ 2.15/ 2.25/ 2.37/ 2.50/ 2.65/ 2.82/ 3.01/ 3.22/ 3.47/ 3.76/ 4.10/ 4.51V)

Interrupt Sources

- External Interrupts (EINT0/1/10/11/12) (5)
- Timer (0/1/2) (3), WDT (1), BIT (1), WT (1)
- I2C (1)
- USART (2)
- ADC (1)

Internal RC Oscillator

- Low frequency: 200kHz ±3.0% (T_A= -20~ +85°C)
- High frequency: 8MHz ±2.0% (T_A= 0~ +50°C)

Power Down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- 1.8V to 5.5V (@32 to 38kHz with crystal)

- 1.8V to 5.5V (@0.4 to 4.2MHz with ceramic)
- 2.0V to 5.5V (@0.4 to 4.2MHz with crystal)
- 2.7V to 5.5V (@0.4 to 12MHz with crystal)
- 1.8V to 5.5V (@0.5 to 8MHz with HFIRC)
- 1.8V to 5.5V (@25 to 200kHz with LFIRC)
- Voltage dropout converter included for core

Minimum Instruction Execution Time

- 167ns (@12MHz main clock)
- 61us (@ 32.768kHz sub clock)

Operating Temperature

- –40 ~ +85℃

Package Type

- 20 SOP/TSSOP
- 16 SOPN/QFN
- 10 SSOP
- 8 SOP
- Pb-free package

Product selection table

Table 1. Device Summary

Part number	Flash	IRAM	ADC	I/O	Package
MC96F8204D	4 Kbytes	256 bytes	8 inputs	18	20 SOP
MC96F8204R	4 Kbytes	256 bytes	8 inputs	18	20 TSSOP
MC96F8204M	4 Kbytes	256 bytes	8 inputs	14	16 SOPN
MC96F8204U	4 Kbytes	256 bytes	8 inputs	14	16 QFN
MC96F8104S	4 Kbytes	256 bytes	8 inputs	8	10 SSOP
MC96F8104M	4 Kbytes	256 bytes	6 inputs	6	8 SOP

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1 Description

MC96F8204 is an advanced CMOS 8-bit microcontroller with 4 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost-effective solution to many embedded control applications.

Table 2 introduces features of MC96F8204 and peripheral counts. In addition, MC96F8204 supports power down modes to reduce power consumption.

1.1 Device overview

Table 2. MC96F8204 Device Features and Peripheral Counts

Peripheral / Device		MC96F8204
CPU		8-bit CISC core (M8051, 2 clocks per cycle)
Flash		• 4 Kbytes with self r/w capability • On chip debug and ISP • Endurance: 10,000 cycles (Sector 0 – 119), 100,000 cycles (Sector 120 – 127) • Retention: 10 years
IRAM		256 bytes
GPIO		• Normal I/O 18 ports: P0, P1, P2[1:0]
Timer/ counter		• BIT 8-bit x 1-ch • WDT 8-bit x 1-ch: 5 kHz internal RC oscillator for WDT • 8-bit x 1-ch (T0) • 16-bit x 2-ch (T1/T2)
Programmable pulse generation		• Pulse generation (T1/T2)
Watch Timer		3.91ms/0.25s/0.5s/1s/1min interval at 32.768kHz
ADC		12-bit ADC, 8 input channels
Reset	Power on reset	Reset release level (1.4V)
	Low voltage reset	14 level detect (1.60V/ 2.05V/ 2.15V/ 2.25V/ 2.37V/ 2.50V/ 2.65V/ 2.82V/ 3.01V/3.22V/ 3.47V/ 3.76V/ 4.10V/ 4.51V)
LVI		13 level detect (2.05V/ 2.15V/ 2.25V/ 2.37V/ 2.50V/ 2.65V/ 2.82V/ 3.01V/3.22V/ 3.47V/ 3.76V/ 4.10V/ 4.51V)
USART		• 8-bit UART x 1-ch, 8-bit SPI x 1-ch
I2C		• 8-bit x 1-ch
Interrupt sources		• External interrupts: EINT0/1/10/11/12, 5 • Timer0/1/2, 3 • WT 1 • WDT 1 • BIT 1

	• USART 2 • ADC 1 • I2C, 1
Internal RC oscillator	• Low frequency: 200kHz ± 3.0% (T_A = -20℃ to +85℃) • High frequency: 8MHz ± 2.0% (T_A = 0℃ to +50℃)

Table 2. MC96F8204 Device Features and Peripheral Counts (continued)

Peripheral	MC96F8204
Power down mode	STOP, IDLE
Operating voltage and frequency	• 1.8V to 5.5V @ 32 to 38kHz with crystal • 1.8V to 5.5V @ 0.4 to 4.2MHz with ceramic • 2.0V to 5.5V @ 0.4 to 4.2MHz with crystal • 2.7V to 5.5V @ 0.4 to 12.0MHz with crystal • 1.8V to 5.5V @ 0.5 to 8.0MHz with HFIRC • 1.8V to 5.5V @ 25 to 200kHz with LFIRC • Voltage dropout converter included for core
Minimum instruction execution time	• 167ns @ 12 MHz main clock • 61us @ 32.768kHz sub clock
Operating temperature	-40℃ to +85℃
Oscillator Type	• 0.4-12MHz Crystal or Ceramic for main clock • 32.768kHz Crystal for sub clock
Package type	• 20 SOP/TSSOP • 16 SOPN/QFN • 10 SSOP • 8 SOP • Pb-free package

1.2 Block diagram

Figure 1 describes MC96F8204 in a block diagram.

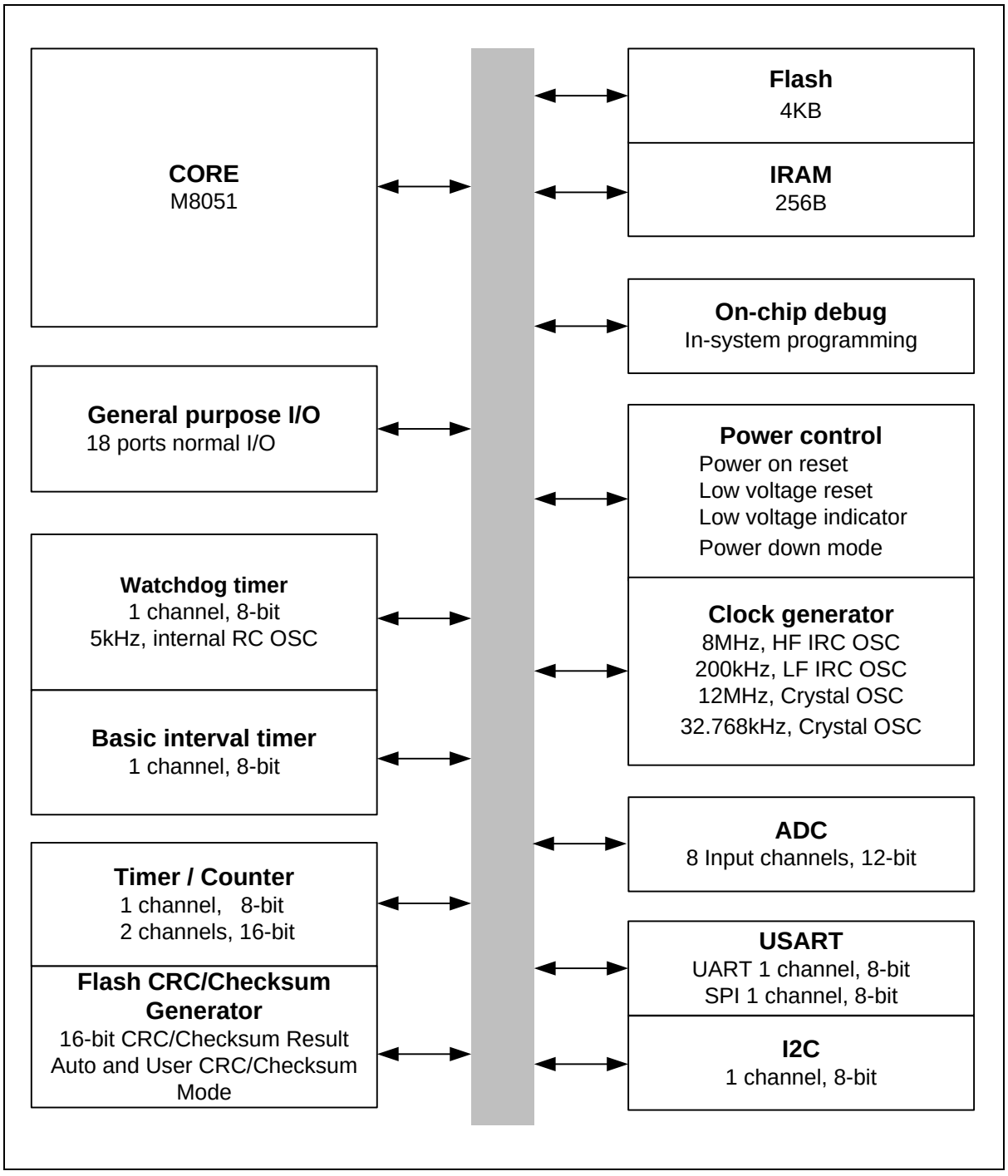
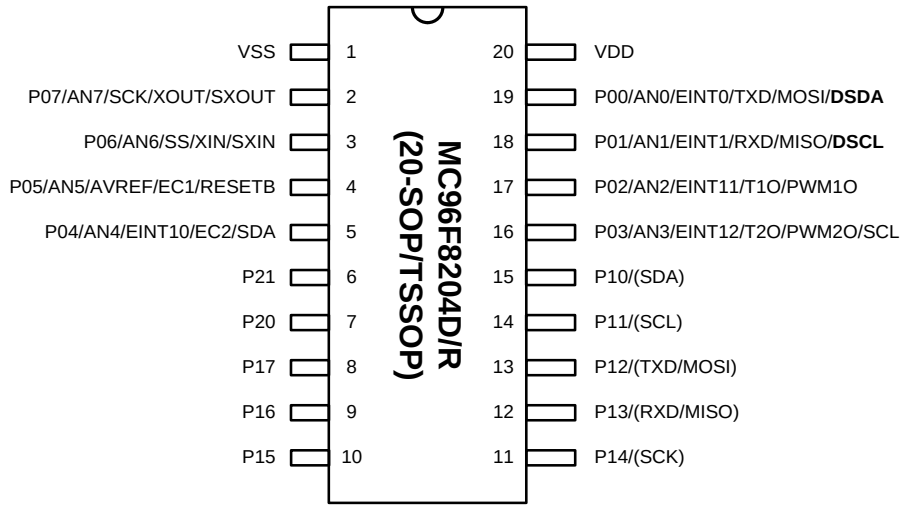


Figure 1. MC96F8204 Block Diagram

2 Pinouts and pin descriptions

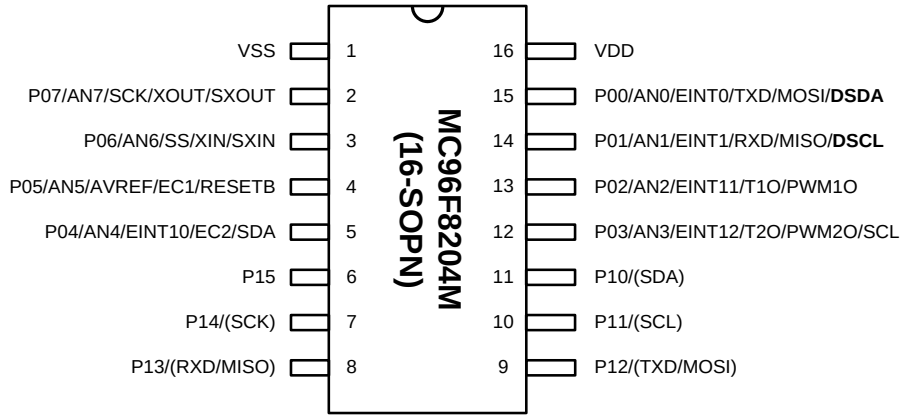
In this chapter, MC96F8204 pinouts and pin descriptions are introduced.

2.1 Pinouts



NOTE: For the On-Chip Debugging, ISP assigns P0[0:1] pins for DSCL and DSDA respectively.

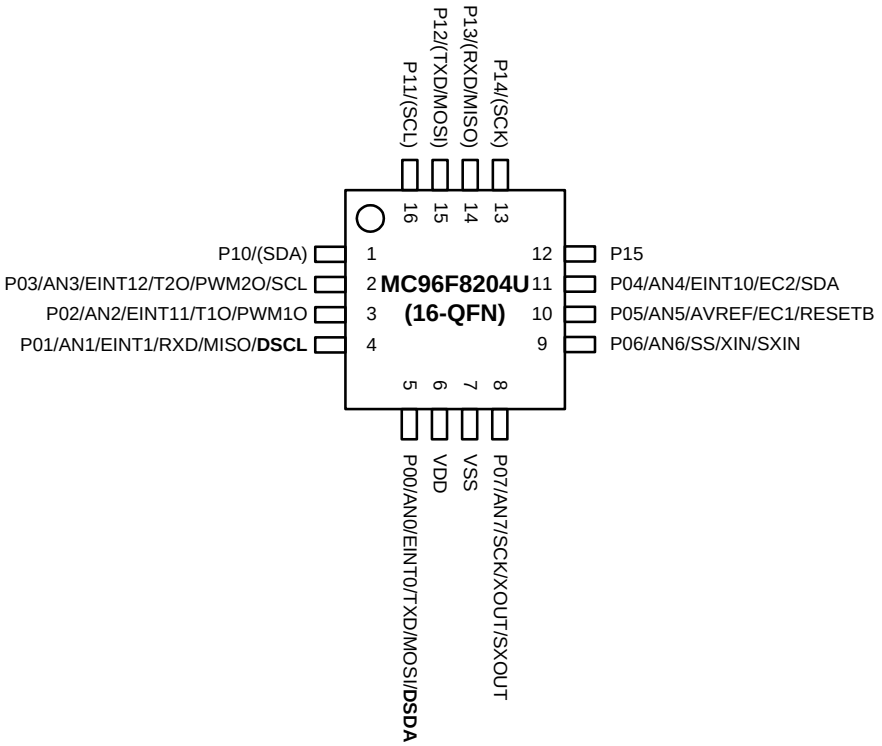
Figure 2. MC96F8204D/R 20 SOP/TSSOP Pinouts



NOTES:

1. For the On-Chip Debugging, ISP assigns P0[0:1] pins for DSCL and DSDA respectively.
2. The P16-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16-pin package is used

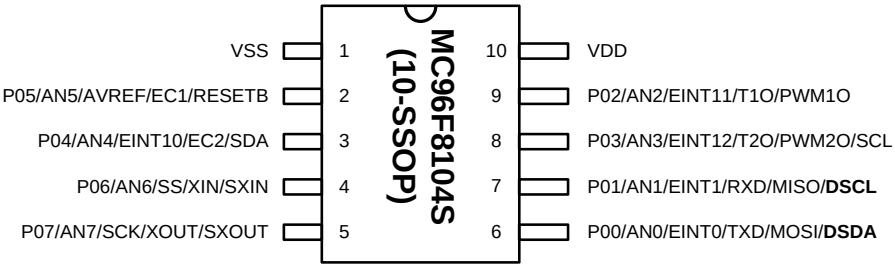
Figure 3. MC96F8204M 16 SOPN Pinouts



NOTES:

1. For the On-Chip Debugging, ISP assigns P0[0:1] pins for DSCL and DSDA respectively.
2. The P16-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16-pin package is used.

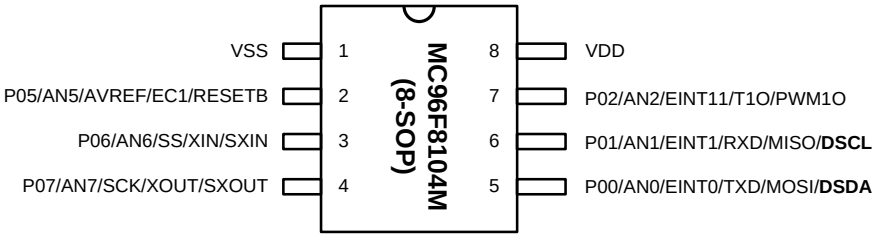
Figure 4. MC96F8204U 16 QFN Pinouts



NOTES:

1. For the On-Chip Debugging, ISP assigns P0[0:1] pins for DSCL and DSDA respectively.
2. The P10-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 10-pin package is used.

Figure 5. MC96F8104S 10 SSOP Pinouts



NOTES:

1. For the On-Chip Debugging, ISP assigns P0[0:1] pins for DSCL and DSDA respectively.
2. The P03-P04, P10-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 8-pin package is used.

Figure 6. MC96F8104M 8 SOP Pinouts

2.2 Pin description

Table 3. Normal Pin Description

Pin name	I/O	Function	@reset	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P03-P04 are not in the 8-Pin package.	Input	AN0/EINT0/TXD/MOSI/DSDA
P01				AN1/EINT1/RXD/MISO/DSCL
P02				AN2/EINT11/T1O/PWM1O
P03				AN3/EINT12/T2O/PWM2O/SCL
P04				AN4/EINT10/EC2/SDA
P05				AN5/AVREF/EC1/RESETB
P06				AN6/SS/XIN/SXIN
P07				AN7/SCK/XOUT/SXOUT
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P10-P17 are not in the 10-Pin/8-Pin package. The P16-P17 are not in the 16-Pin package.	Input	(SDA)
P11				(SCL)
P12				(TXD/MOSI)
P13				(RXD/MISO)
P14				(SCK)
P15				–
P16				–
P17				–
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-	Input	–
P21				–

		pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20-P21 are not in the 16-Pin/10-Pin/8-Pin package.		

Table 3. Normal Pin Description (continued)

Pin name	I/O	Function	@reset	Shared with
EINT0	I/O	External interrupt input	Input	P00/AN0/TXD/MOSI/DSDA
EINT1		External interrupt input		P01/AN1/RXD/MISO/DSCL
EINT10	I/O	External interrupt input and Timer 0 capture input	Input	P04/AN4/EC2/SDA
EINT11	I/O	External interrupt input and Timer 1 capture input		P02/AN2/T1O/PWM1O
EINT12	I/O	External interrupt input and Timer 2 capture input		P03/AN3/T2O/PWM2O/SCL
T1O	I/O	Timer 1 interval output	Input	P02/AN2/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P03/AN3/EINT12/PWM2O/SCL
PWM1O	I/O	Timer 1 PWM output	Input	P02/AN2/EINT11/T1O
PWM2O	I/O	Timer 2 PWM output	Input	P03/AN3/EINT12/T2O/SCL
EC1	I/O	Timer 1 event count input	Input	P05/AN5/AVREF/RESETB
EC2	I/O	Timer 2 event count input	Input	P04/AN4/EINT10/SDA
SCK	I/O	Serial clock input/output	Input	P07/AN7/XOUT/SXOUT
MOSI	I/O	SPI master output, slave input	Input	P00/AN0/EINT0/TXD/DSDA (P12)
MISO	I/O	SPI master input, slave output	Input	P01/AN1/EINT1/RXD/DSCL (P13)
SS	I/O	SPI slave select input	Input	P06/AN6/XIN/SXIN
TXD	I/O	UART data output	Input	P00/AN0/EINT0/MOSI/DSDA (P12)
RXD	I/O	UART data input	Input	P01/AN1/EINT1/MISO/DSCL (P13)
SCL	I/O	I2C clock input/output	Input	P03/AN3/EINT12/T2O/PWM2O (P11)
SDA	I/O	I2C data input/output	Input	P04/AN4/EINT10/EC2 (P10)

RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION.	Input	P05/AN5/AVREF/EC1
AVREF	I/O	A/D converter reference voltage	Input	P05/AN5/EC1/RESETB
AN0	I/O	A/D converter analog input channels	Input	P00/EINT0/TXD/MOSI/DSDA
AN1				P01/EINT1/RXD/MISO/DSCL
AN2				P02/EINT11/T1O/PWM1O
AN3				P03/EINT12/T2O/PWM2O/SCL
AN4				P04/EINT10/EC2/SDA
AN5				P05/AVREF/EC1/RESETB
AN6				P06/SS/XIN/SXIN
AN7				P07/SCK/XOUT/SXOUT

Table 3. Normal Pin Description (continued)

Pin name	I/O	Function	@reset	Shared with
DSCL	I/O	On chip debugger clock input	Input	P01/AN1/EINT1/RXD/MISO
DSDA	I/O	On chip debugger data input/output	Input	P00/AN0/EINT0/TXD/MOSI
XIN	I/O	Main oscillator pins	Input	P06/AN6/SS/SXIN
XOUT	I/O			P07/AN7/SCK/SXOUT
SXIN	I/O	Sub oscillator pins	Input	P06/AN6/SS/XIN
SXOUT	I/O			P07/AN7/SCK/XOUT
VDD, VSS	–	Power input pins	–	–

NOTES:

1. The P16-P17 and P20-P21 are not in the 16-Pin package.
2. The P10-P17 and P20-P21 are not in the 10-Pin package.
3. The P03-P04, P10-P17 and P20-P21 are not in the 8-Pin package.
4. The P05/RESETB pin is configured as one of the P05 and the RESETB pin by the “CONFIGURE OPTION”.
5. If the P00/AN0/EINT0/TXD/MOSI/DSDA and P01/AN1/EINT1/RXD/MISO/DSCL pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
6. The P00/AN0/EINT0/TXD/MOSI/DSDA and P01/AN1/EINT1/RXD/MISO/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
7. The P06/XIN/SXIN and P07/XOUT/SXOUT pins are configured as a function pin by software control.

3 Port structures

3.1 GPIO port structure

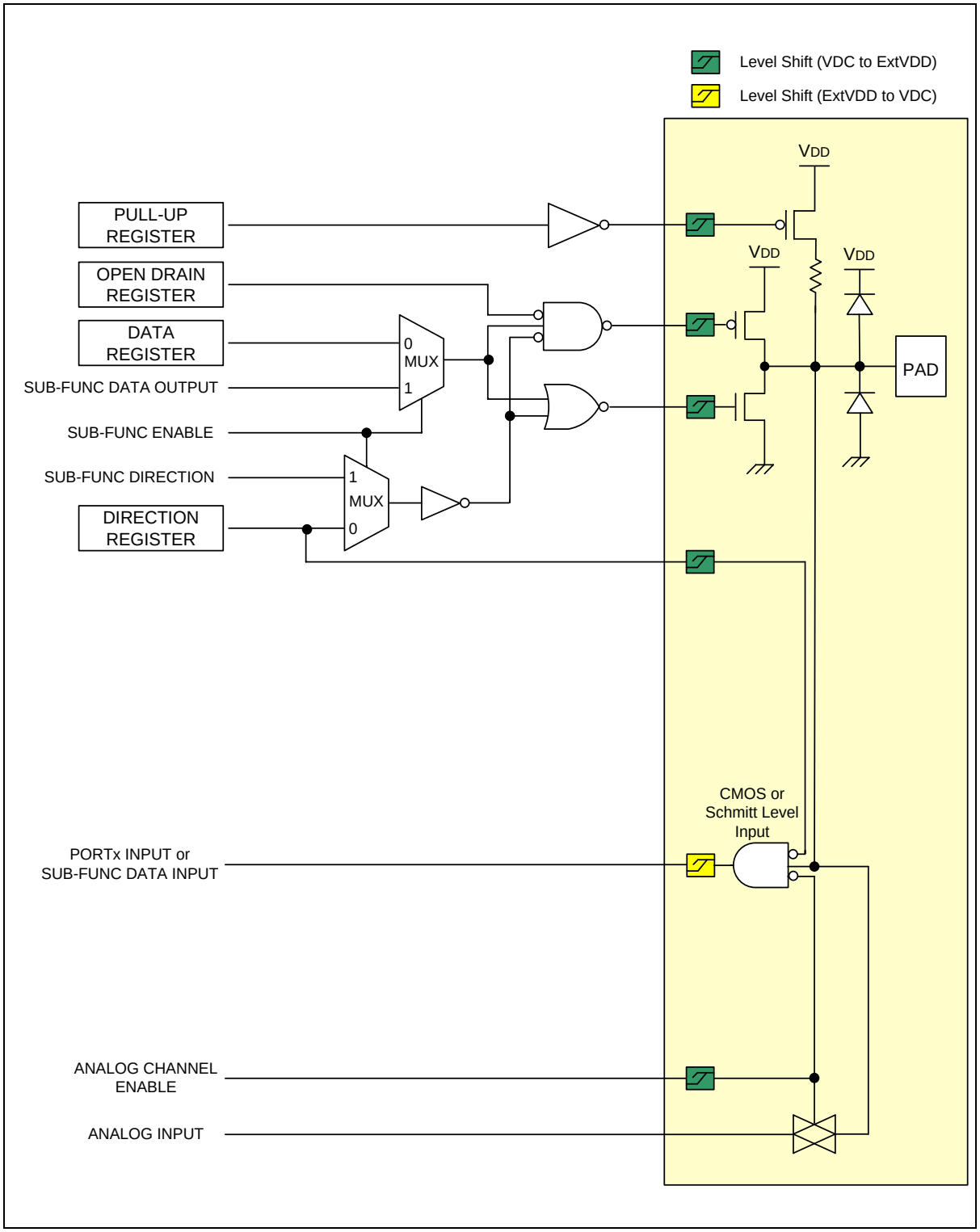


Figure 7. General Purpose I/O Port Structure

3.2 External interrupt I/O port structure

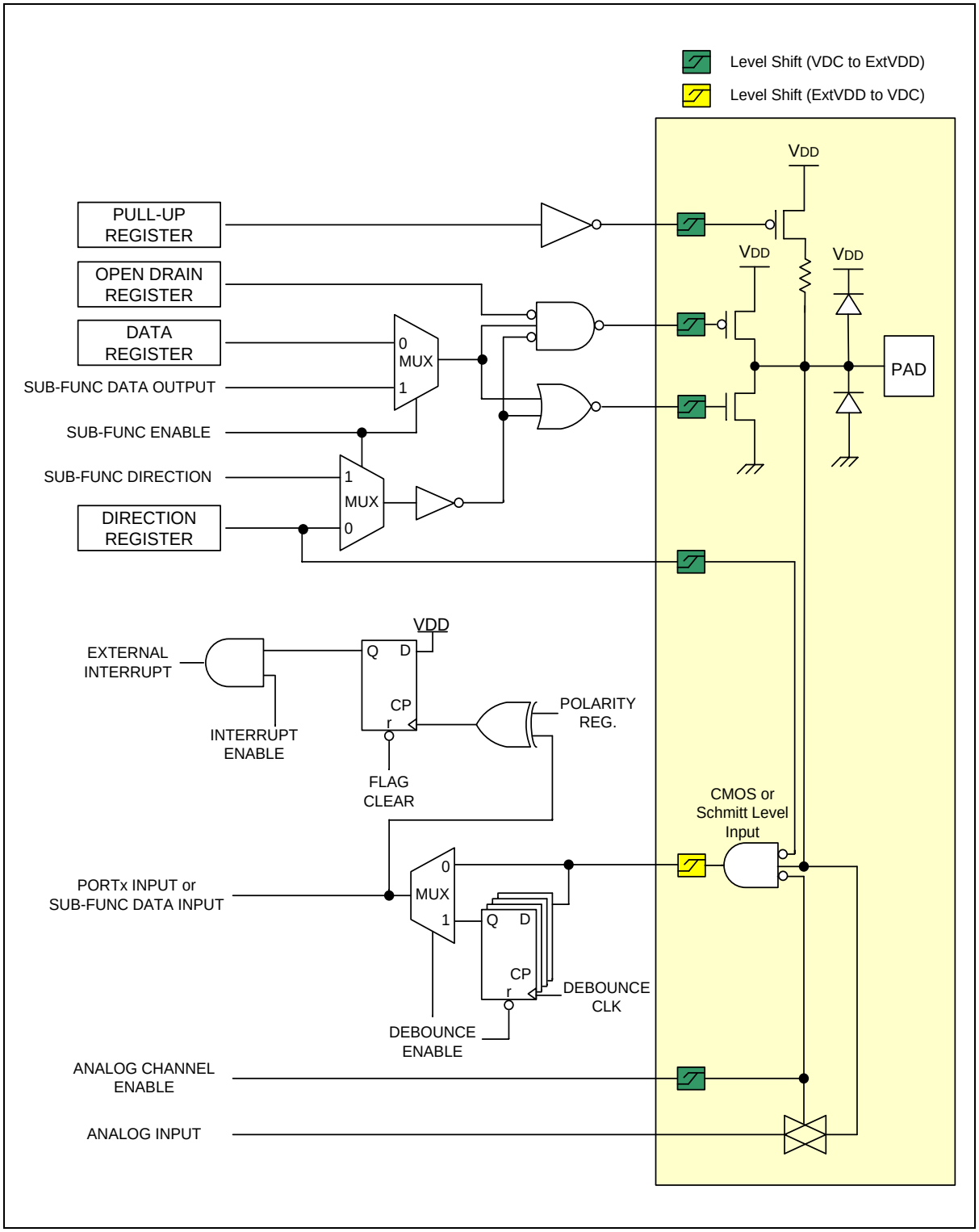


Figure 8. External Interrupt I/O Port Structure

4 Memory organization

MC96F8204 addresses three separate memory spaces:

- Program memory
- Data memory
- XRAM memory

By means of this logical separation of the memory, 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

MC96F8204 provides on-chip 4 Kbytes of the ISP type flash program memory, which is readable and writable. Internal data memory (IRAM) is 256 bytes and it includes the stack area.

4.1 Program memory

A 16-bit program counter is capable of addressing up to 64 Kbytes, but MC96F8204 has only 4 Kbytes program memory space. After reset, CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 11 is assigned to location 000BH. If the external interrupt 11 is going to be used, its service routine must begin at location 000BH. If the interrupt is not going to be used, its service location is available as general-purpose program memory. If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8-byte interval.

A longer service routine can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use. Figure 9 shows a map of the lower part of the program memory.

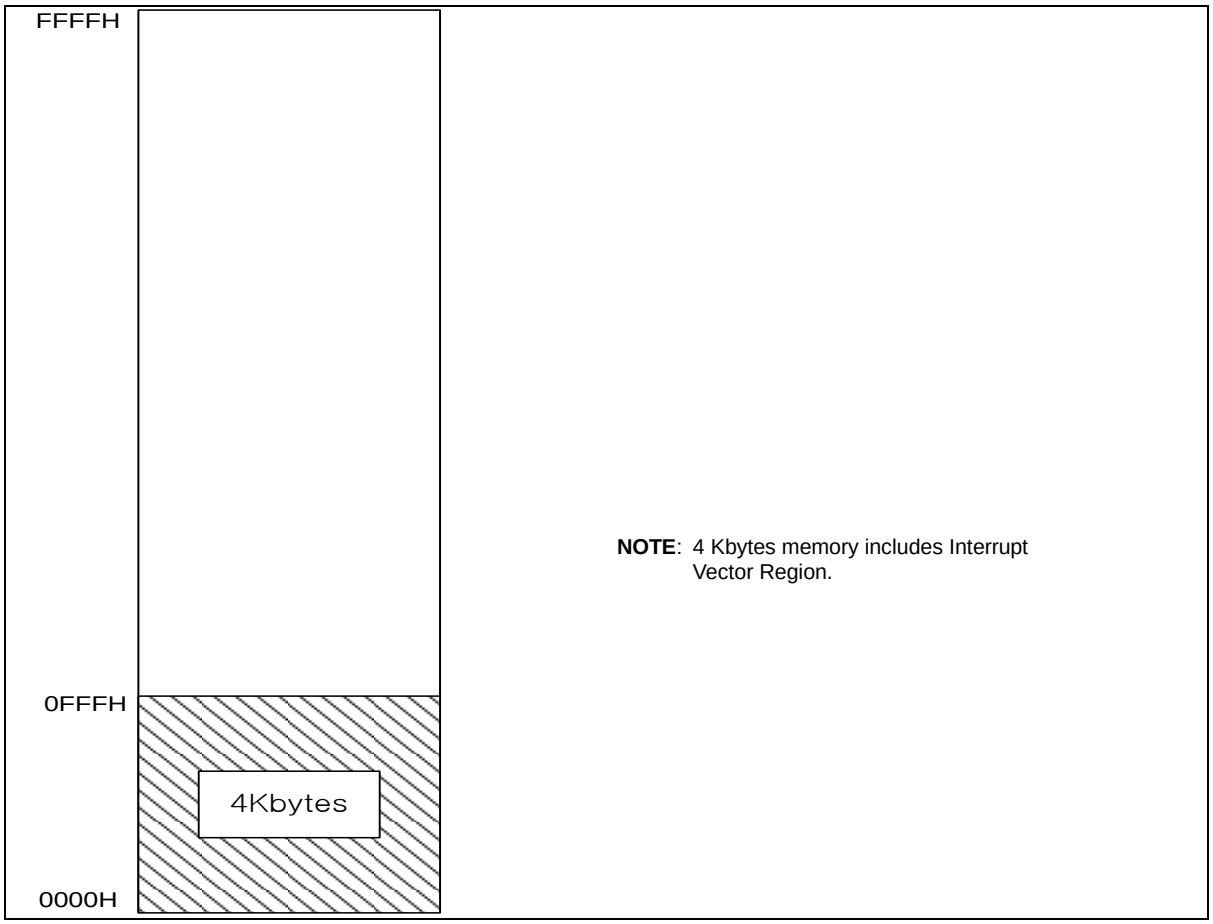


Figure 9. Program Memory

More detailed description of program memory is introduced in chapter 19. Flash memory later part in this document.

4.2 Internal data memory

Internal data memory is divided into three spaces as shown in figure 10. Those three spaces are generally called as,

- Lower 128 bytes
- Upper 128 bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256 bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. By means of this method, the upper 128 bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in figure 10.

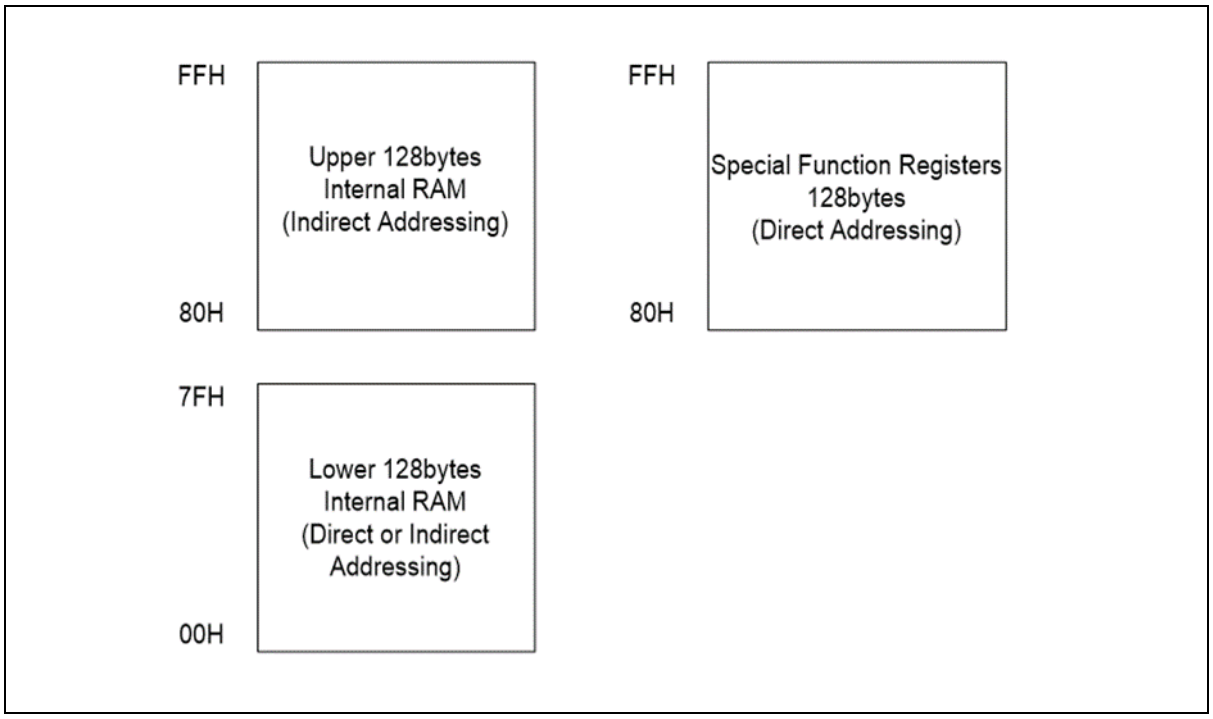


Figure 10. Internal Data Memory Map

The lower 128 bytes of RAM are present in all 8051 devices as mapped in figure 11. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128 bytes can be accessed by either direct or indirect addressing, while the upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

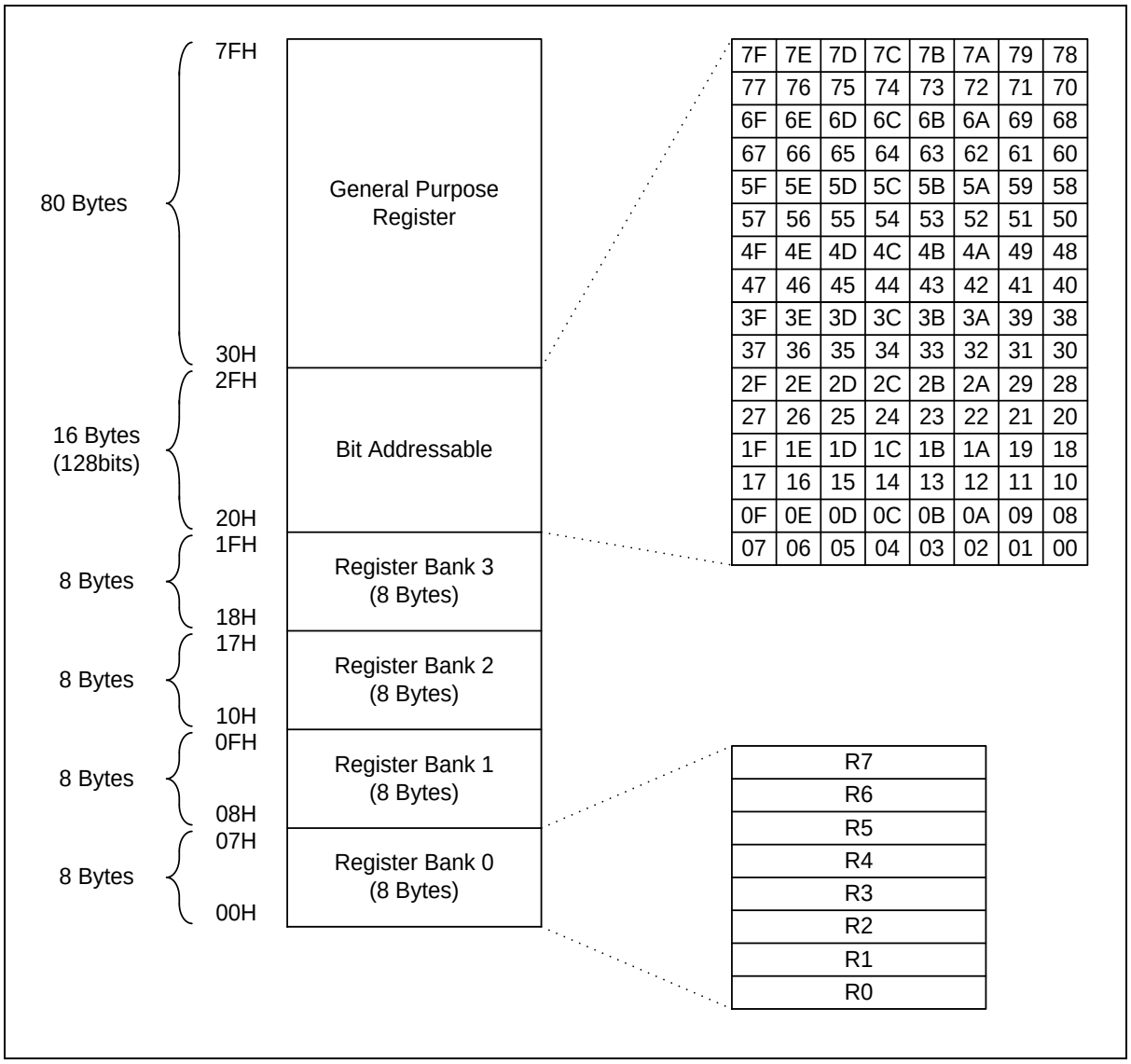


Figure 11. Lower 128 bytes Internal RAM

4.3 Extended SFR area

Extended SFR area has no relation with RAM nor FLASH. This area can be read or written to by using SFR in 8-bit unit.

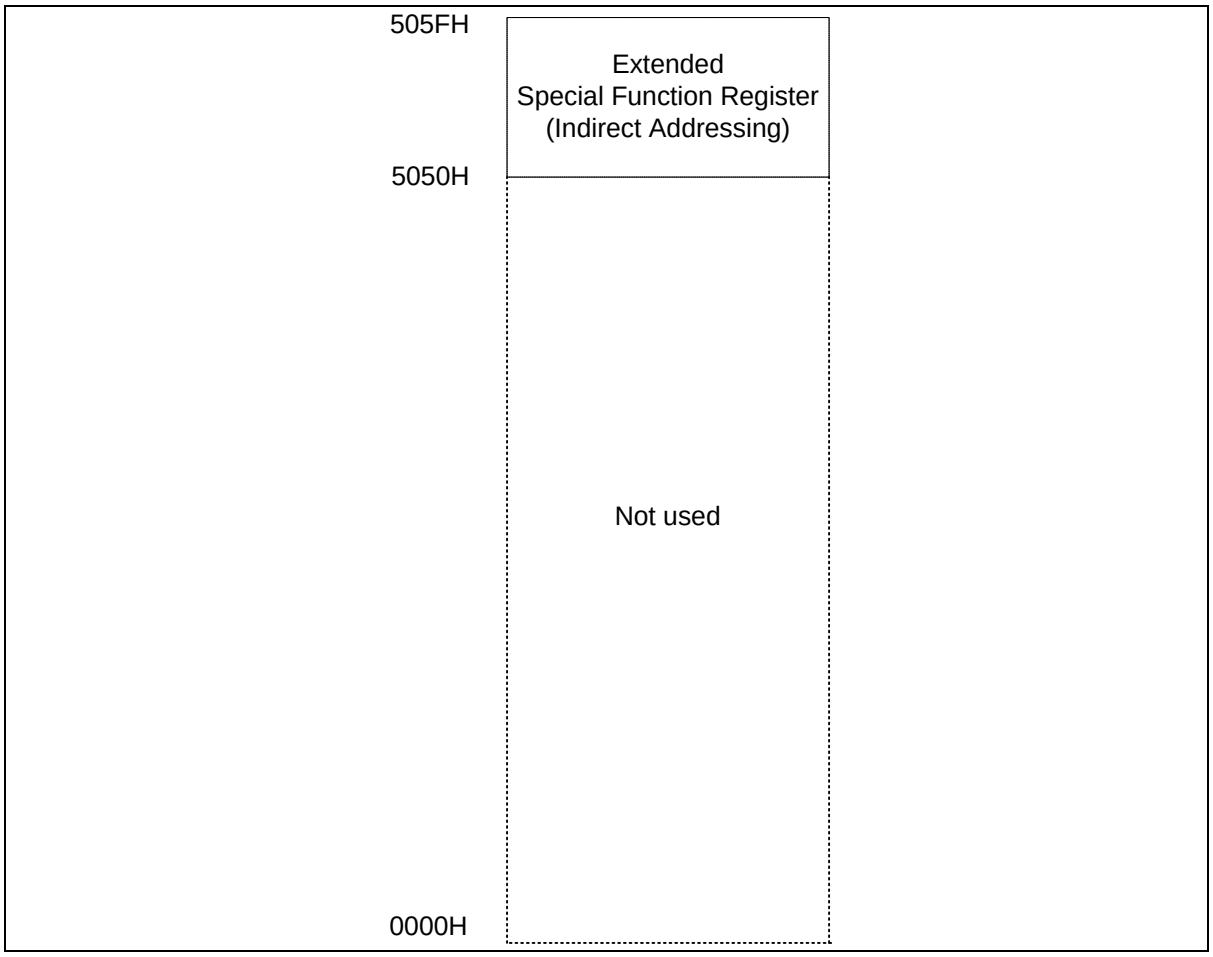


Figure 12. Extended SFR (XSFR) Area

4.4 SFR map

In this section, information of SFR map and map summaries are introduced through table 4 to 7.

4.4.1 SFR map summary

Table 4. SFR Map Summary

– Reserved M8051 compatible

	00H/8H[NOTE]	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	–
0F0H	B	I2CSAR1	–	–	–	–	–	–
0E8H	RSTFR	I2CCR	I2CSR	I2CSAR0	I2CDR	I2CSDHR	I2CSCLR	I2CSCHR
0E0H	ACC	–	–	–	–	–	–	–
0D8H	LVRCR	USTCR1	USTCR2	USTCR3	USTST	USTBD	USTDR	–
0D0H	PSW	–	–	–	–	–	–	FCDIN
0C8H	OSCCR	LIFSR	–	–	–	–	ADCDRL	ADCDRH
0C0H	EIFLAG	–	–	–	P2	P2IO	P2PU	P2OD
0B8H	IP	–	–	–	–	–	–	XTFLSR
0B0H	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH	–	–
0A8H	IE	IE1	IE2	IE3	P1	P1IO	P1PU	P1OD
0A0H	ADCCRL	ADCCRH	EO	–	EIPOL0	EIPOL1	–	P1FSR
98H	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH	WTCR	WTDR/ WTCNT
90H	T0CR	T0CNT	T0DR/ T0CDR	P0PU	P0OD	P0DB	P0FSRL	P0FSRH
88H	P0IO	–	SCCR	BITCR	BITCNT	WDTCR	WDTDR/ WDTCNT	P0FSRM
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTE: Registers 00H/8H are bit-addressable.

4.4.2 Extended SFR map summary

Table 5. XSFR Map Summary

– Reserved

	00H/8H	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
5058H	FCDRL	–	–	–	–	–	–	–
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH

4.4.3 SFR map

Table 6. SFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
80H	P0 Data Register	P0	R/W	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	–	–	–	–	–	–	0	0
88H	P0 Direction Register	P0IO	R/W	0	0	0	0	0	0	0	0
89H	reserved	–	–	–							
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0
8BH	Basic Interval Timer Control Register	BITCR	R/W	0	0	0	–	0	0	0	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0
8DH	Watch Dog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0
8EH	Watch Dog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1
8EH	Watch Dog Timer Counter Register	WDTCNT	R	0	0	0	0	0	0	0	0
8FH	P0 Function Selection Middle Register	P0FSRM	R/W	–	–	–	–	0	0	0	0
90H	Timer 0 Control Register	T0CR	R/W	0	–	0	–	0	0	0	0
91H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0
92H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1
92H	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0
93H	P0 Pull-up Resistor Selection Register	P0PU	R/W	0	0	0	0	0	0	0	0
94H	P0 Open-drain Selection Register	P0OD	R/W	0	0	0	0	0	0	0	0
95H	P0 Debounce Enable Register	P0DB	R/W	0	0	–	0	0	0	0	0
96H	P0 Function Selection Low Register	P0FSRL	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
97H	P0 Function Selection High Register	P0FSRH	R/W	–	–	–	0	0	0	0	0
98H	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	0	0	0	0
99H	Timer 1 Control High Register	T1CRH	R/W	0	–	0	0	–	–	–	0
9AH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1
9BH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1
9CH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1
9DH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1
9EH	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0
9FH	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1
9FH	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0
A0H	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0
A1H	A/D Converter Control High Register	ADCCRH	R/W	0	–	–	–	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0
A3H	Reserved	–	–	–							
A4H	External Interrupt Polarity 0 Register	EIPOL0	R/W	–	–	–	–	0	0	0	0
A5H	External Interrupt Polarity 1 Register	EIPOL1	R/W	–	–	0	0	0	0	0	0
A6H	Reserved	–	–	–							
A7H	P1 Function Selection Register	P1FSR	R/W	–	–	–	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	–	–	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	–	0	–
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	–	–	0	0	0	–
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	–	0	0	0	–	0
ACH	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0
ADH	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0
AEH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0
AFH	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
B0H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	0	0	0	0
B1H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	0
B2H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1
B3H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1
B4H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1
B5H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1
B6H	Reserved	–	–	–							
B7H	Reserved	–	–	–							
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0
B9H	Reserved	–	–	–							
BAH	Reserved	–	–	–							
BBH	Reserved	–	–	–							
BCH	Reserved	–	–	–							
BDH	Reserved	–	–	–							
BEH	Reserved	–	–	–							
BFH	X-tal Filter Selection Register	XTFLSR	R/W	0	0	0	0	0	0	0	0
C0H	External Interrupt Flag Register	EIFLAG	R/W	–	0	0	0	0	0	0	0
C1H	Reserved	–	–	–							
C2H	Reserved	–	–	–							
C3H	Reserved	–	–	–							
C4H	P2 Data Register	P2	R/W	–	–	–	–	–	–	0	0
C5H	P2 Direction Register	P2IO	R/W	–	–	–	–	–	–	0	0
C6H	P2 Pull-up Resistor Selection Register	P2PU	R/W	–	–	–	–	–	–	0	0
C7H	P2 Open-drain Selection Register	P2OD	R/W	–	–	–	–	–	–	0	0
C8H	Oscillator Control Register	OSCCR	R/W	0	–	0	0	1	0	0	0
C9H	LFIRC Frequency Selection Register	LIFSR	R/W	0	0	0	0	0	–	0	0
CAH	Reserved	–	–	–							
CBH	Reserved	–	–	–							
CCH	Reserved	–	–	–							
CDH	Reserved	–	–	–							
CEH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x
CFH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–							
D2H	Reserved	–	–	–							
D3H	Reserved	–	–	–							
D4H	Reserved	–	–	–							
D5H	Reserved	–	–	–							
D6H	Reserved	–	–	–							
D7H	Flash CRC Data In Register	FCDIN	R/W	0	0	0	0	0	0	0	0
D8H	Low Voltage Reset Control Register	LVRCR	R/W	0	–	–	0	0	0	0	0
D9H	USART Control Register 1	USTCR1	R/W	0	0	0	0	0	0	0	0
DAH	USART Control Register 2	USTCR2	R/W	0	0	0	0	0	0	0	0
DBH	USART Control Register 3	USTCR3	R/W	0	0	0	0	0	0	0	0
DCH	USART Status Register	USTST	R/W	1	0	0	0	0	0	0	0
DDH	USART Baud Rate Generation Register	USTBD	R/W	1	1	1	1	1	1	1	1
DEH	USART Data Register	USTDR	R/W	0	0	0	0	0	0	0	0
DFH	Reserved	–	–	–							
E0H	Accumulator Register	ACC	R/W	0	0	0	0	0	0	0	0
E1H	Reserved	–	–	–							
E2H	Reserved	–	–	–							
E3H	Reserved	–	–	–							
E4H	Reserved	–	–	–							
E5H	Reserved	–	–	–							
E6H	Reserved	–	–	–							
E7H	Reserved	–	–	–							
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	0	x	–	–	–
E9H	I2C Control Register	I2CCR	R/W	0	0	0	0	0	0	0	0
EAH	I2C Status Register	I2CSR	R/W	0	0	0	0	0	0	0	0
EBH	I2C Slave Address 0 Register	I2CSAR0	R/W	0	0	0	0	0	0	0	0
ECH	I2C Data Register	I2CDR	R/W	0	0	0	0	0	0	0	0
EDH	I2C SDA Hold Time Register	I2CSDHR	R/W	0	0	0	0	0	0	0	1
EEH	I2C SCL Low Period Register	I2CSCLR	R/W	0	0	1	1	1	1	1	1
EFH	I2C SCL High Period Register	I2CSCHR	R/W	0	0	1	1	1	1	1	1

Table 6. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	I2C Slave Address 1 Register	I2CSAR1	R/W	0	0	0	0	0	0	0	0
F2H	Reserved	-	-	-							
F3H	Reserved	-	-	-							
F4H	Reserved	-	-	-							
F5H	Reserved	-	-	-							
F6H	Reserved	-	-	-							
F7H	Reserved	-	-	-							
F8H	Interrupt Priority Register 1	IP1	R/W	-	-	0	0	0	0	0	0
F9H	Reserved	-	-	-							
FAH	Flash Sector Address High Register	FSADRH	R/W	-	-	-	-	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	-	-	-	-	0	0	0
FFH	Reserved	-	-	-							

4.4.4 Extended SFR map

Table 7. XSFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
5050H	Flash CRC Start Address High Register	FCSARH	R/W	–	–	–	–	–	–	–	0
5051H	Flash CRC End Address High Register	FCEARH	R/W	–	–	–	–	–	–	–	0
5052H	Flash CRC Start Address Middle Register	FCSARM	R/W	0	0	0	0	0	0	0	0
5053H	Flash CRC End Address Middle Register	FCEARM	R/W	0	0	0	0	0	0	0	0
5054H	Flash CRC Start Address Low Register	FCSARL	R/W	0	0	0	0	–	–	–	–
5055H	Flash CRC End Address Low Register	FCEARL	R/W	0	0	0	0	1	1	1	1
5056H	Flash CRC Control Register	FCCR	R/W	0	0	–	–	0	0	0	0
5057H	Flash CRC Data High Register	FCDRH	R	1	1	1	1	1	1	1	1
5058H	Flash CRC Data Low Register	FCDRL	R	1	1	1	1	1	1	1	1
5059H	Reserved	–	–	–							
505AH	Reserved	–	–	–							
505BH	Reserved	–	–	–							
505CH	Reserved	–	–	–							
505DH	Reserved	–	–	–							
505EH	Reserved	–	–	–							
505FH	Reserved	–	–	–							

5 Ports

5.1 I/O ports

MC96F8204 has three groups of I/O ports, P0 ~ P2. Each port can be easily configured as an input pin, an output, or an internal pull up and open-drain pin by software. The port configuration pursues to meet various system configurations and design requirements. P0 ~ P2 have a function generating interrupts in accordance with a change of state of the pin.

5.2 Port registers

5.2.1 Data register (Px)

Data register (Px) is related to a bidirectional I/O port. If a port is configured as an output port, data can be written to the corresponding bit of the Px. If a port is configured as an input, data can be read from the corresponding bit of the Px.

5.2.2 Direction register (PxIO)

Each I/O pin can be used as an input or an output independently by setting a PxIO register. If a bit is cleared in this read/write register, the corresponding pin of Px will be an input. While setting bits in this register will configure the corresponding pins to output.

Most bits are cleared by a system reset, but some bits are set by the system reset.

5.2.3 Pull-up register selection register (PxPU)

On-chip pull-up resistors can be connected to I/O ports individually by configuring a pull-up resistor selection register (PxPU). Setting a PxPU register can enable or disable a pull-up resister of each port. If a certain bit in PxPU register is 1, a pull-up resister of the corresponding pin is enabled. While the bit is 0, the pull-up resister is disabled. All bits are cleared by a system reset.

5.2.4 Open-drain selection register (PxOD)

There are internal open-drain selection registers (PxOD) for P0. Setting a PxOD register can enable or disable an open-drain of each port.

Most ports become push-pull by a system reset, but some ports become open-drain by the system reset.

5.2.5 Debounce enable register (P0DB)

P0[4:0] support a debounce function. Debounce clocks of the ports are fx/1, fx/4, fx/32, and fx/4096 respectively.

5.2.6 Port function selection register (P0FSRH, P0FSRM, P0FSRL, P1FSR)

Port function selection registers define alternative functions of ports. Please remember that these registers must be set properly for alternative port functions. A reset clears the P0FSRH, P0FSRM, P0FSRL, P1FSR register to '00H', which makes all pins to normal I/O ports.

6 Interrupt controller

Up to 15 interrupt sources are available in the MC96F8204. Allowing software control, each interrupt source can be enabled by defining separate enable register bit associated with it. It can also have four levels of priority assigned. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources and is not controllable by software.

The interrupt controller features the followings:

- Receives requests from 15 interrupt sources
- 6 group priority
- 4 priority levels
- Multi interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit
- Interrupt latency varies ranging from 3 to 9 machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupts enable registers (IE, IE1, IE2, IE3). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control. It must be set to '1' to enable interrupts as introduced in the followings:

- When EA is set to '0' ➔ all interrupts are disabled.
- When EA is set to '1' ➔ a particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

EA is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. MC96F8204 supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of the four levels according to IP and IP1.

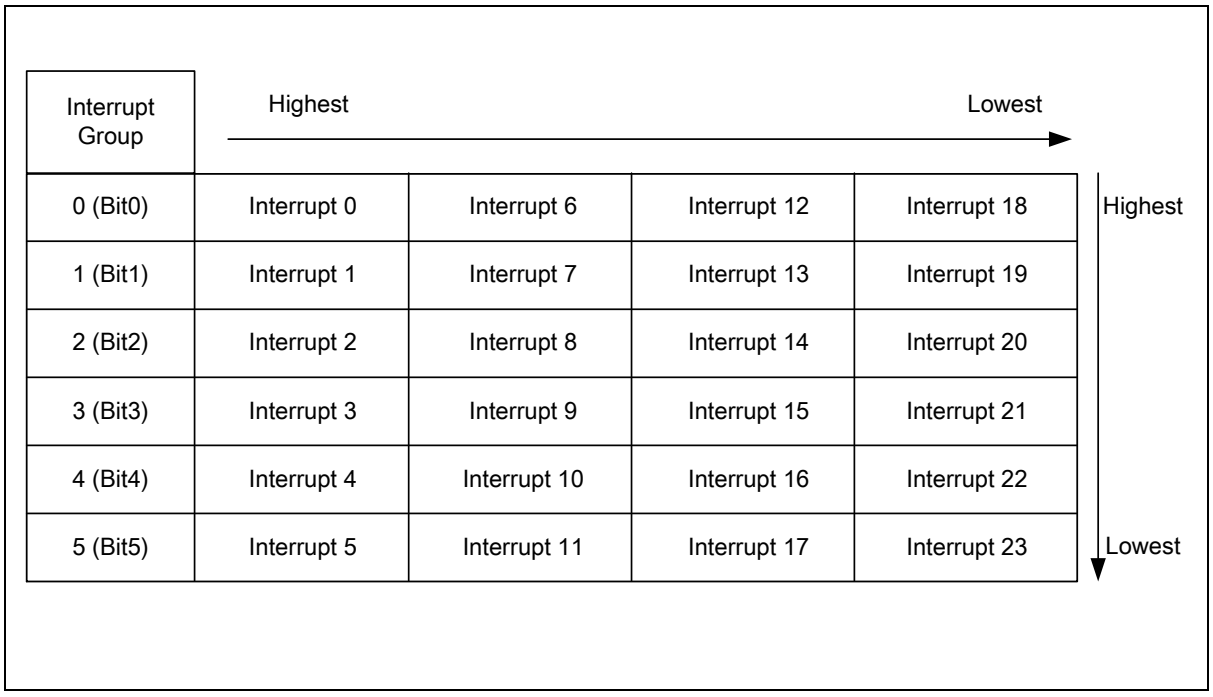


Figure 13. Interrupt Group Priority Level

Figure 13 introduces interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by 2 bits of Interrupt Priority (IP) registers: 1 bit from IP and another 1 bit from IP1.

Interrupt Service Routine serves an interrupt having higher priority first. If two requests of different priority levels are received simultaneously, the request with higher priority level is served prior to the lower one.

6.1 External interrupt

External interrupts on pins of INT0, INT1, INT10, INT11, and INT12 receive various interrupt requests in accordance with the external interrupt polarity 0 register (EIPOL0) and external interrupt polarity 1 register (EIPOL1) as shown in figure 14. Each external interrupt source has enable/disable bits. An external interrupt flag register (EIFLAG) provides status of the external interrupts.

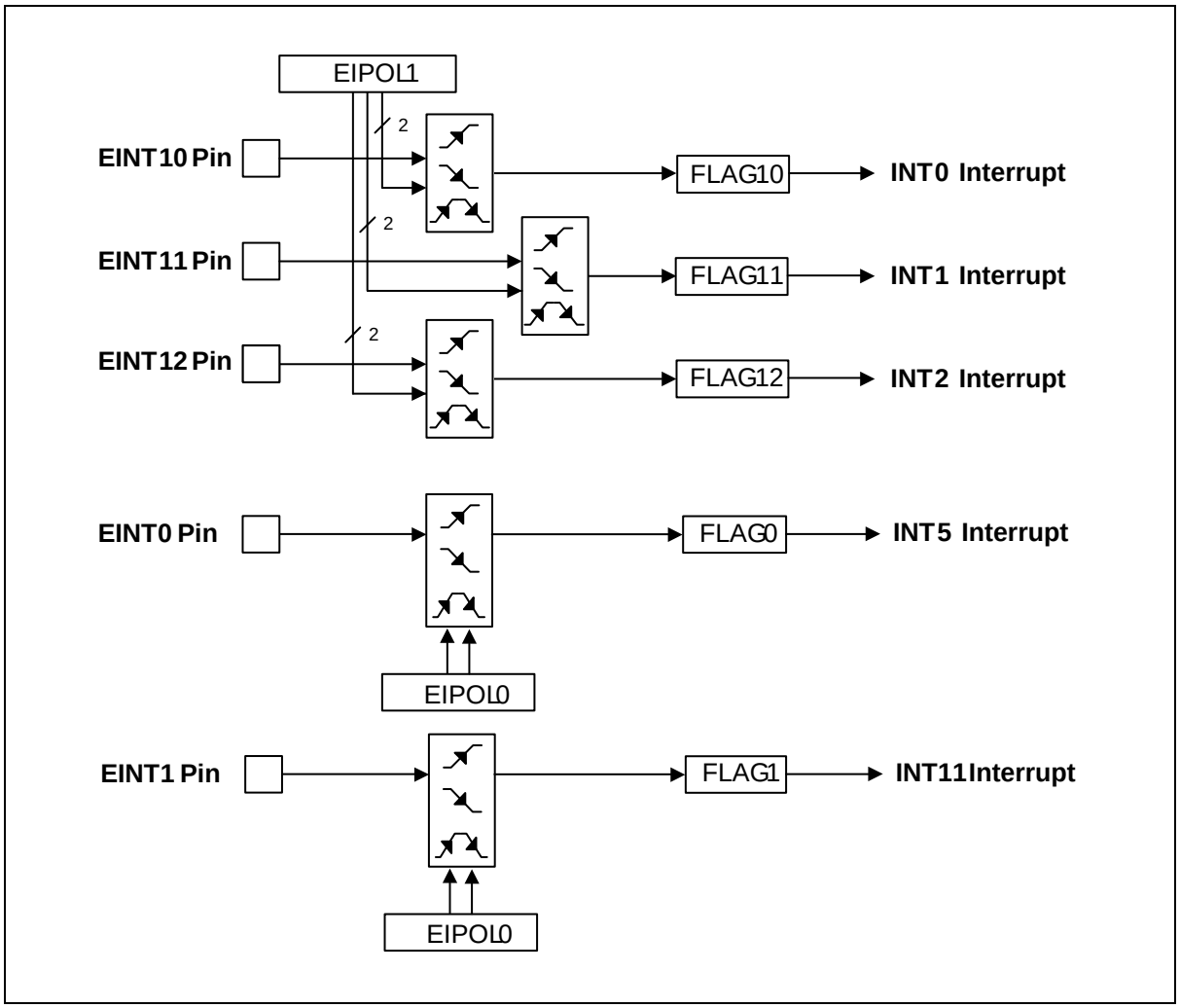


Figure 14. External Interrupt Description

6.2 Interrupt controller block diagram

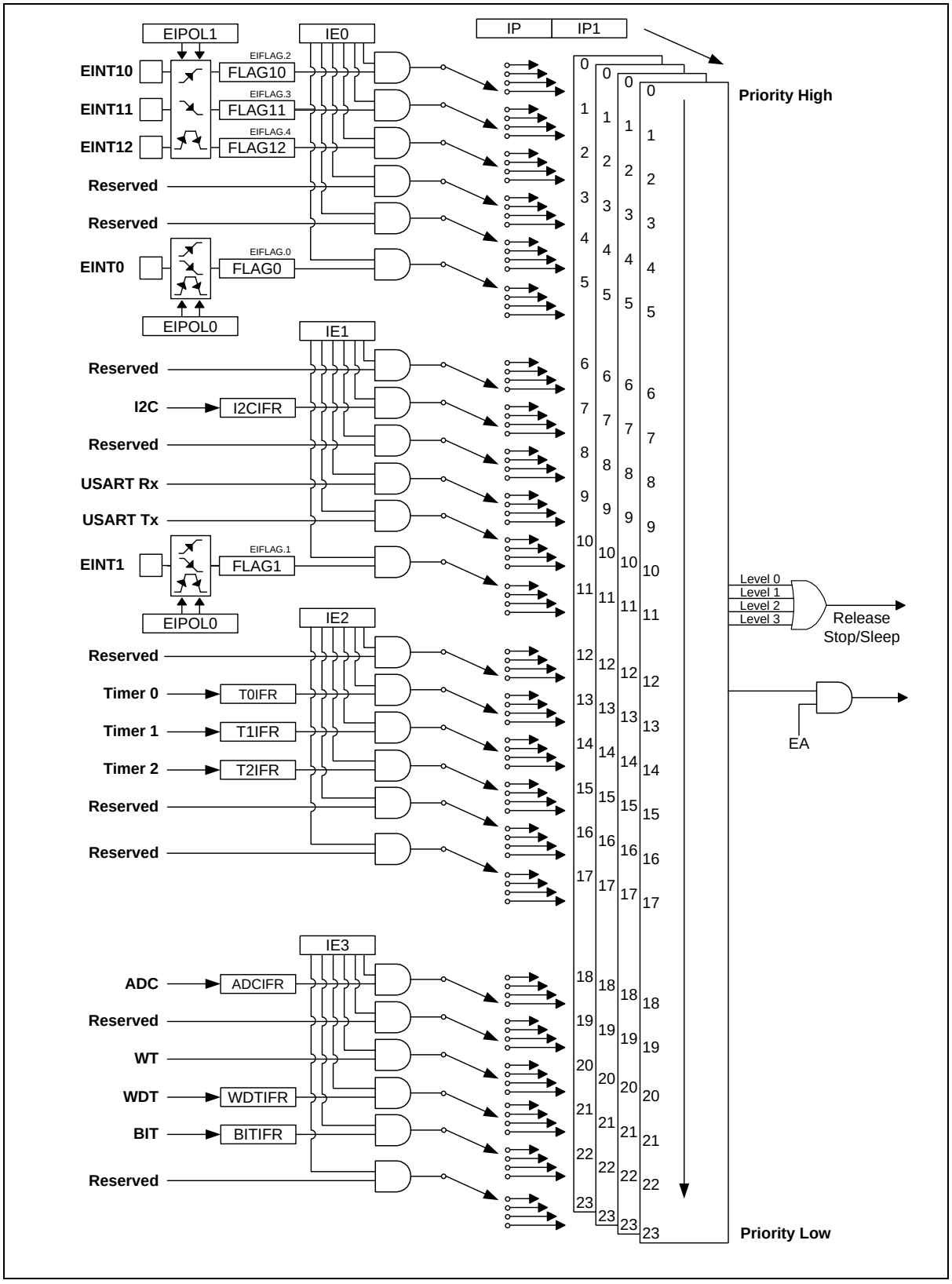


Figure 15. Interrupt Controller Block Diagram

In figure 15, release signal for STOP and IDLE mode can be generated by all interrupt sources which

are enabled without reference to priority level. An interrupt request will be delayed while data is written to one of the registers IE, IE1, IE2, IE3, IP, IP1, and PCON.

6.3 Interrupt vector table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address.

Interrupt controller supports 24 interrupt sources and each interrupt source has a determined priority order as shown in table 8.

Table 8. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector address
Hardware RESET	RESETB	-	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
External Interrupt 12	INT2	IE.2	3	Maskable	0013H
–	INT3	IE.3	4	Maskable	001BH
–	INT4	IE.4	5	Maskable	0023H
External Interrupt 0	INT5	IE.5	6	Maskable	002BH
–	INT6	IE1.0	7	Maskable	0033H
I2C Interrupt	INT7	IE1.1	8	Maskable	003BH
–	INT8	IE1.2	9	Maskable	0043H
USART Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
USART Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
External Interrupt 1	INT11	IE1.5	12	Maskable	005BH
–	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
–	INT16	IE2.4	17	Maskable	0083H
–	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
–	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
–	INT23	IE3.5	24	Maskable	00BBH

To execute the maskable interrupts, both EA bit and a corresponding bit of IEx associated with a specific interrupt source must be set to ‘1’. When an interrupt request is received, a particular interrupt request flag is set to ‘1’ and maintains its status until CPU accepts the interrupt. After the interrupt acceptance, the interrupt request flag will be cleared automatically.

7 Clock generator

As shown in figure 16, the clock generator produces the basic clock pulses which provide the system clock to be supplied to the CPU and the peripheral hardware. It contains main/sub-frequency clock oscillator. The main/sub clock operation can be easily obtained by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively.

The main/sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN/SXIN pin and open the XOUT/SXOUT pin. The default system clock is 1MHz INT-RC Oscillator and the default division rate is eight. In order to stabilize system internally, it is used 1MHz INT-RC oscillator on POR.

MC96F8204 incorporates four types of oscillators:

- Calibrated Internal RC Oscillator (8MHz)
  - INT-RC OSC/1 (8MHz)
  - INT-RC OSC/2 (4MHz)
  - INT-RC OSC/4 (2MHz)
  - INT-RC OSC/8 (1MHz, default system clock)
  - INT-RC OSC/16 (0.5MHz)
  - INT-RC LF (200kHz)
- Main Crystal Oscillator (0.4~12MHz)
- Sub Crystal Oscillator (32.768kHz)
- Internal WDTRC Oscillator (5KHz)

7.1 Block diagram

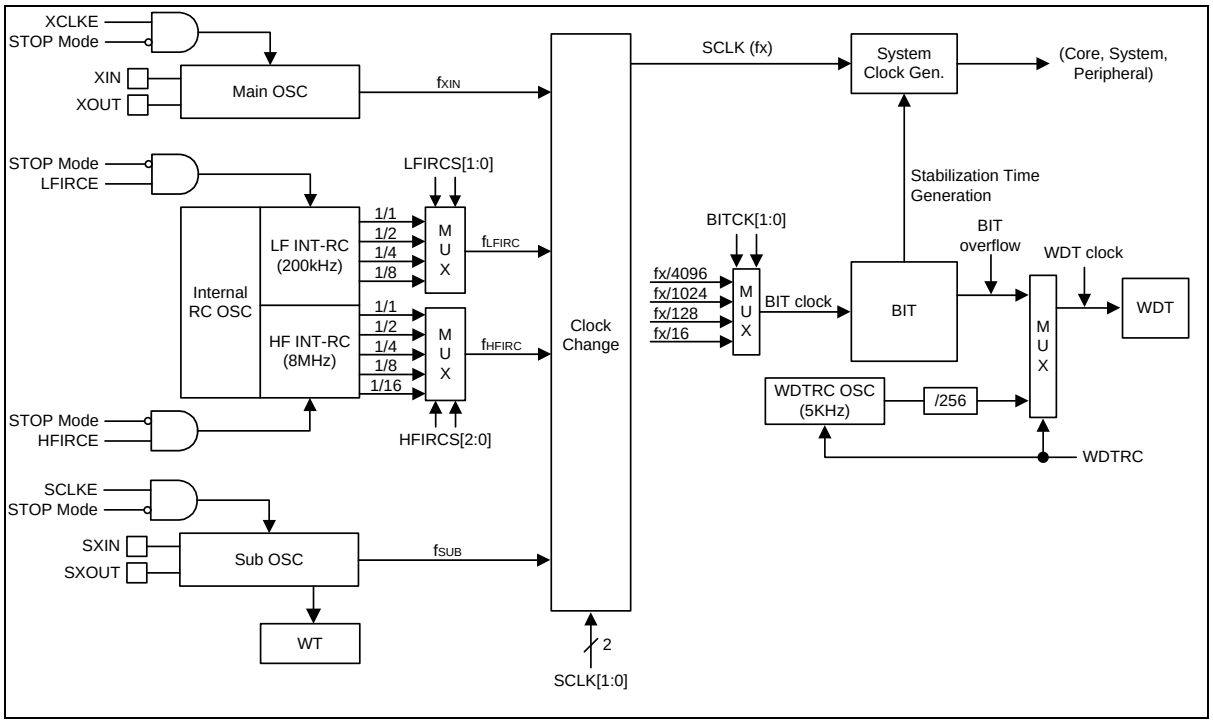


Figure 16. Clock Generator in Block Diagram

8 Basic interval timer

MC96F8204 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting and provides a basic interval timer interrupt (BITIFR).

BIT of MC96F8204 features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

8.1 Block diagram

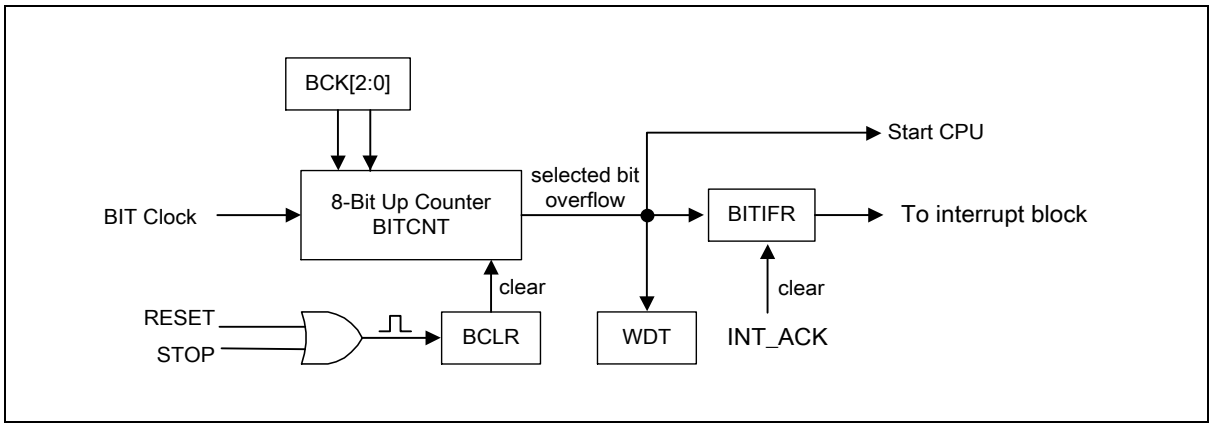


Figure 17. Basic Interval Timer in Block Diagram

9 Watchdog timer

Watchdog timer is used to rapidly detect the CPU malfunctions such as endless looping caused by noise. In addition, it is used to resume the CPU in a normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the Watchdog Timer is not being used for the detection of the CPU malfunctions, it can be used as a timer generating an interrupt at fixed intervals.

Watchdog timer can be used in a free running 8-bit timer mode or in a watch dog timer mode by setting WDTRSON bit, which is WDTCR[5]. If '1' is written to WDTCR[5], WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

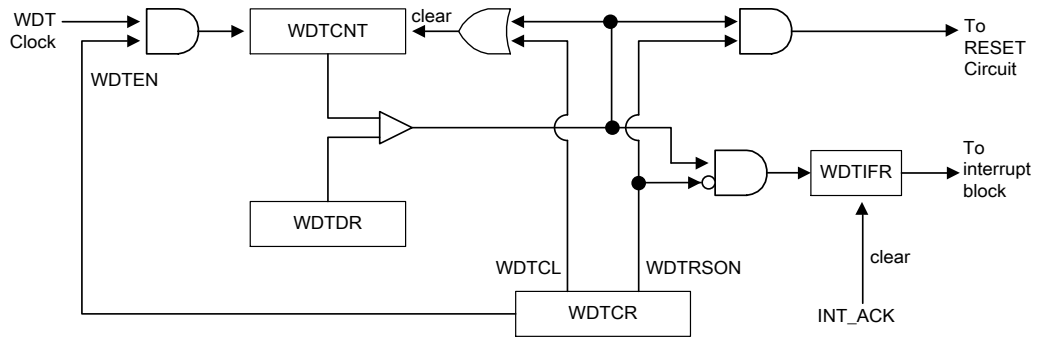
Watchdog timer consists of an 8-bit binary counter and a watchdog timer data register. When value of an 8-bit binary counter is equal to the 8 bits of WDTCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset of CPU in accordance with a bit WDTRSON.

The input clock source of watch dog timer is the BIT overflow and WDTRC. Interval of watchdog timer interrupt is decided by the BIT overflow period and WDTDR set value. Equation of the WDT interrupt interval is described in the followings:

WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1) when BIT overflows

WDT Interrupt Interval = $256/f_{WDTRC}$ x (WDTDR Value+1) when WDTRC

9.1 Block diagram



NOTE: Watchdog timer clock depends on WDTCK bit in WDTCR register.

Figure 18. Watchdog Timer in Block Diagram

10 Watch timer

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit, and watch timer control register. To operate the watch timer, determine the input clock source, output interval, and set WTEN to '1' in watch timer control register (WTCR). It is able to execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register. Even if CPU is STOP mode, sub clock is able to be so alive that WT can continue the operation. The watch timer counter circuits may be composed of 21-bit counter which contains low 14-bit with binary counter and high 7-bit counter in order to raise resolution. In WTDR, it can control WT clear and set interval value at write time, and it can read 7-bit WT counter value at read time.

10.1 Block diagram

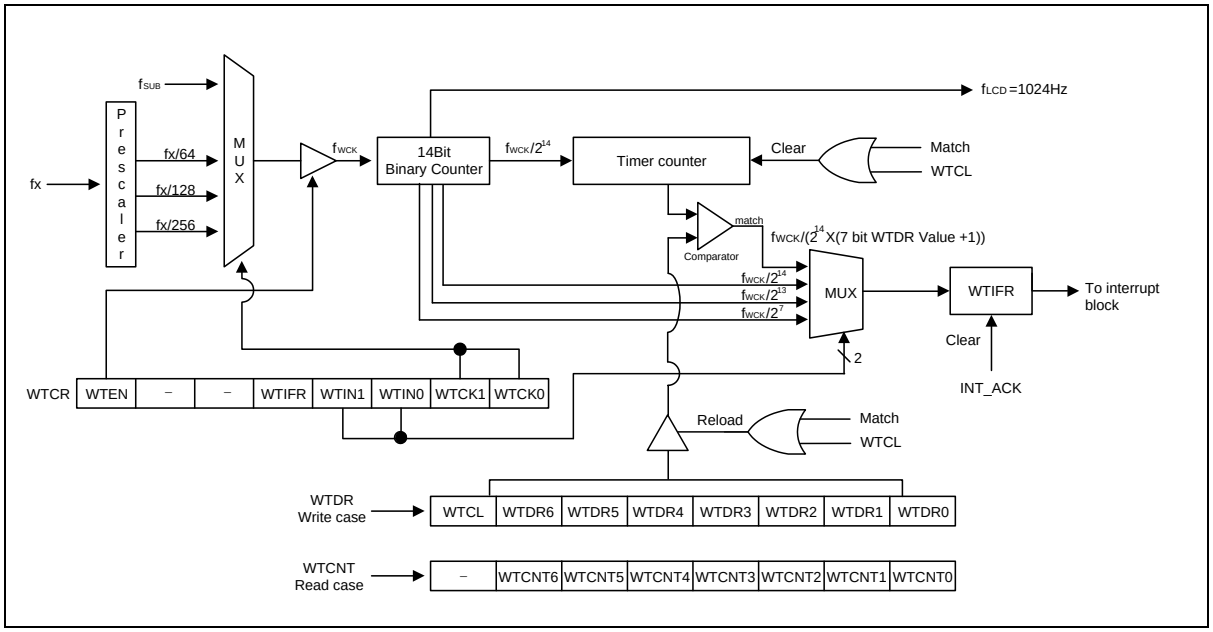


Figure 19. Watch Timer in Block Diagram

11 TIMER 0

An 8-bit timer 0 incorporates a multiplexer and four registers such as timer0 counter register, timer0 data register, timer0 capture data register and timer0 control register (T0CNT, T0DR, T0CDR, T0DR).

TIMER 0 operates in one of two operating modes:

- 8-bit timer/ counter mode
- 8-bit capture mode

Specifically, in capture mode, data is captured into input capture data register (T0CDR) by EINT10. In timer/counter mode, whenever counter value is equal to T0DR, a match signal is generated.

A timer/counter 0 uses an internal clock. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (T0CK[2:0]).

- TIMER 0 clock sources: f_X/2, 4, 8, 32, 128, 512, 2048

Table 9. TIMER 0 Operating Modes

T0EN	T0MS	T0CK[2:0]	Timer 0
1	0	XXX	8 Bit Timer/Counter Mode
1	1	XXX	8 Bit Capture Mode

11.1 Block diagram

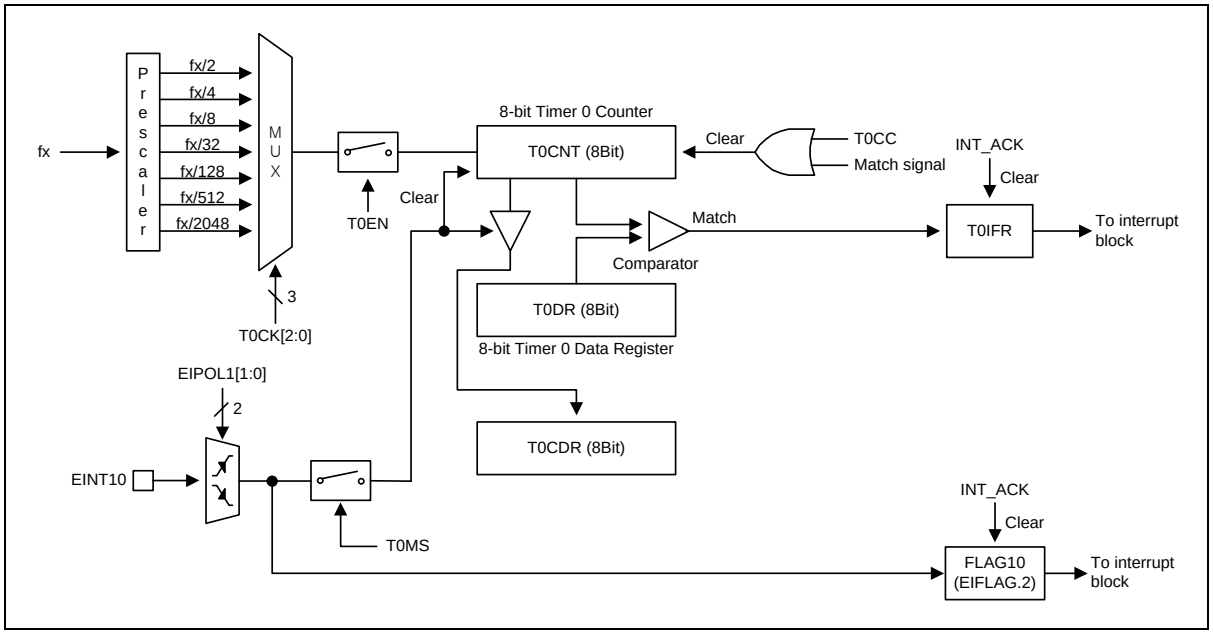


Figure 20. 8-bit Timer 0 in Block Diagram

12 TIMER 1/2

A 16-bit timer 1/2 incorporates a multiplexer and six registers such as timer1/2 A data register high/low, timer1/2 B data register high/low, timer1/2 control register high/low (TnADRH, TnADRL, TnBDRH, TnBDRL, TnCRH, TnCRL).

TIMER 1/2 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically, in capture mode, data is captured into input capture data register (TnBDRH/TnBDRL) by EINT11/EINT12. TIMER 1/2 outputs the comparison result between counter and data register through TnO port in timer/counter mode. TIMER 1/2 outputs PWM wave form through PWMnO port in the PPG mode.

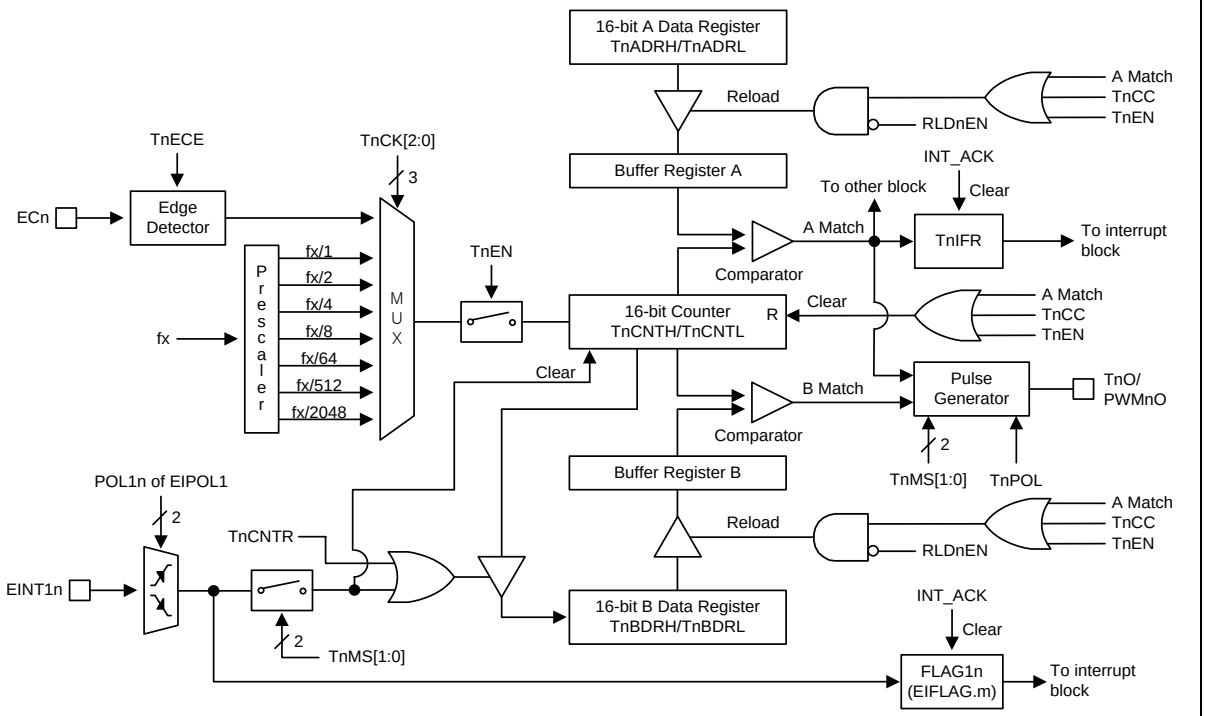
A timer/counter 1/2 uses an internal clock or an external clock (ECn) as an input clock source. The clock sources are introduced below, and one is selected by clock selection logic which is controlled by clock selection bits (TnCK[2:0]).

- TIMER 1/2 clock sources: f_X/1, 2, 4, 8, 64, 512, 2048 and ECn

Table 10. TIMER 1/2 Operating Modes

TnEN	P0FSRL [5:4](T1)	P0FSRL [7:6](T2)	TnMS[1:0]	TnCK[2:0]	Timer 1
1	10	10	00	XXX	16 Bit Timer/Counter Mode
1	00	00	01	XXX	16 Bit Capture Mode
1	10	10	10	XXX	16 Bit PPG mode (one-shot mode)
1	10	10	11	XXX	16 Bit PPG mode (repeat mode)

12.1 Block diagram



NOTE: TnEN is automatically cleared to logic '0' after one pulse is generated at a PPG one-shot mode.
1.

Figure 21. 16-bit Timer 1/2 in Block Diagram (Where n = 1 and 2, m = 3 and 4)

13 12-bit A/D Converter

Analog-to-digital (A/D) converter allows conversion of an analog input signal to a corresponding 12-bit digital output. The A/D module has 8 analog inputs, and the output of the multiplexer becomes the input into the converter, which generates a result via successive approximation.

The A/D module has four registers which are the A/D converter control high register (ADCCRH), A/D converter control low register (ADCCRL), A/D converter data high register (ADCDRH), and A/D converter data low register (ADCDRL). The channels to be converted are selected by setting ADSEL[3:0]. To execute A/D conversion, TRIG[1:0] bits should be set to ‘xx’. The register ADCDRH and ADCDRL contains the results of the A/D conversion. When the conversion is completed, the result is loaded into the ADCDRH and ADCDRL, the A/D conversion status bit AFLAG is set to ‘1’, and the A/D interrupt is set. During A/D conversion, AFLAG bit is read as ‘0’.

13.1 Block diagram

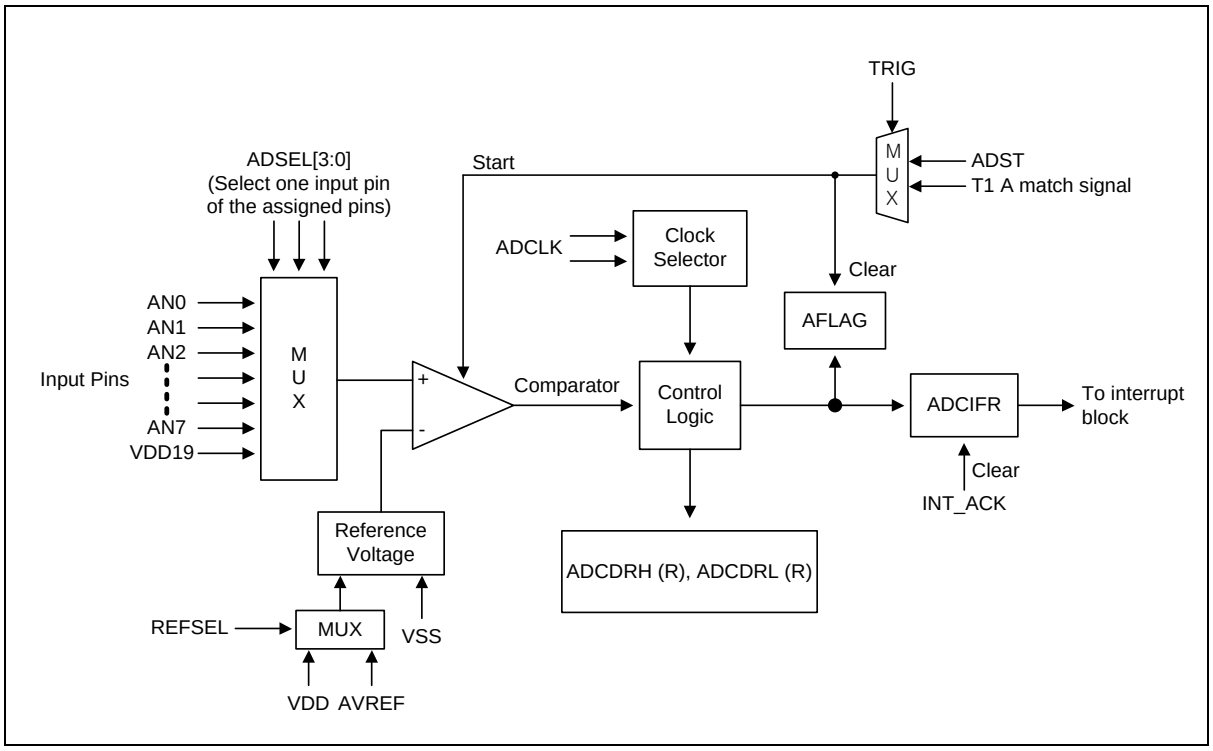
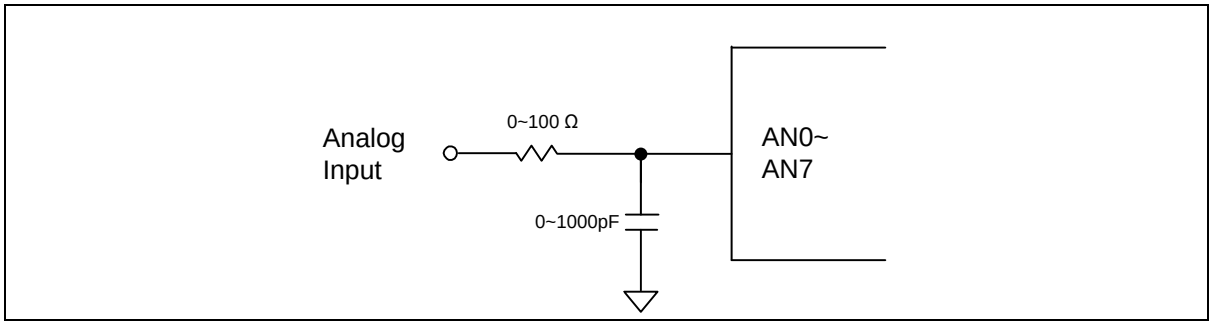


Figure 22. 12-bit ADC Block Diagram



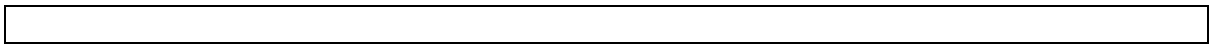


Figure 23. AD Analog Input Pin with Capacitor

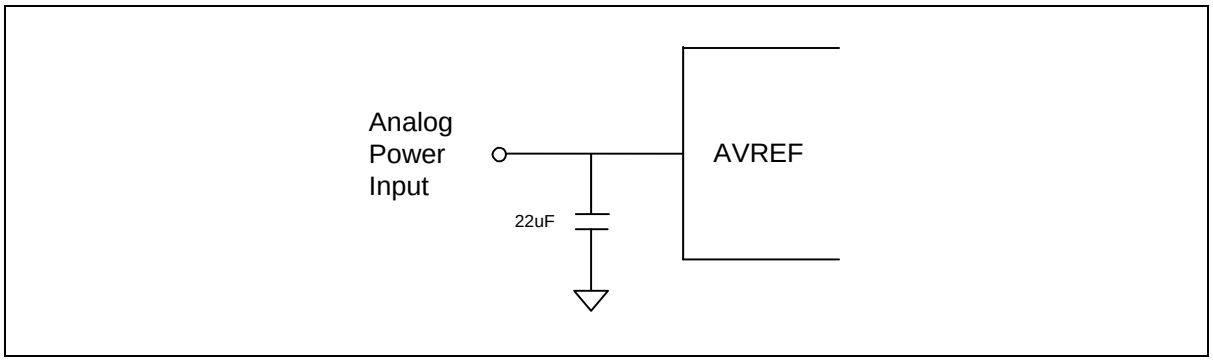


Figure 24. AD Power (AVREF) Pin with Capacitor

14 USART

USART (Universal Synchronous/Asynchronous Receiver/Transmitter) is a microchip that facilitates communication through a computer's serial port using RS-232C protocol. MC96F8204 incorporates a USART function block inside. The USART function block consists of USART control register1/2/3/4, USART status register, USART baud-rate generation register and USART data register.

Operation mode is selected by the operation mode of USART selection bits (USTMS[1:0]).

It has three operating modes as listed in the followings:

- Asynchronous mode (UART)
- Synchronous mode
- SPI mode

14.1 UART block diagram

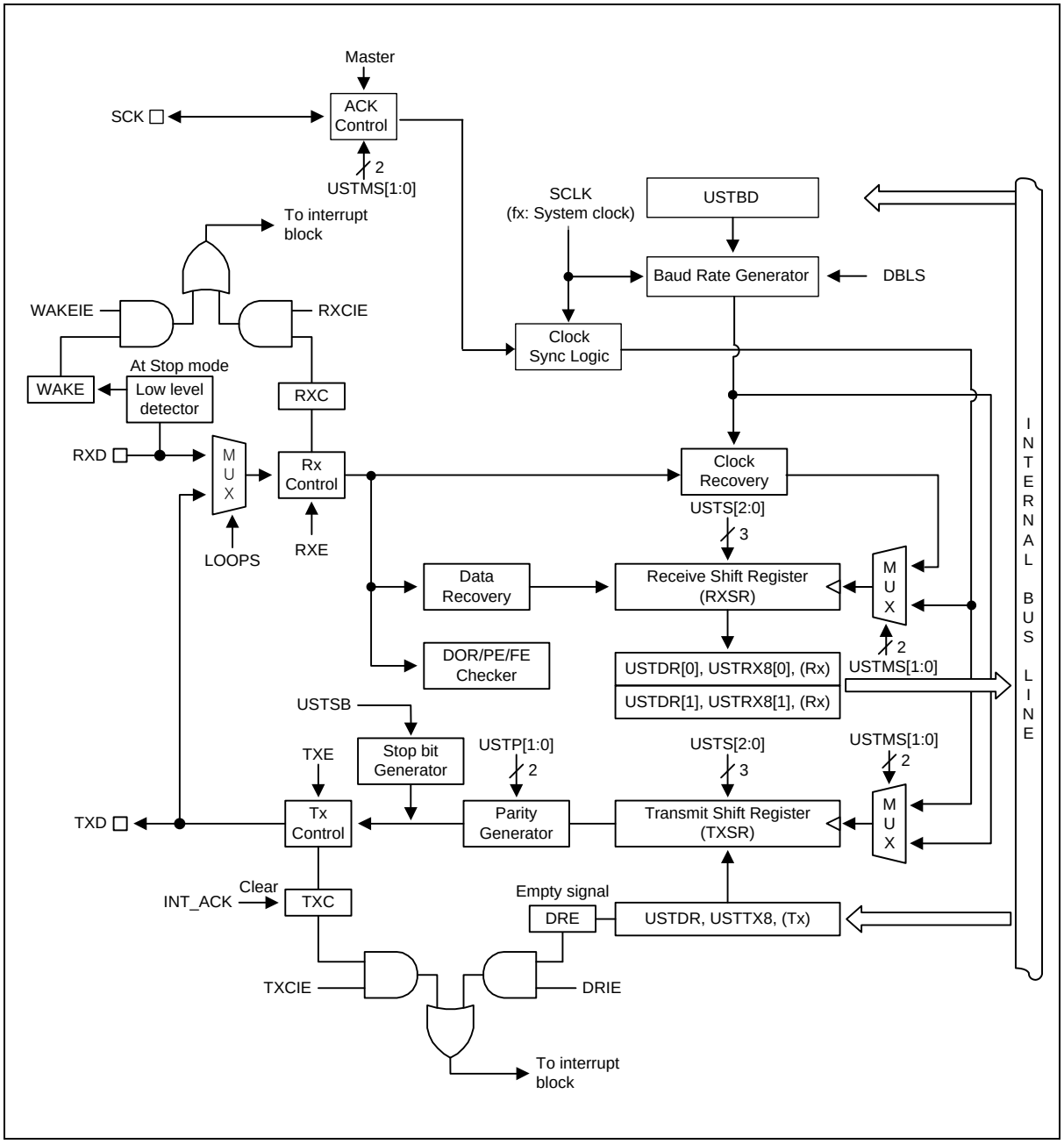
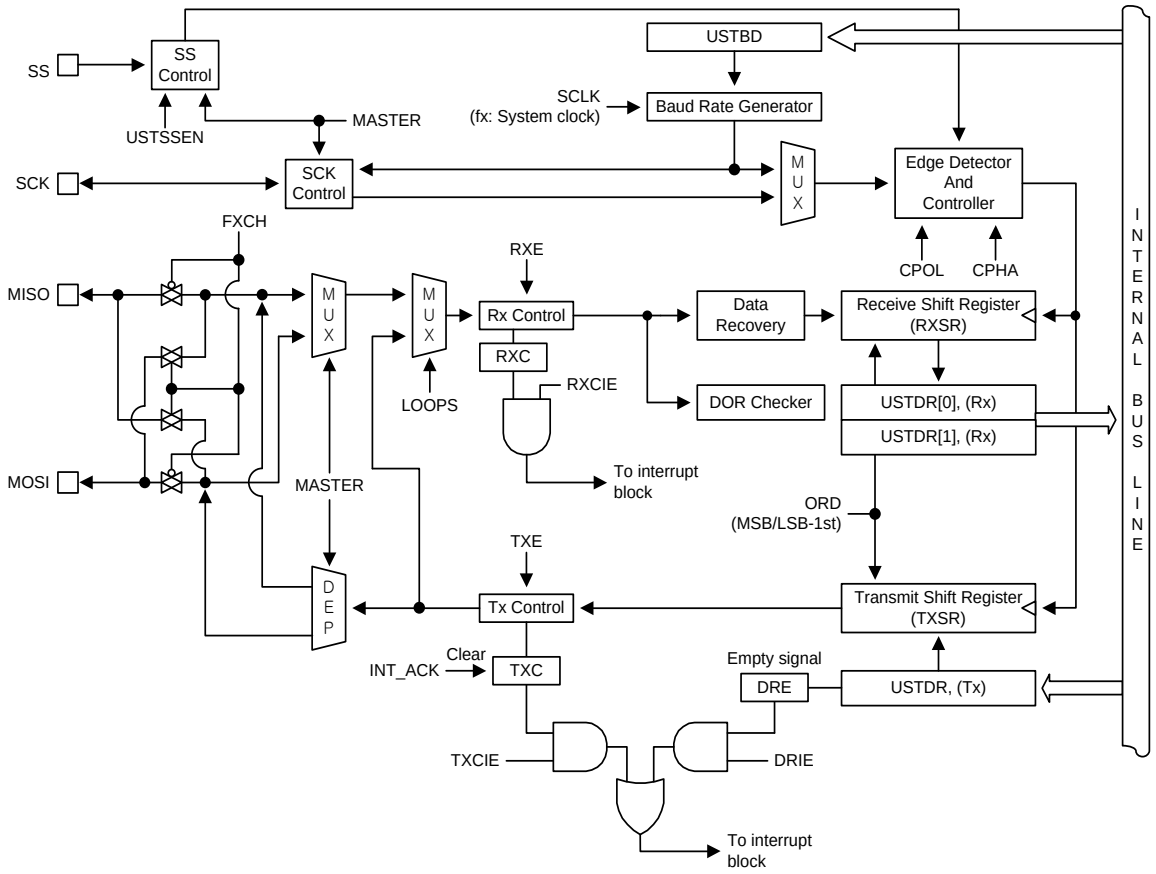


Figure 25. UART Block Diagram

14.2 SPI block diagram



NOTE: The P06 should be configured as “I/O Port” by P0FSRH[1:0] bits on SPI slave mode of USART.

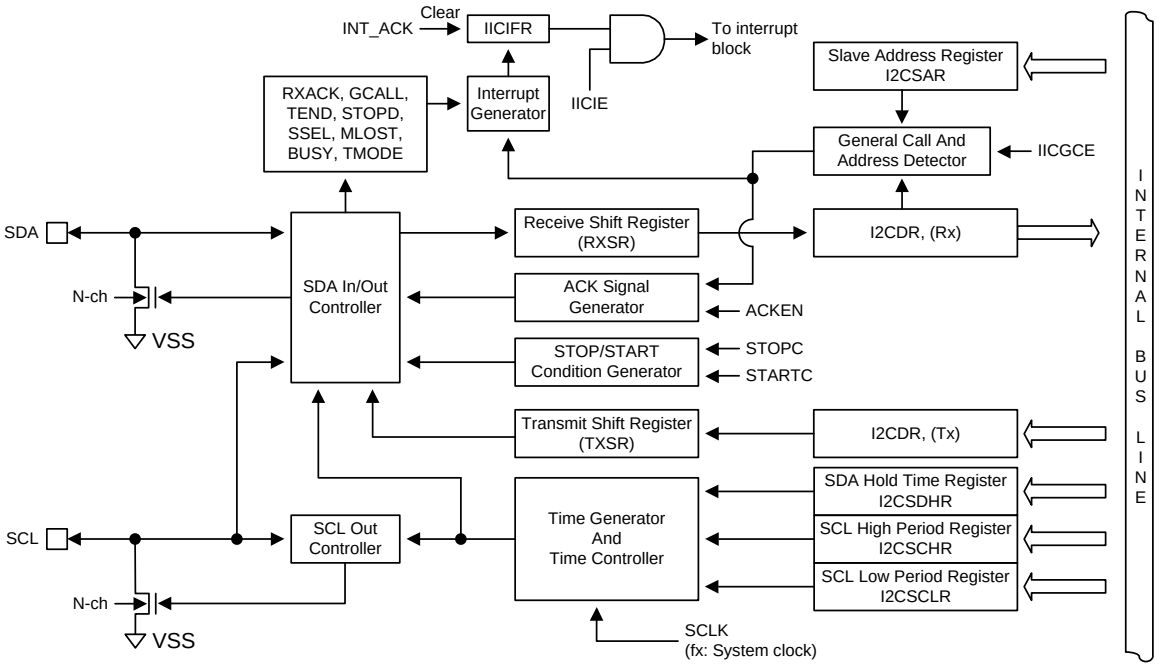
Figure 26. SPI Block Diagram

15 I2C

The I2C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I2C bus standard
- Multi-master operation
- Up to 400kHz data transfer read speed
- 7 bit address
- Support two slave address
- Both master and slave operation
- Bus busy detection

15.1 Block diagram



NOTE: When the corresponding port is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 27. I2C Block Diagram

16 Flash CRC and Checksum generator

Flash CRC (Cyclic Redundancy Check) generator of MC96F8204 generates 16-bit CRC code bits from flash and a generator polynomial. The CRC code for each input data frame is appended to the frame.

Specifically, CRC-based technique is used to verify data transmission or storage integrity. In the scope of the functional safety standards, this technique offers a means of verifying the Flash memory integrity. The flash CRC generator helps compute a signature of software during runtime, to be compared with a reference signature.

The CRC generator has following features:

- Auto CRC and User CRC Mode
- CRC Clock : f_{HFIRC}, $f_{HFIRC}/2$, $f_{HFIRC}/4$, $f_{HFIRC}/8$ and f_X (System clock)
- CRC-16 polynomial: 0x8C81 ($X^{16} + X^{15} + X^{11} + X^{10} + X^7 + 1$)

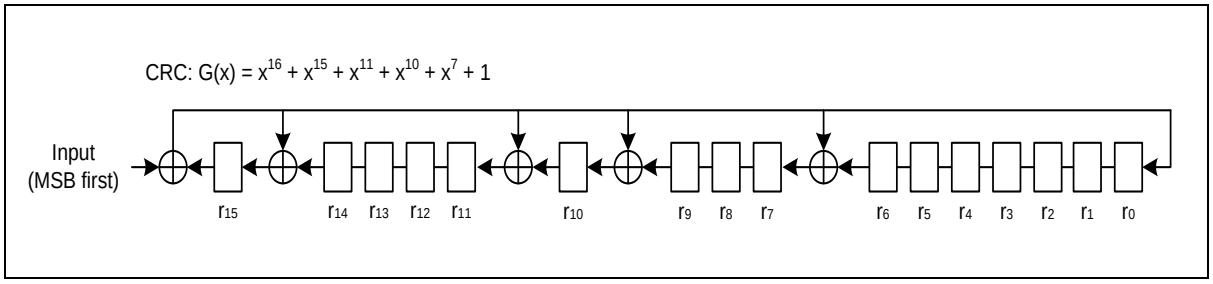


Figure 28. CRC-16 Polynomial Structure

16.1 Block diagram

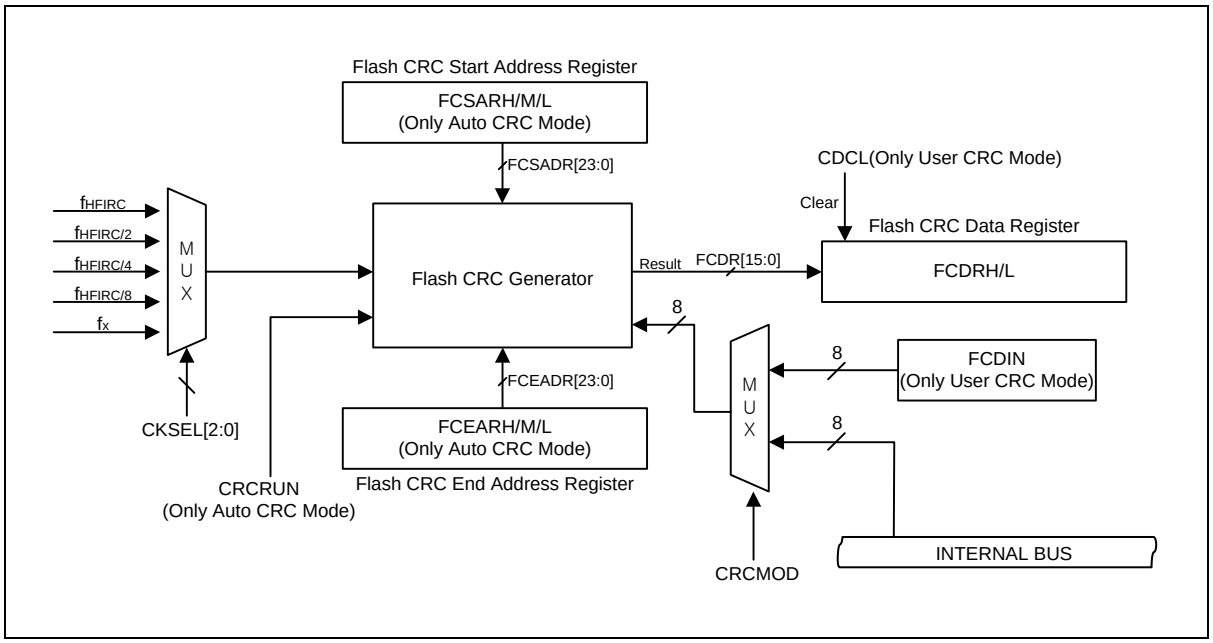


Figure 29. Flash CRC/Checksum Generator Block Diagram

17 Power down operation

MC96F8204 offers two power-down modes to minimize power consumption of itself. Programs under the two power saving modes IDLE and STOP, are stopped and power consumption is reduced considerably.

17.1 Peripheral operation in IDLE/STOP mode

Peripheral's operations during IDLE/STOP mode is introduced in table 11.

Table 11. Peripheral Operation during Power-down Mode

Peripheral	IDLE mode	STOP mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~2	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
USART	Operates Continuously	Only operate with external clock
I2C	Operates Continuously	Only operate with external clock
Internal OSC	Oscillation	Stop when the system clock (f_X) is f_{HFIRC} or f_{LFIRC}
WDTRC OSC (5KHz)	Can be operated with setting value	Can be operated with setting value
Main OSC (0.4~12MHz)	Oscillation	Stop when $f_X=f_{XIN}$
Sub OSC (32.768kHz)	Oscillation	Stop when $f_X=f_{SUB}$
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC1, EC2), External Interrupt, USART by Rx, WT, WDT

18 Reset

When a reset event occurs, an internal register is selected to be initialized in accordance with a reset value. Each reset value introduced in table 12 indicates a corresponding On Chip Hardware that is to be initialized.

Table 12. Reset Value and the Relevant On Chip Hardware

On Chip Hardware	Reset Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral clock	On
Control register	Refer to peripheral registers.

MC96F8204 has 5 types of reset sources as listed in the followings:

- External RESETB
- Power On RESET (POR)
- WDT overflow reset (in a case of WDTEN='1')
- Low voltage reset (in a case of LVREN='0')
- OCD RESET

18.1 Reset block diagram

Figure 30 shows a reset block of MC96F8204.

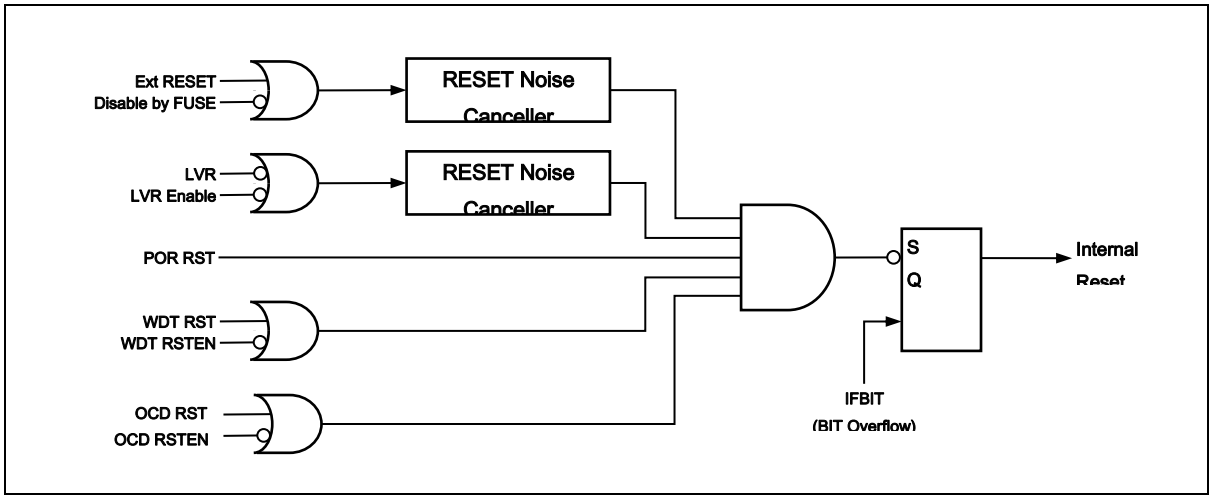


Figure 30. Reset Block Diagram

19 Flash memory

MC96F8204 incorporates flash memory inside. Program can be written, erased, and overwritten on the flash memory while it is mounted on a board. The flash memory can be read by 'MOVC' instruction and programmed in OCD, serial ISP mode or user program mode. Followings are features summary of flash memory.

- Flash Size : 4Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory

NOTE: The RXE bit of USTCR2 register should be disabled before flash memory erase and write start.

19.1 Flash program ROM structure

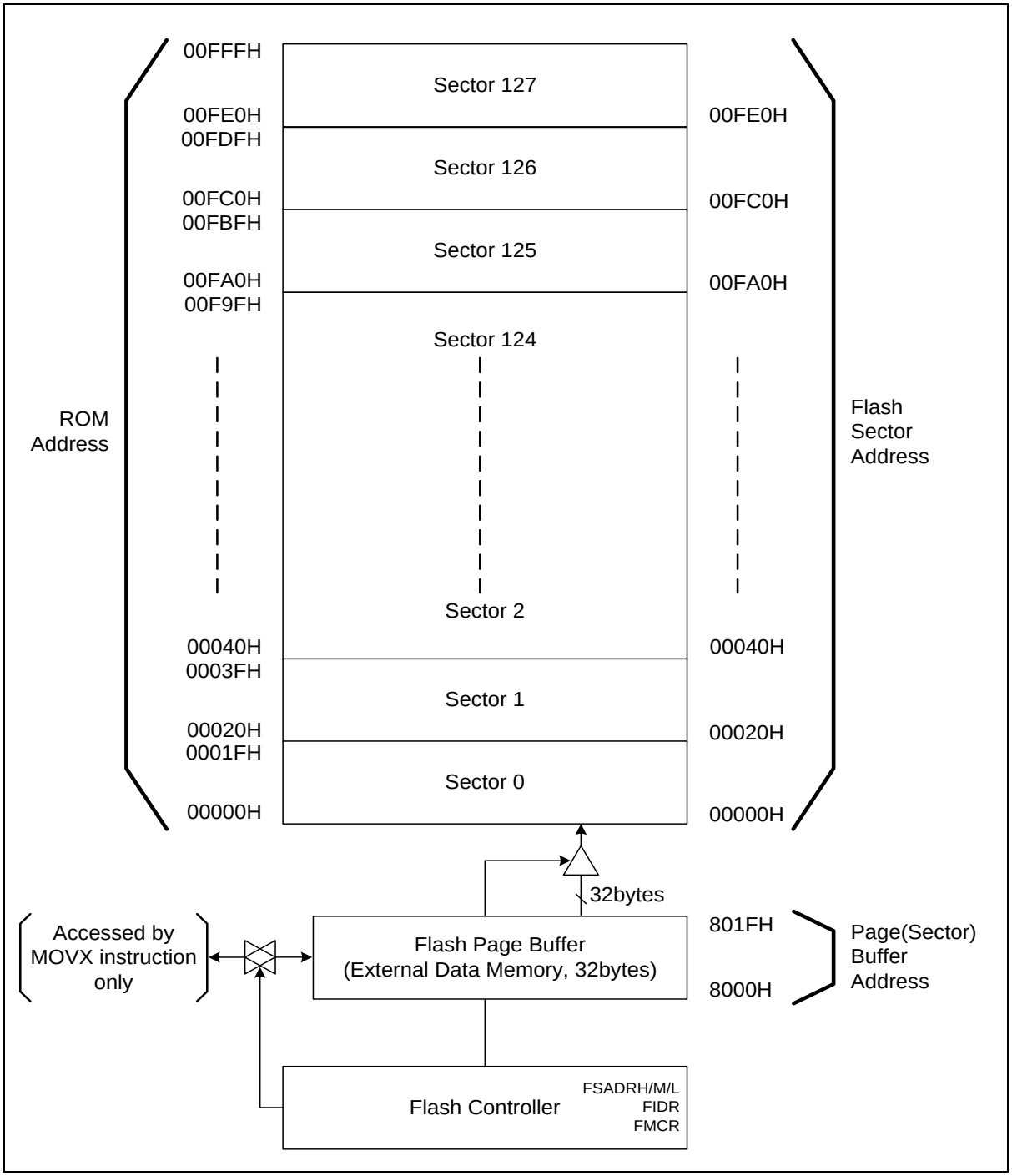


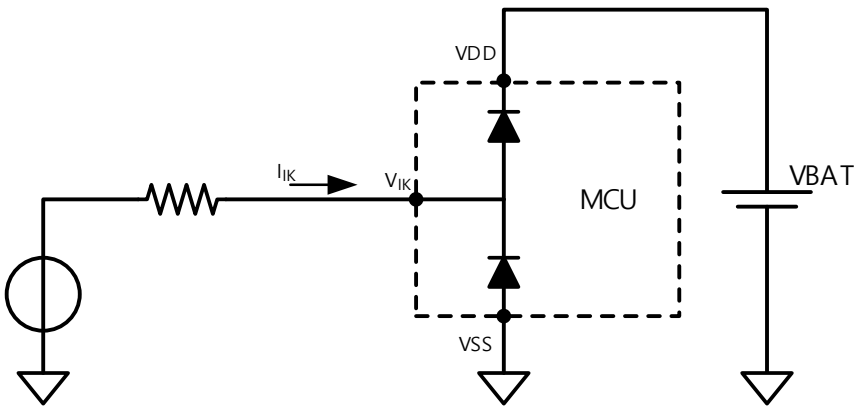
Figure 31. Flash program ROM structure

20 Electrical characteristics

20.1 Absolute maximum ratings

Table 13. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	VDD	-0.3 ~ +6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	V_{IK}(NOTE2)	V_{IK} < 6.5	V	I_{IK} = 200uA
		(VDD-V_{IK}) < 6.5	V	I_{IK} = -200uA
	IOH	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	∑IOH	-80	mA	Maximum current (∑I_{OH})
	IOL	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	∑IOL	120	mA	Maximum current (∑I_{OL})
Total Power Dissipation	PT	600	mW	–
Storage Temperature	TSTG	-65 ~ +150	°C	–



NOTES:

1. Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.
2. V_{IK} is instantaneous voltage like noise (Burst, Impulse etc).

Figure 32. Figure Describing V_{IK}

20.2 Operating conditions

The device must be used in operating conditions that comply with the parameters in table 14.

Table 14. Recommended Operating Conditions

(TA=-40℃ to +85℃)

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Operating voltage	VDD	f_X= 32 ~ 38kHz	SX-tal		1.8	—	5.5	V
		f_X= 0.4 ~ 4.2MHz	X-tal	Ceramic	1.8	—	5.5	
				Crystal	2.0	—	5.5	
		f_X= 0.4 ~ 12.0MHz	X-tal		2.7	—	5.5	
		f_X= 0.2 ~ 8.0MHz	Internal RC		1.8	—	5.5	
Operating temperature	T_{OPR}	VDD=1.8 to 5.5V			-40	—	85	℃

Table 15. Recommended Operating Conditions for IRC during power-up

(TA=+5℃ to +35℃)

Parameter	Symbol	Conditions		Min.	Max.	Unit
Operating voltage	VDD	f_X= 1.0MHz (Reset value)	IRC	V_{LVR} (Reset value)	5.5	V
Operating temperature	T_{OPR}	VDD=V_{LVR} to 5.5V		+5	35	℃

NOTES:

1. The CPU clock should be kept with 1MHz IRC (Reset value) during VDD ≤ 1.8V.
2. During power-up, the LVI can be used for checking VDD voltage by enabling and the CPU clock shouldn't be changed during LVICR.LVIF flag = "1b".

20.3 ADC characteristics

Table 16. ADC Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	–	–		–	12	–	bit
Integral Non-Linear	INL	AVREF= 2.7V to 5.5V fx=8MHz		–	–	±6	LSB
Differential Non-Linearity	DNL			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CONV}	AVREF= 4.0V to 5.5V		20	–	–	us
		AVREF= 3.0V to 5.5V		30	–	–	
		AVREF= 2.7V to 5.5V		60	–	–	
Analog Input Voltage	V_{AIN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	NOTE3		1.8	–	VDD	
Internal VDC Voltage	VDD19	–		1.85	1.95	2.05	V
A/DC Input Leakage Current	I_{AIN}	AVREF=5.12V		–	–	2	uA
A/DC Current	I_{ADC}	Enable	VDD=5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

NOTES:

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)
4. ADCLK must be less than 0.5MHz. If ADCLK is less than 0.125MHz, it can be improved INL characteristic.

Table 17. Recommended ADC Resolution

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

VDD= AVREF [V]	Resolution	Conditions
2.6	11-bit/ Upper 11-bit	ADCLK ≤ 0.5MHz, ILE = ±6[LSB]
2.5	10-bit/ Upper 10-bit	
2.4	9-bit/ Upper 9-bit	
2.3	8-bit/ Upper 8-bit	
2.2	7-bit/ Upper 7-bit	
2.1	6-bit/ Upper 6-bit	
2.0	5-bit/ Upper 5-bit	
1.9	4-bit/ Upper 4-bit	

1.8	3-bit/ Upper 3-bit	

20.4 Power on Reset

Table 18. Power on Reset Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	–	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	uA

20.5 Low voltage reset and Low Voltage Indicator characteristics

Table 19. LVR and LVI Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels. But LVI can select other levels except 1.60V.		–	1.60	1.79	V
				1.90	2.05	2.20	
				2.00	2.15	2.30	
				2.10	2.25	2.40	
				2.22	2.37	2.52	
				2.35	2.50	2.65	
				2.45	2.65	2.85	
				2.62	2.82	3.02	
				2.81	3.01	3.21	
				3.02	3.22	3.42	
				3.27	3.47	3.67	
				3.46	3.76	4.06	
				3.80	4.10	4.40	
				4.21	4.51	4.81	
LVR Hysteresis	△V	–		–	50	150	mV
LVI Hysteresis	△V	–		–	10	50	mV
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable(Both)	VDD= 3V, Run mode	–	14.0	24.0	uA
		Enable(One of two)		–	10.0	18.0	
		Disable	VDD= 3V	–	–	0.1	

20.6 High Frequency Internal RC oscillator characteristics

Table 20. High Internal RC Oscillator Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Frequency	f_{HFIRC}	–		–	8	–	MHz
Tolerance	–	T_A = 0°C to +50°C		–	–	±2.0	%
		T_A = -20°C to +85°C				±3.0	
		T_A = -40°C to +85°C				±4.0	
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{HFS}	–		–	–	100	us
IRC Current	I_{HFIRC}	Enable	VDD=5V	–	0.2	–	mA
		Disable		–	–	0.1	uA

20.7 Low Frequency Internal RC oscillator characteristics

Table 21. Low Internal RC Oscillator Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Frequency	f_{LFIRC}	–		–	200	–	kHz
Tolerance	–	V_{DD}= 2.2 to 5.5V, T_A = -20°C to +85°C		–	–	±3.0	%
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{LFS}	–		–	–	100	us
IRC Current	I_{LFIRC}	Enable	VDD=5V	–	40	–	uA
		Disable		–	–	0.1	uA

20.8 Internal Watch-dog Timer RC oscillator characteristics

Table 22. Internal WDTRC Oscillator Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

20.9 DC characteristics

Table 23. DC Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V, f_{XIN}=12MHz)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input high voltage	V_{IH}	P0, P1, P2, RESETB		0.8VDD	–	VDD	V
Input low voltage	V_{IL}	P0, P1, P2, RESETB		–	–	0.2VDD	V
Output high voltage	V_{OH}	VDD= 4.5V, I_{OH}= –2mA, All output ports		VDD-1.0	–	–	V
Output low voltage	V_{OL1}	VDD= 4.5V, I_{OL}= 10mA, All output ports except V_{OL2}		–	–	1.0	V
	V_{OL2}	VDD=4.5V, I_{OL} = 15mA, P00-P05		–	–	1.0	V
Input high leakage current	I_{IH}	All input ports		–	–	1.0	uA
Input low leakage current	I_{IL}	All input ports		-1.0	–	–	uA
Pull-up resistor	R_{PU1}	VI=0V, T_A=25℃, All Input ports	VDD= 5.0V	25	50	100	KΩ
			VDD= 3.0V	50	100	200	
	R_{PU2}	VI=0V, T_A=25℃, RESETB	VDD= 5.0V	150	250	400	KΩ
			VDD= 3.0V	300	500	700	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A=25℃, VDD= 5V		600	1200	2000	KΩ
	R_{X2}	SXIN= VDD, SXOUT= VSS, T_A=25℃, VDD= 5V		2500	5000	10000	

Table 23. DC Characteristics (continued)

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V, f_{XIN}=12MHz)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply current	I_{DD1} (RUN)	f_{XIN} = 12MHz	VDD=5V±10%	–	3.0	6.0	mA
		f_{HFIRC} = 8MHz		–	2.0	4.0	
		f_{XIN} = 10MHz	VDD=3V±10%	–	2.0	4.4	
		f_{LFIRC} = 200kHz		–	120	240	uA
	I_{DD2} (IDLE)	f_{XIN} = 12MHz	VDD=5V±10%	–	2.0	4.0	mA
		f_{HFIRC} = 8MHz		–	1.0	2.0	
		f_{XIN} = 10MHz	VDD=3V±10%	–	1.0	2.0	
		f_{LFIRC} = 200kHz		–	65	130	uA
	I_{DD3}	f_{XIN}= 32.768kHz, VDD= 3V±10%, T_A= 25℃	Sub RUN	–	90.0	180.0	uA
	I_{DD4}		Sub IDLE	–	8.0	16.0	uA
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25℃		–	0.5	3.0	uA

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{HFIRC} and f_{LFIRC} are an internal RC oscillator, and the f_X is the selected system clock, the f_{SUB} is an external sub oscillator.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current includes the current of the power-on reset (POR) block.

20.10 AC characteristics

Table 24. AC Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB input low width	t_{RST}	VDD = 5V	10	–	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD = 5V	200	–	–	ns
External counter input high, low pulse width	t_{ECWH}, t_{ECWL}	EC1/EC2, VDD = 5V	200	–	–	
External counter transition time	t_{REC}, t_{FEC}	EC1/EC2, VDD = 5V	20	–	–	

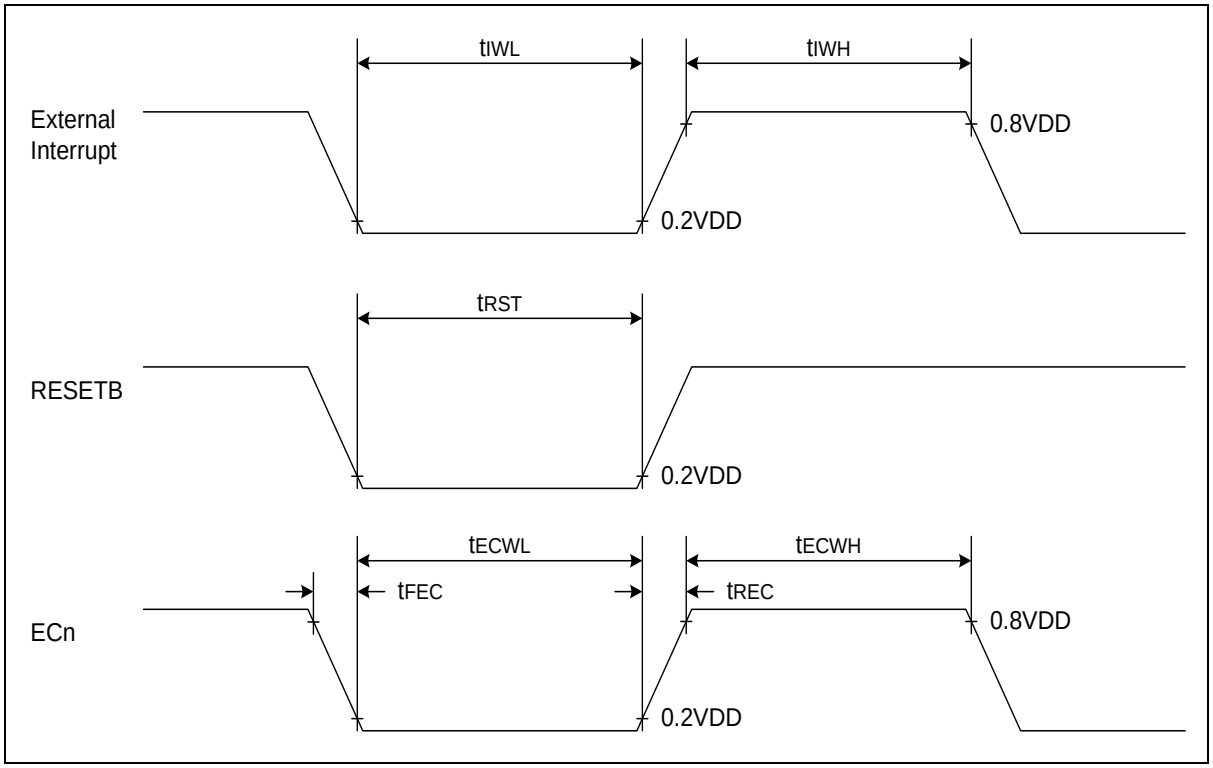


Figure 33. AC Timing (Where n= 1, 2)

20.11 SPI characteristics

Table 25. SPI Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output clock pulse period	t_{SCK}	Internal SCK source	400	–	–	ns
Input clock pulse period		External SCK source	400	–	–	
Output clock high, low pulse width	t_{SCKH} t_{SCKL}	Internal SCK source	140	–	–	
Input clock high, low pulse width		External SCK source	140	–	–	
First output clock delay time	t_{FOD}	Internal/external SCK source	200	–	–	
Output clock delay time	t_{DS}	–	–	–	50	
Input setup time	t_{DIS}	–	200	–	–	
Input hold time	t_{DIH}	–	200	–	–	

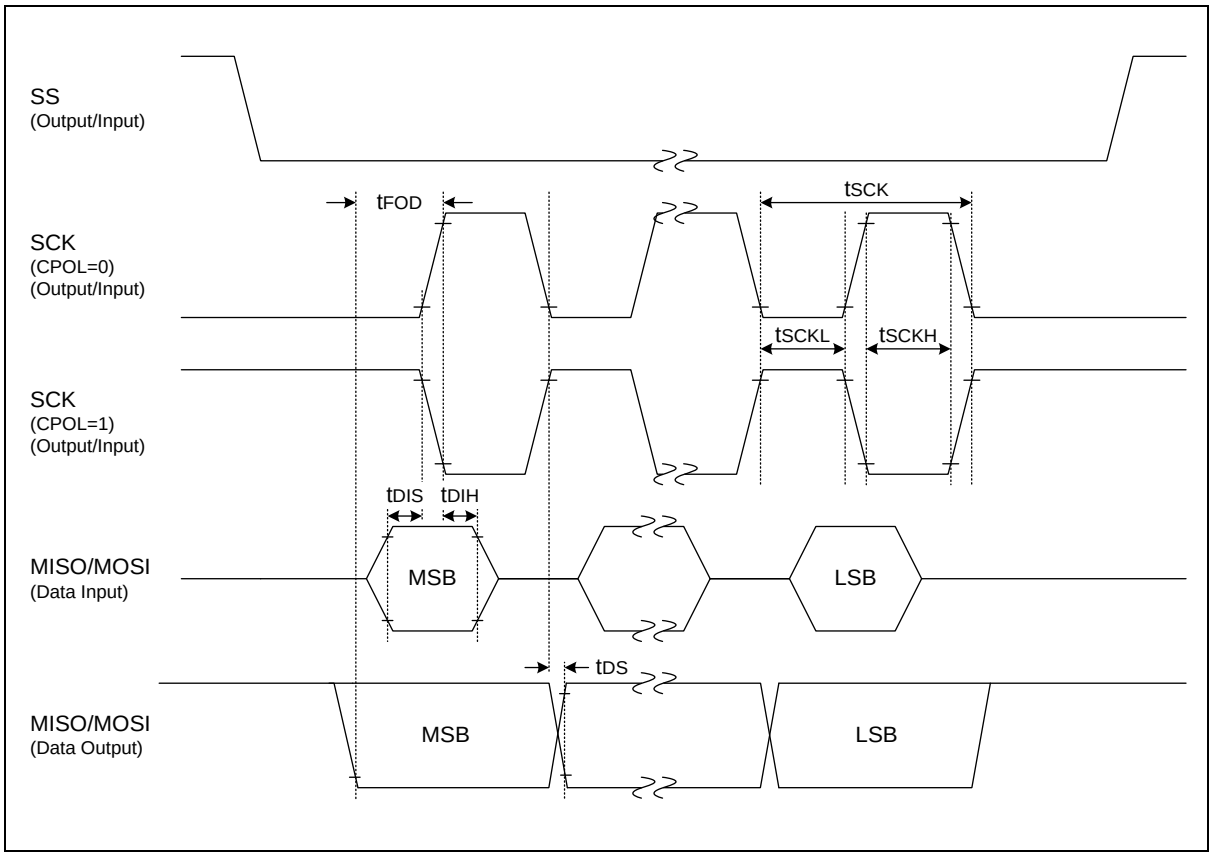


Figure 34. SPI Timing

20.12 UART timing characteristics

Table 26. UART Timing Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU} – 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

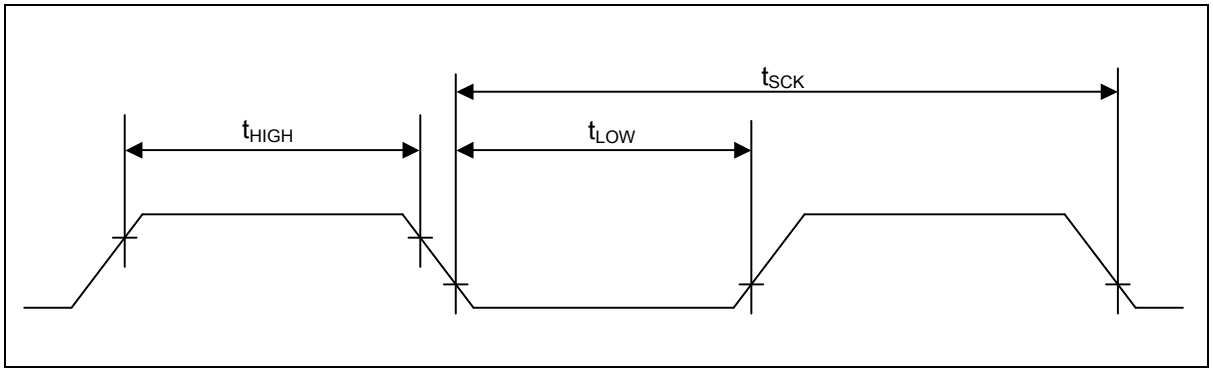


Figure 35. UART Timing Characteristics

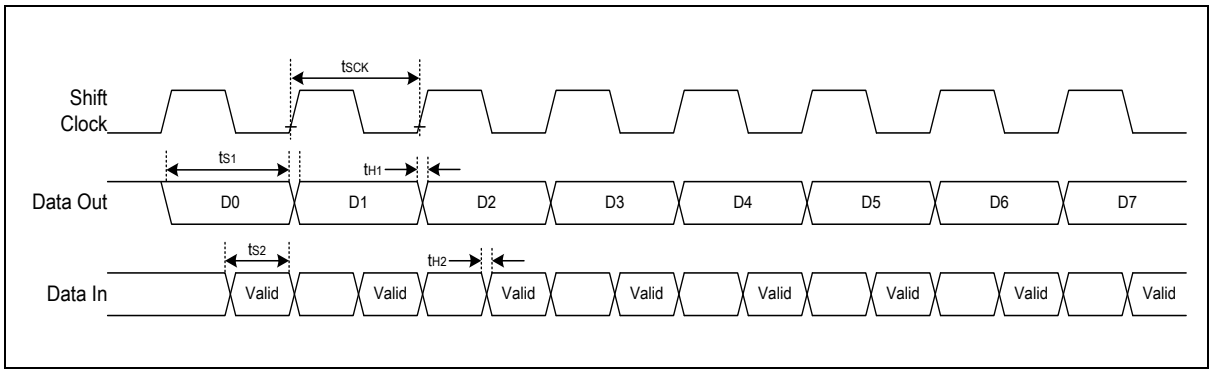


Figure 36. Timing Waveform of UART Module

20.13 I2C characteristics

Table 27. I2C Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Parameter	Symbol	Standard mode		High-Speed mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

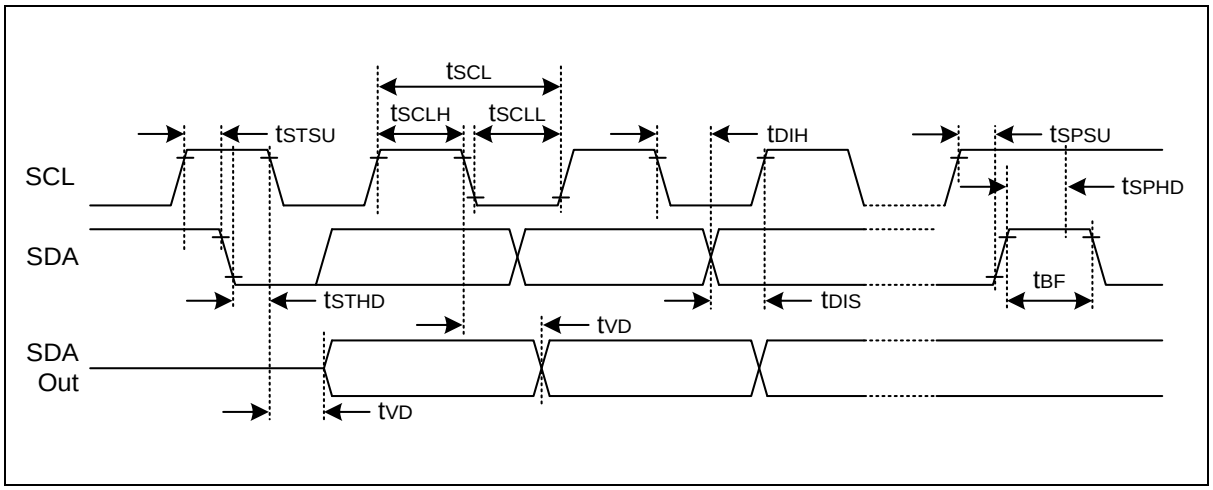


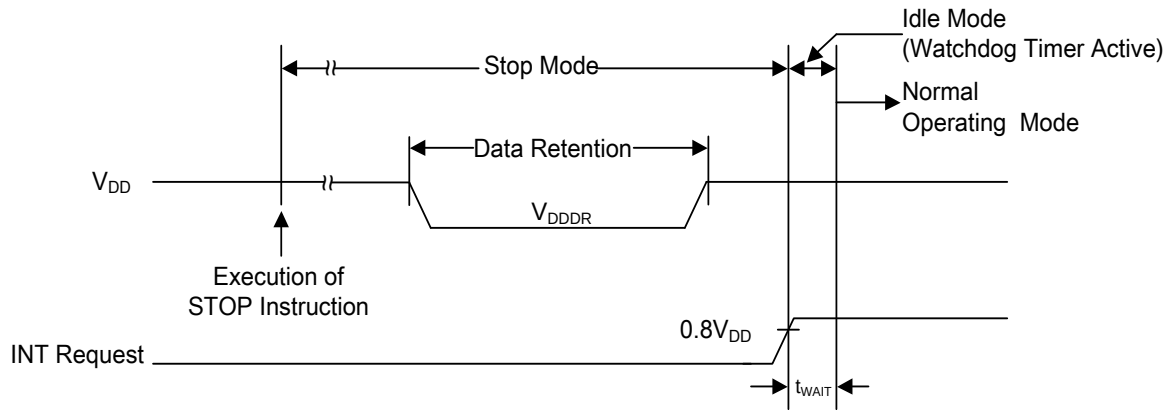
Figure 37. Timing Waveform of I2C

20.14 Data retention voltage in STOP mode

Table 28. Data Retention Voltage in STOP Mode

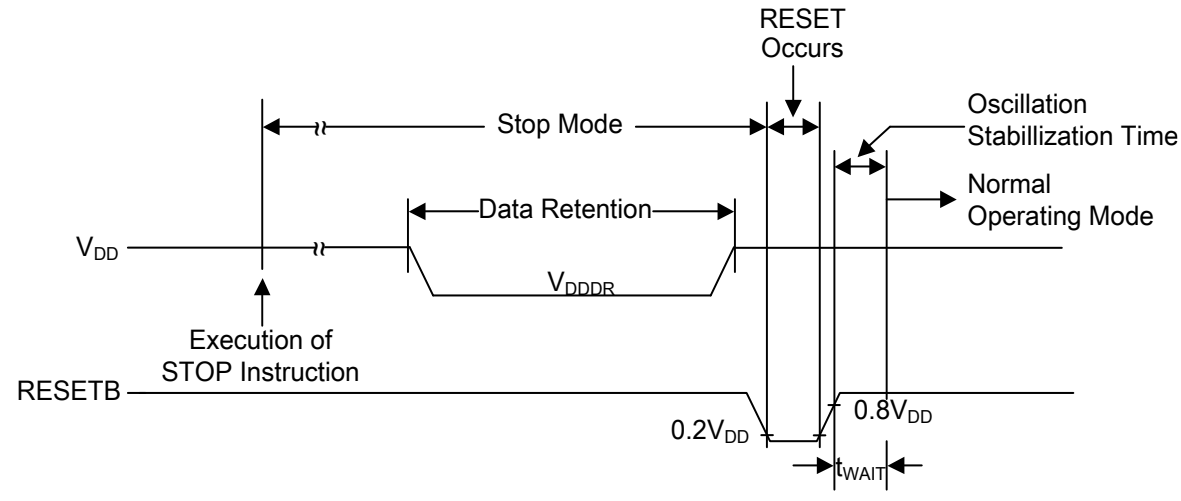
(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V (T_A= 25°C), STOP mode	–	–	1	uA



NOTE: t_{WAIT} is the same as (the selected bit overflow of BIT) x 1/ (BIT clock)

Figure 38. STOP Mode Release Timing when Initiated by an Interrupt



NOTE: t_{WAIT} is the same as (4096 x 4 x f_{IRC}) x 1/ (BIT clock) = (16.4 ms @ 1MHz)

Figure 39. STOP Mode Release Timing when Initiated by RESETB

20.15 Internal flash characteristics

Table 29. Internal Flash Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector write time	t_{FSW}	–	–	2.5	2.7	ms
Sector erase time	t_{FSE}	–	–	2.5	2.7	
Code write protection time	t_{FHL}	–	–	2.5	2.7	
Page buffer reset time	t_{FBR}	–	–	–	5	us
Flash programming frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of write/erase	NF_{WE}	Sector 0 to 119	–	–	10,000	Times
		Sector 120 to 127(256 byte)	–	–	100,000	
Flash Data Retention Time	t_{RT}	–	10	–	–	Years

NOTE: During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

20.16 Input/output capacitance characteristics

Table 30. I/O Capacitance Characteristics

(T_A=-40℃ to +85℃, VDD=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	fx=1MHz unmeasured pins are connected to VSS.	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

20.17 Main Clock Oscillator Characteristics

Table 31. Main Clock Oscillator Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal	Main oscillation frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
External Clock	XIN input frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	

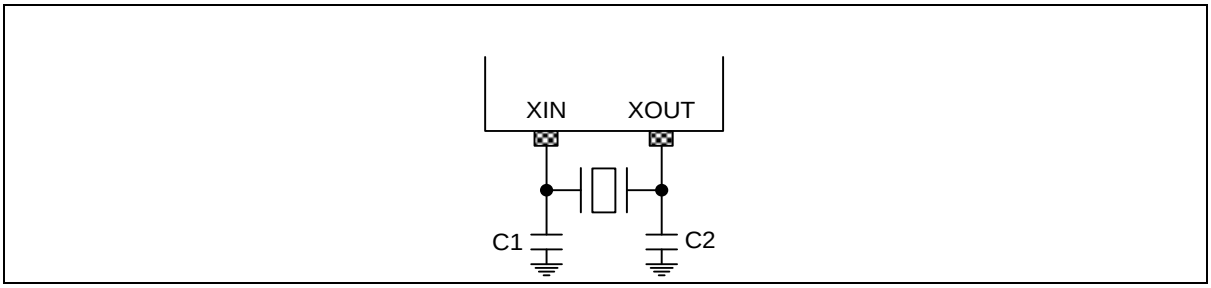


Figure 40. Crystal/Ceramic Oscillator

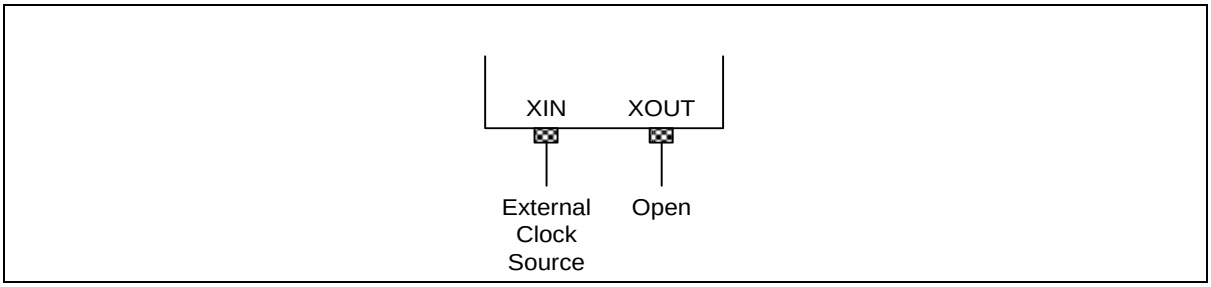


Figure 41. External Clock

20.18 Sub Clock Oscillator Characteristics

Table 32. Sub Clock Oscillator Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal	Sub oscillation frequency	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

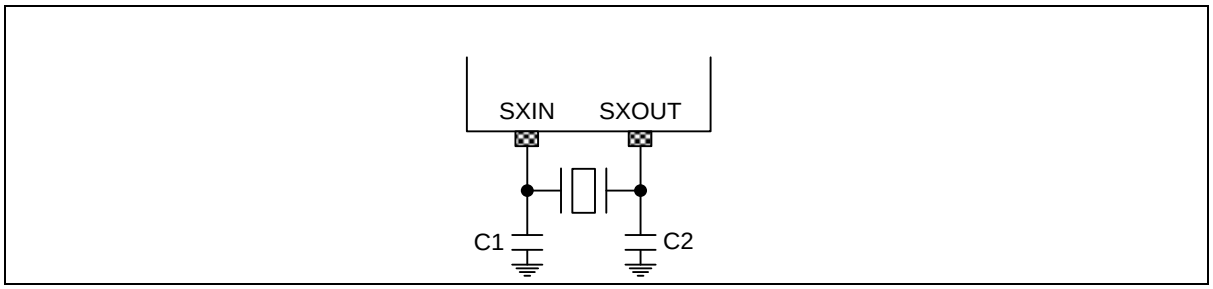


Figure 42. Crystal Oscillator

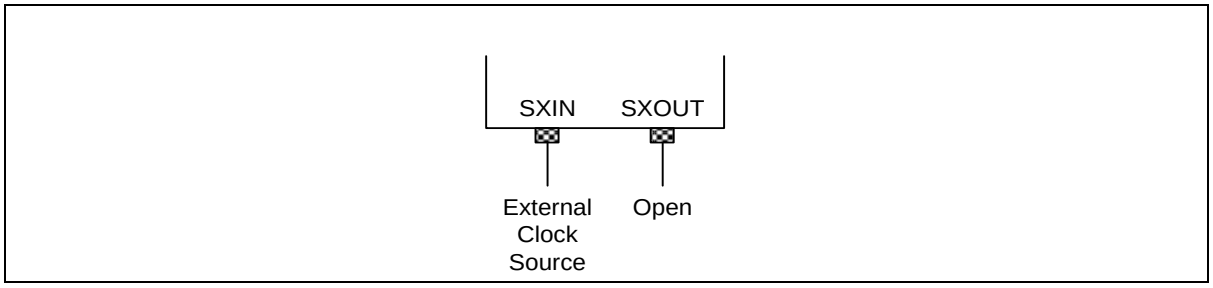


Figure 43. External Clock

20.19 Main Oscillation Stabilization Characteristics

Table 33. Main Oscillation Stabilization Characteristics

(T_A=-40℃ to +85℃, VDD=1.8V to 5.5V)

Oscillator	Parameter	Min.	Typ.	Max.	Unit
Crystal	f_X > 1MHz, VDD= 2.0V to 5.5V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic	f_X > 1MHz, VDD= 1.8V to 5.5V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	10	ms
External Clock	f_{XIN} = 0.4 to 12MHz XIN input high and low width(t_{XH},t_{XL}).	41.7	–	1250	ns

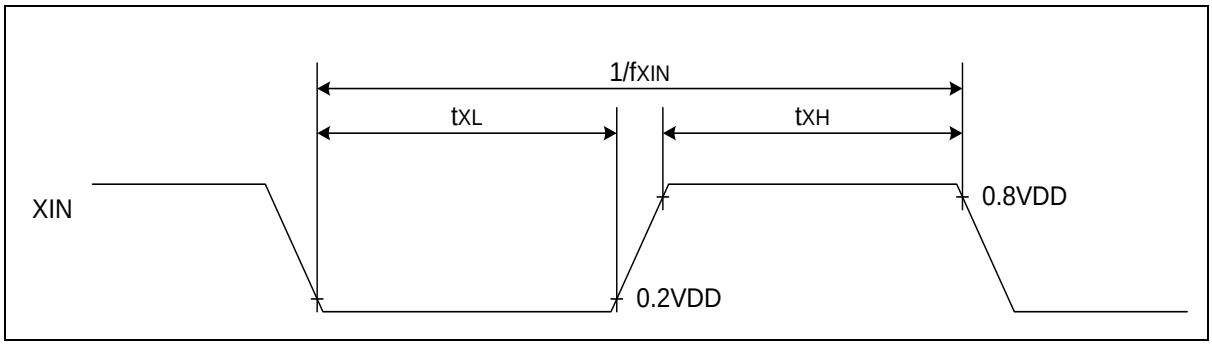


Figure 44. Clock timing measurement at XIN

20.20 Sub Oscillation Stabilization Characteristics

Table 34. Sub Oscillation Stabilization Characteristics

(T_A=-40℃ to +85℃, VDD=2.2V to 5.5V)

Oscillator	Parameter	Min.	Typ.	Max.	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width(t_{XH},t_{XL}).	5	–	15	us

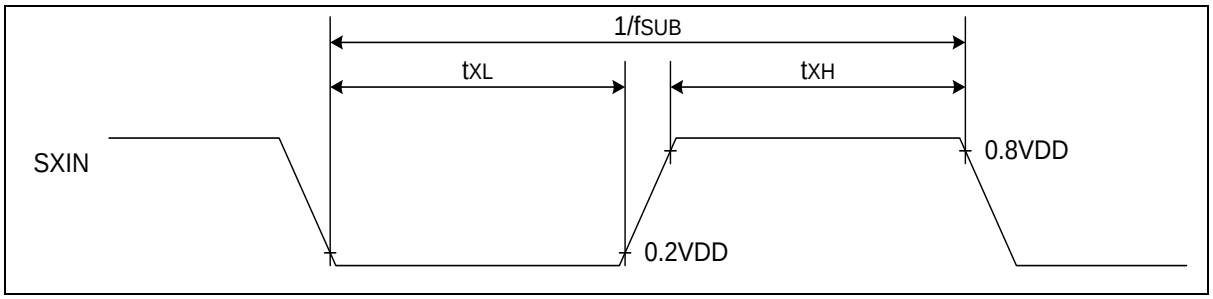


Figure 45. Clock timing measurement at SXIN

20.21 Operating Voltage Range

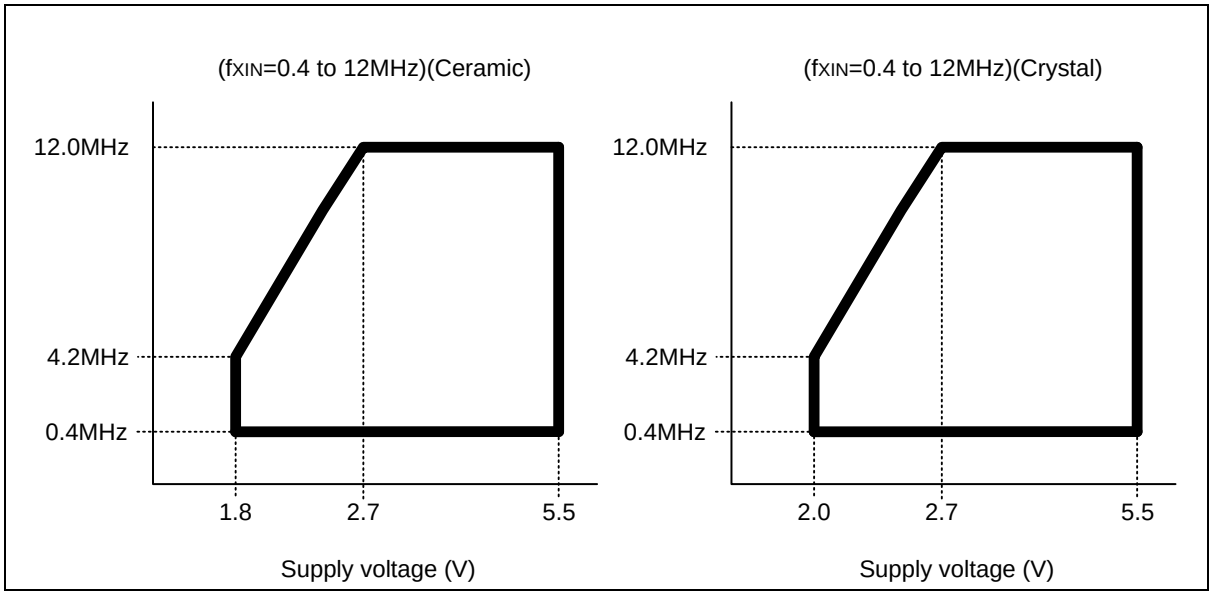


Figure 46. Operating Voltage Range

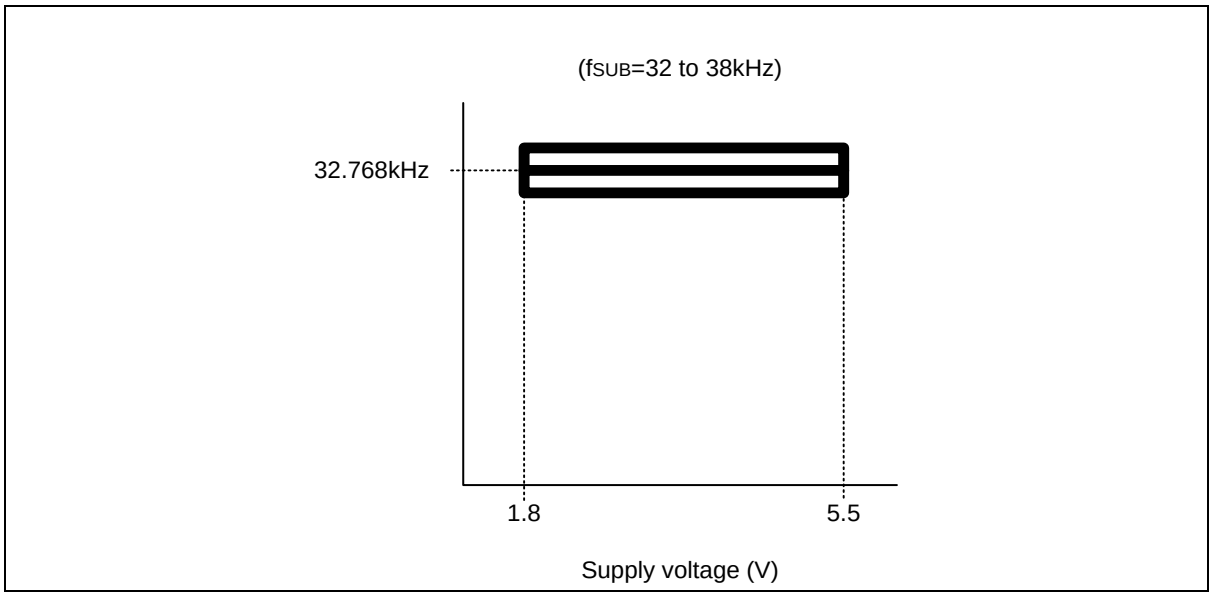


Figure 47. Operating Voltage Range (Sub OSC)

20.22 Recommended circuit and layout

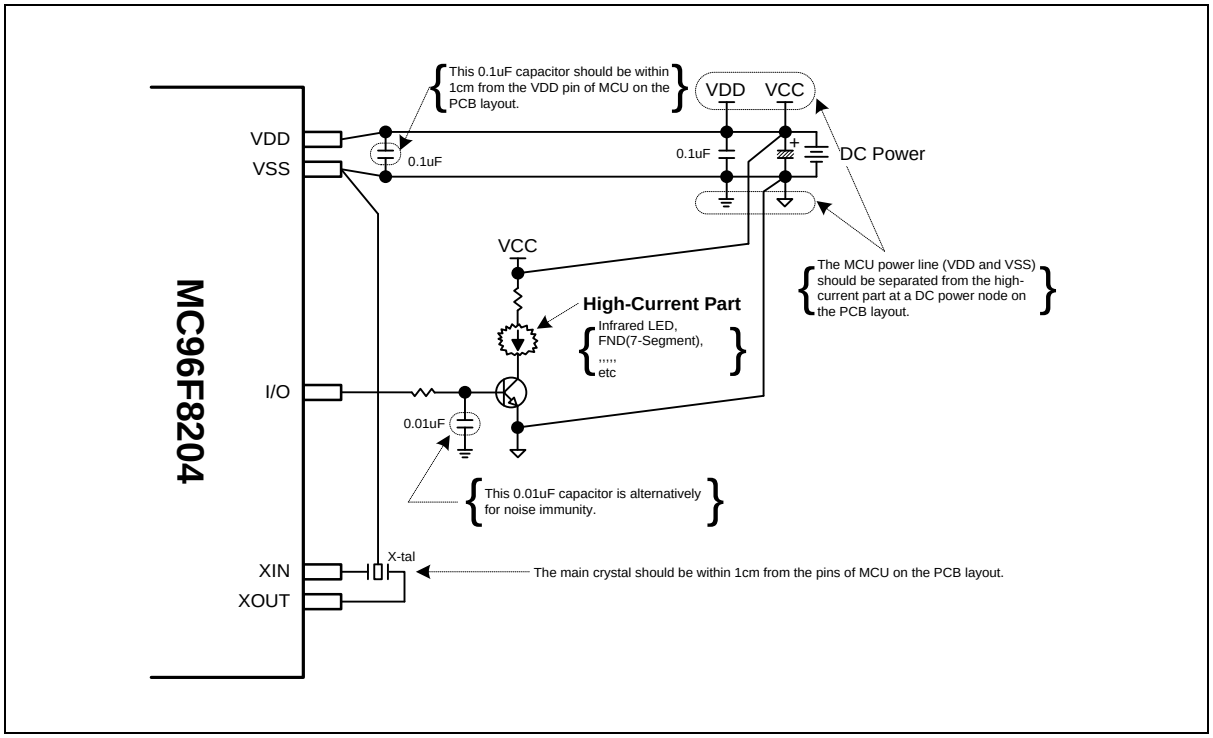


Figure 48. Recommended Circuit and Layout for Main X-TAL OSC

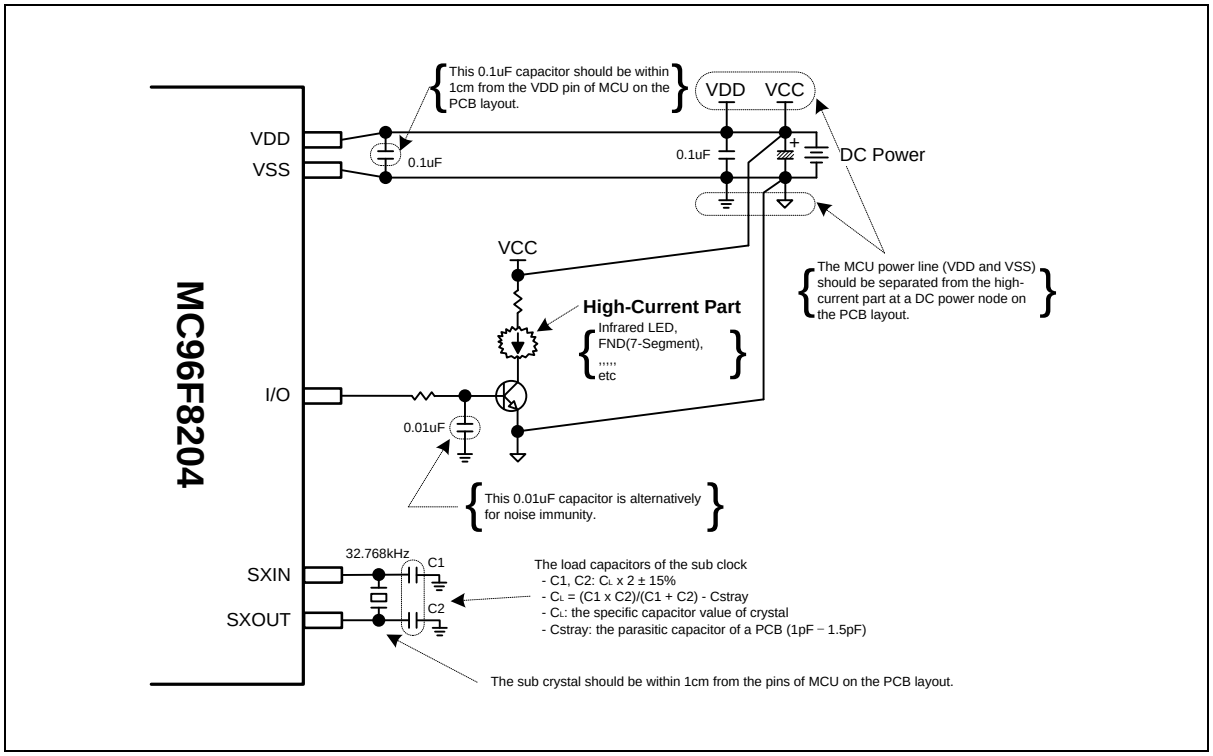
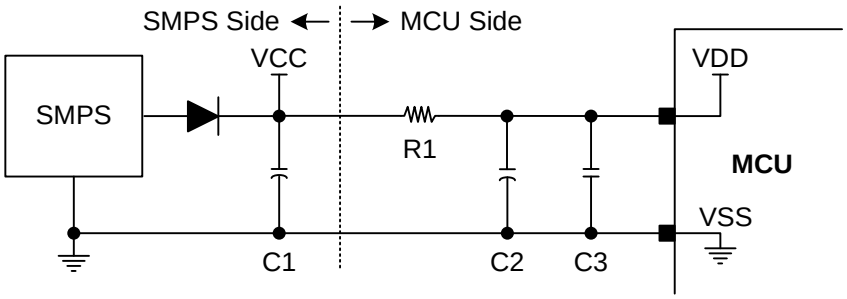


Figure 49. Recommended Circuit and Layout for Sub X-TAL OSC

20.23 Recommended circuit and layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 50. Recommended Circuit and Layout with SMPS Power

20.24 Typical characteristics

Figures and tables introduced in this chapter can be used only for design guidance and are not tested or guaranteed. In graphs or tables some data may exceed specified operating range and can be only for information. The device is guaranteed to operate properly only within the specified range.

The data presented in this chapter is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

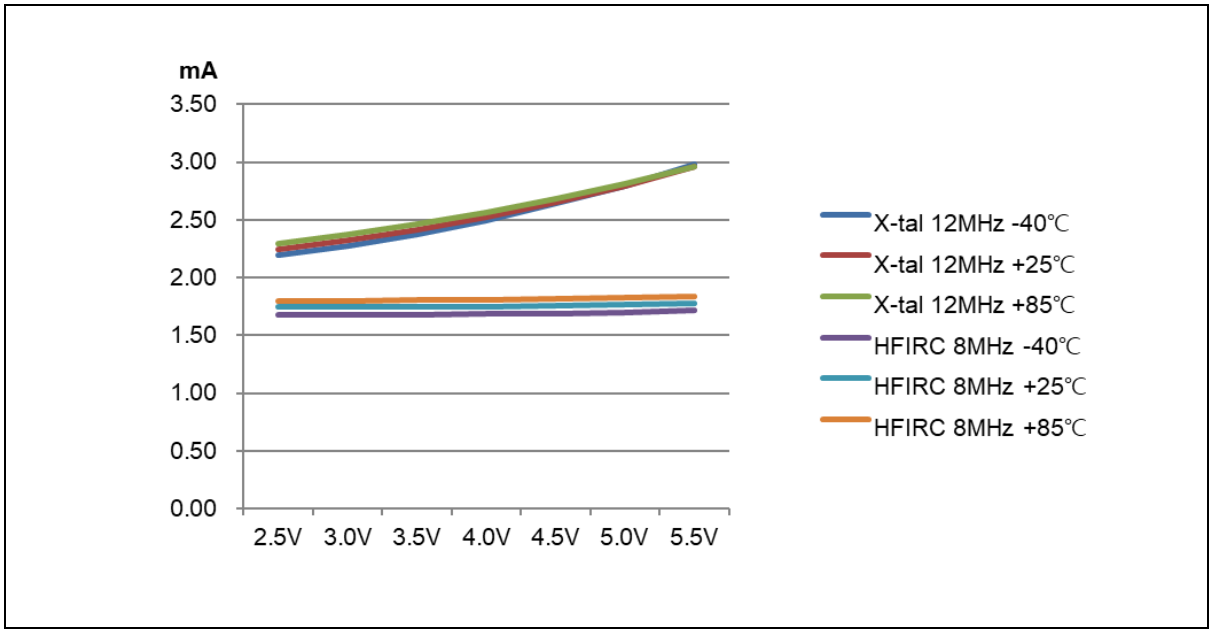


Figure 51. X-TAL, HFIRC RUN (IDD1) Current

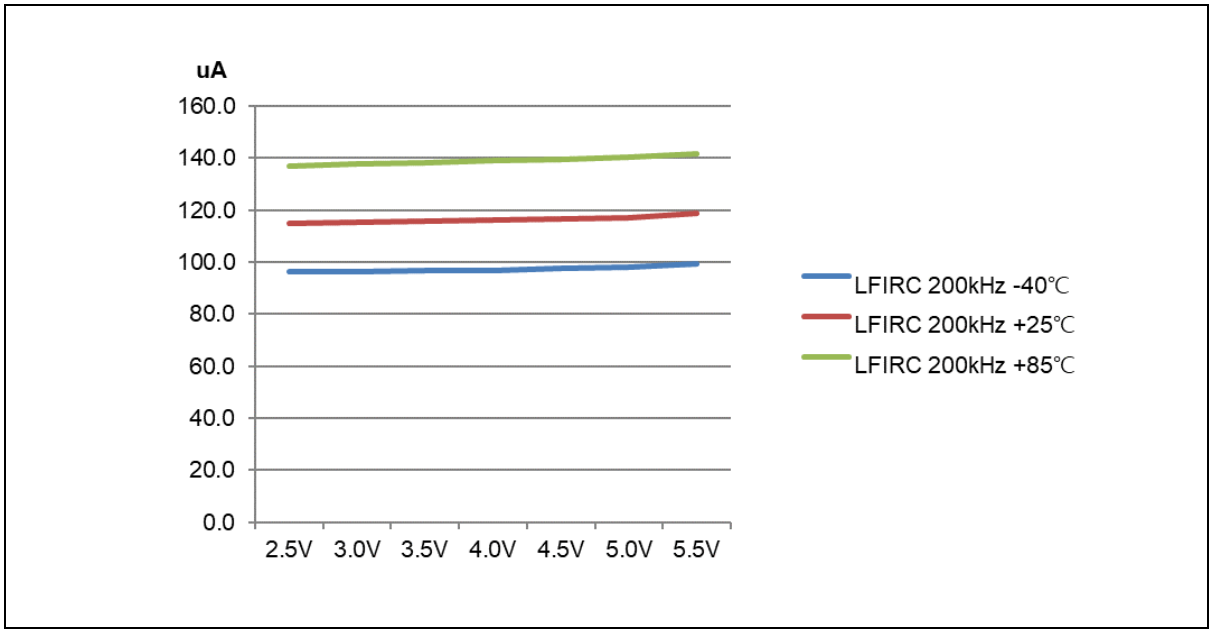


Figure 52. LFIRC RUN (IDD1) Current

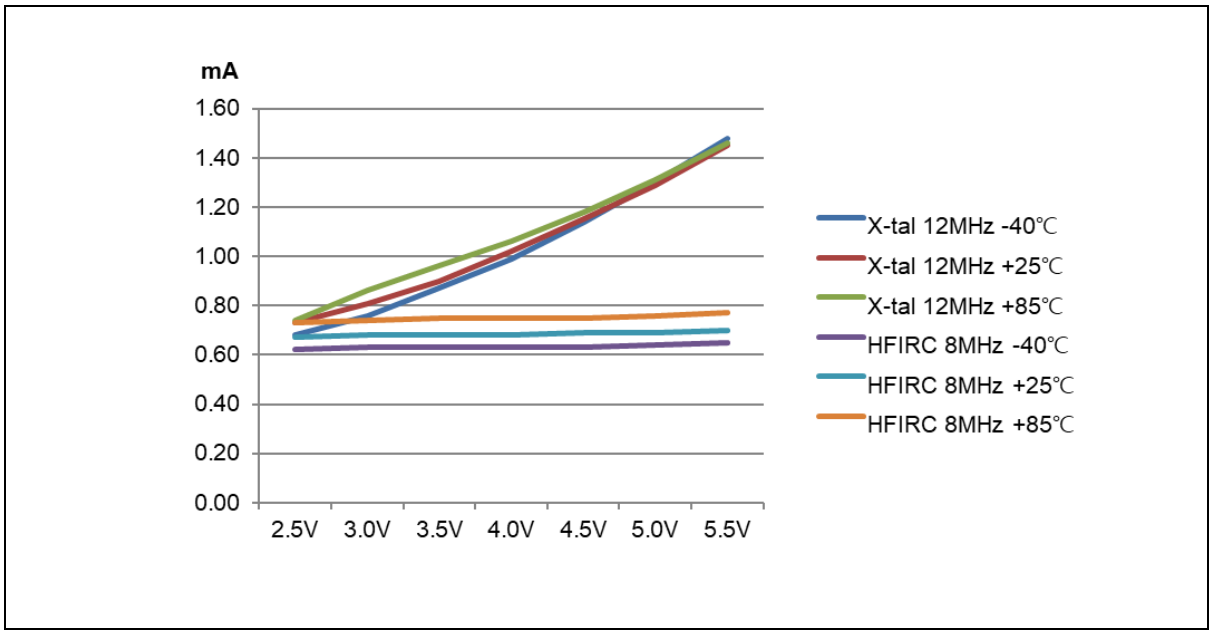


Figure 53. X-TAL, HFIRC IDLE (IDD2) Current

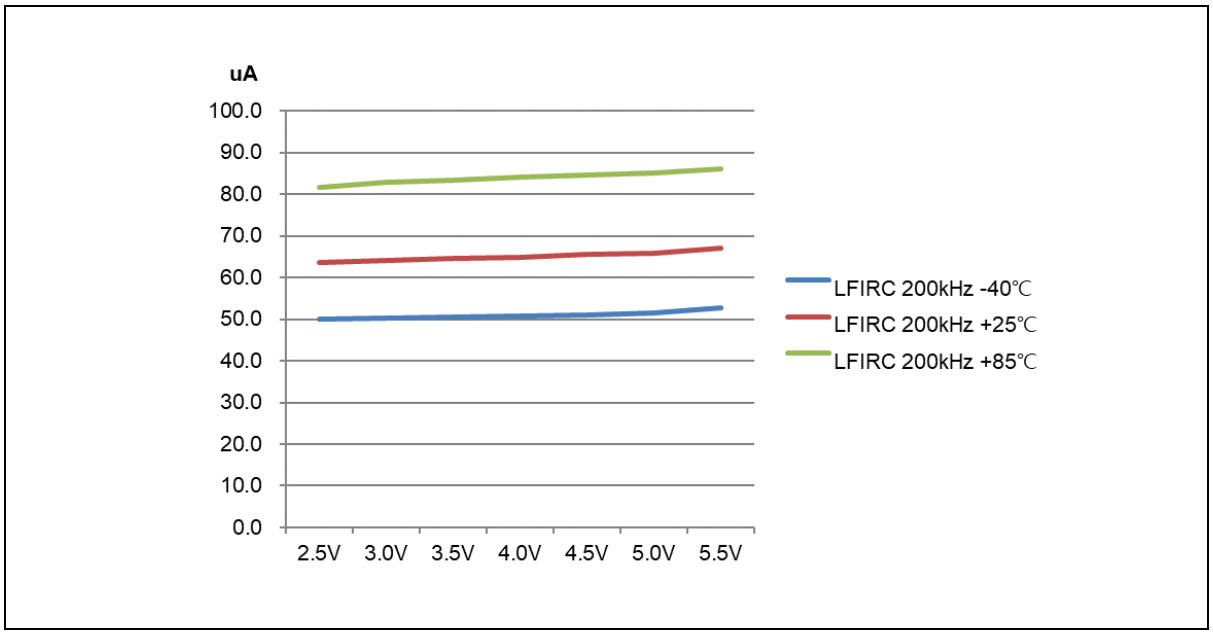


Figure 54. LFIRC IDLE (IDD2) Current

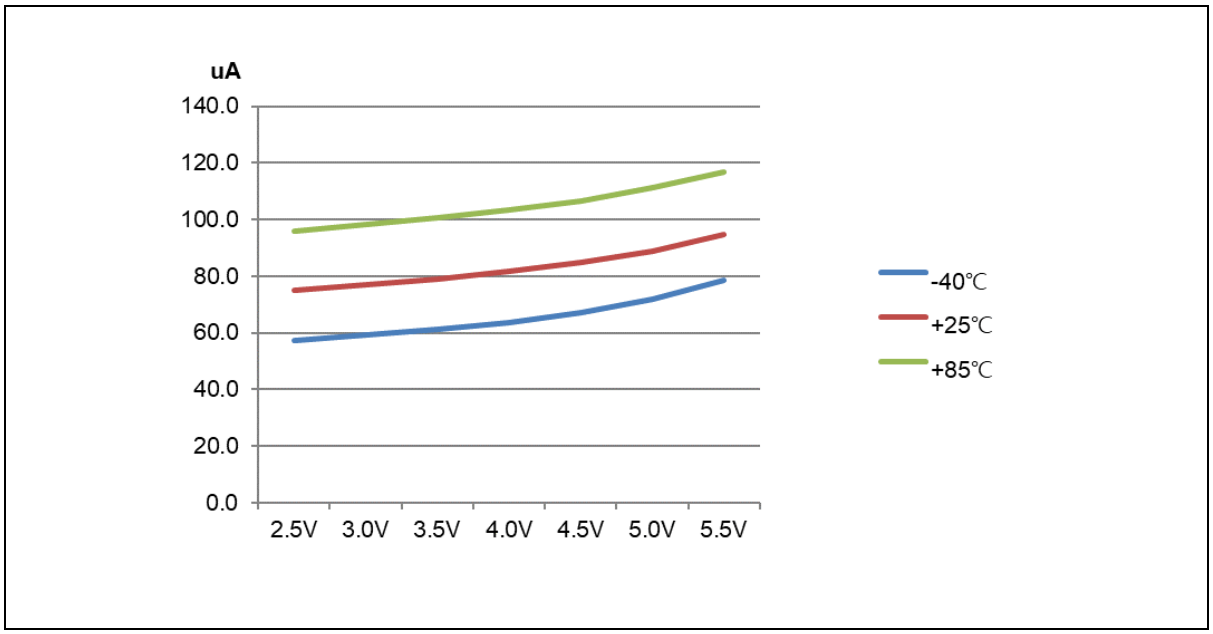


Figure 55. SUB RUN (IDD3) Current

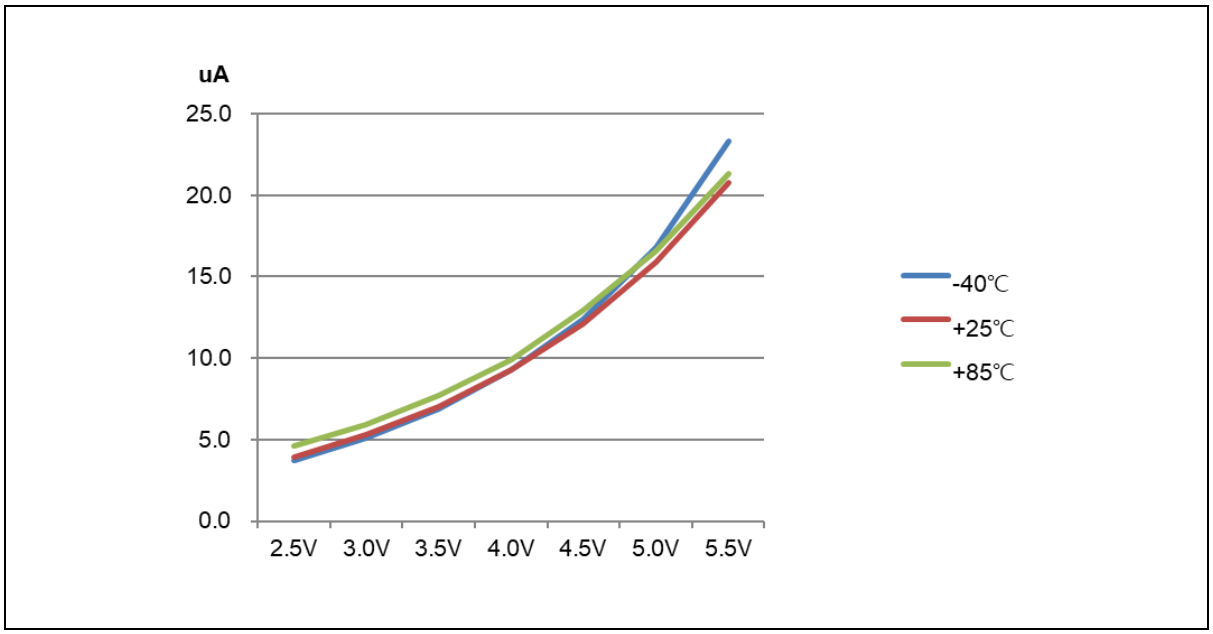


Figure 56. SUB IDLE (IDD4) Current

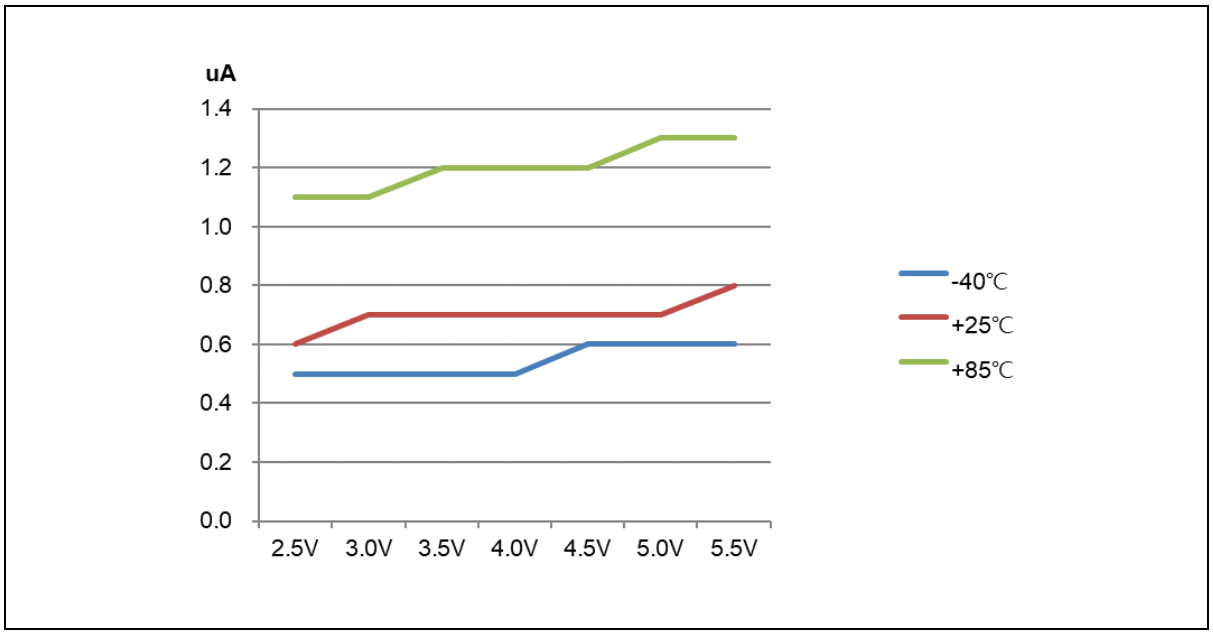


Figure 57. STOP (IDD5) Current

21 Development tools

This chapter introduces wide range of development tools for MC96F8204. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

21.1 Compiler

ABOV semiconductor does not provide any compiler for MC96F8204. However, since MC96F8204 has Mentor 8051 as its CPU core, you can use all kinds of third party's standard 8051 compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Please visit our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

21.2 OCD (On-Chip Debugger) emulator and debugger

The OCD emulator supports ABOV Semiconductor's 8051 series MCU emulation. The OCD uses two wires interfacing between PC and MCU, which is attached to user's system. The OCD can read or change the value of MCU's internal memory and I/O peripherals. In addition, the OCD controls MCU's internal debugging logic. This means OCD controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the OCD is provided in section 21.5 Circuit design guide later part in this chapter. More detailed information about the OCD, please visit our website www.abovsemi.com and download the debugger S/W and documents.

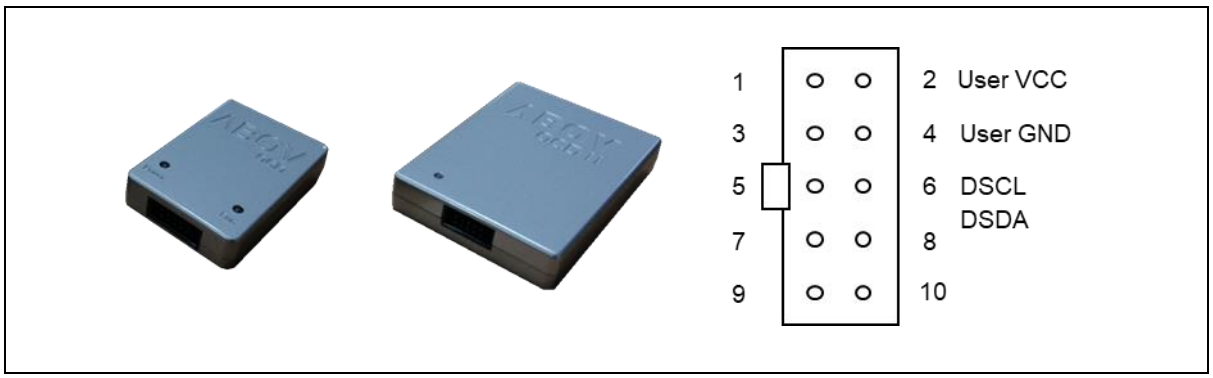


Figure 58. OCD and Pin Descriptions

Following is the OCD mode connections:

- DSCL (MC96F8204 P01 port)
- DSDA (MC96F8204 P00 port)

21.3 Programmer

E-PGM+

E-PGM+ is a single programmer and allows a user to program on the device directly.

- Support ABOV / ADAM devices
- 2~5 times faster than S-PGM+
- Main controller : 32-bit MCU @ 72MHz
- Buffer memory : 1MB

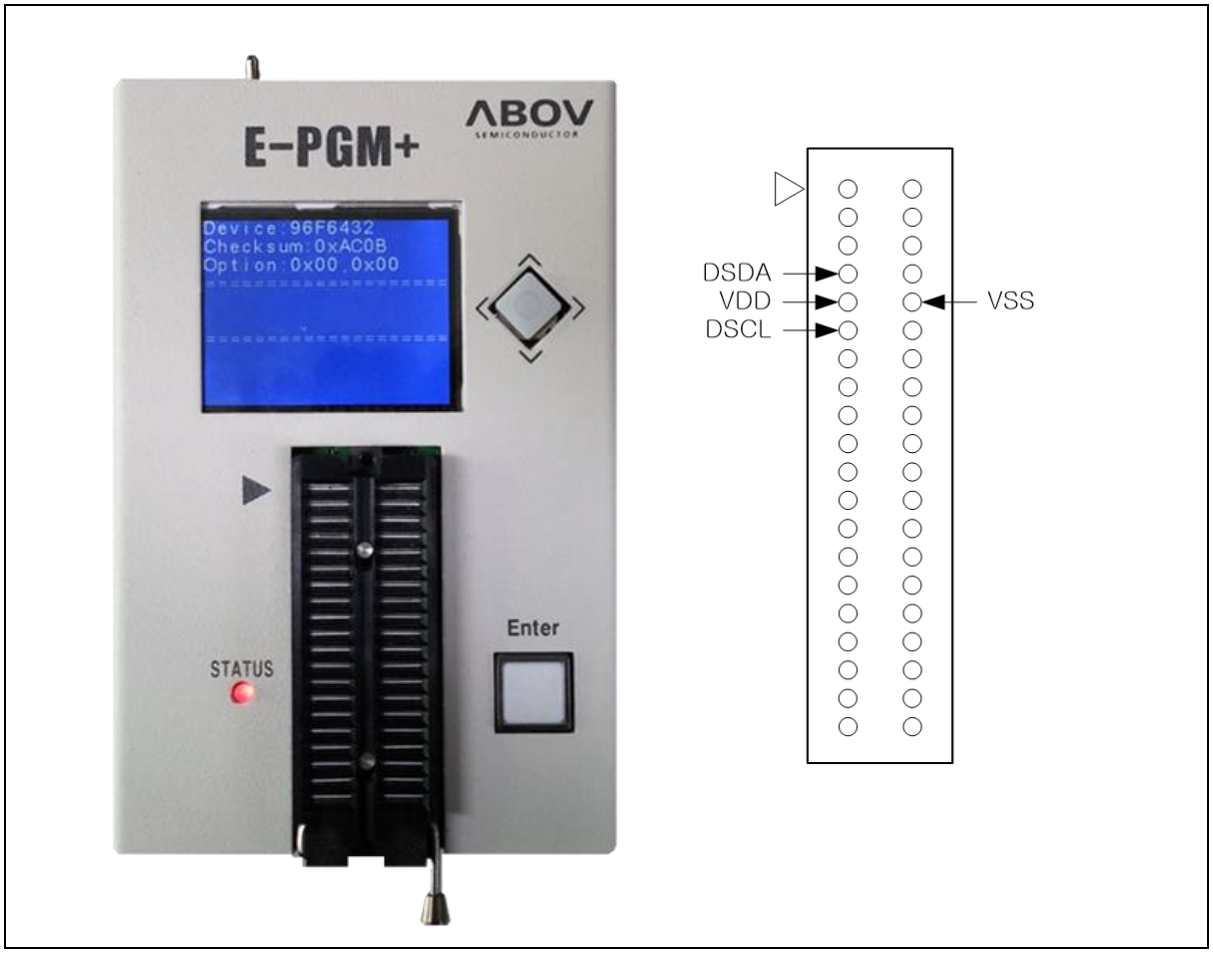


Figure 59. E-PGM+ (Single Writer) and Pin Descriptions

OCD emulator

OCD emulator allows a user to write code on the device too, since OCD debugger supports ISP (In System Programming). It doesn't require additional H/W, except developer's target system.

Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Table 35. Specification of E-Gang4 and E-Gang6

Gang programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x35mm	148.2 x 22.5 x35mm
Weight	2.0kg	2.8kg
Input voltage	DC Adaptor 15V/2A	DC Adaptor 15V/2A
Operating temperature	-10 ~ 40℃	-10 ~ 40℃
Storage temperature	-30 ~ 80℃	-30 ~ 80℃
Waterproof	No	No

Figure 60. E-Gang4 and E-Gang6 (for Mass Production)

21.4 MTP programming

Program memory of MC96F8204 is an MTP Type. This flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. Table 36 introduces each pin and corresponding I/O status.

Table 36. Pins for MTP Programming

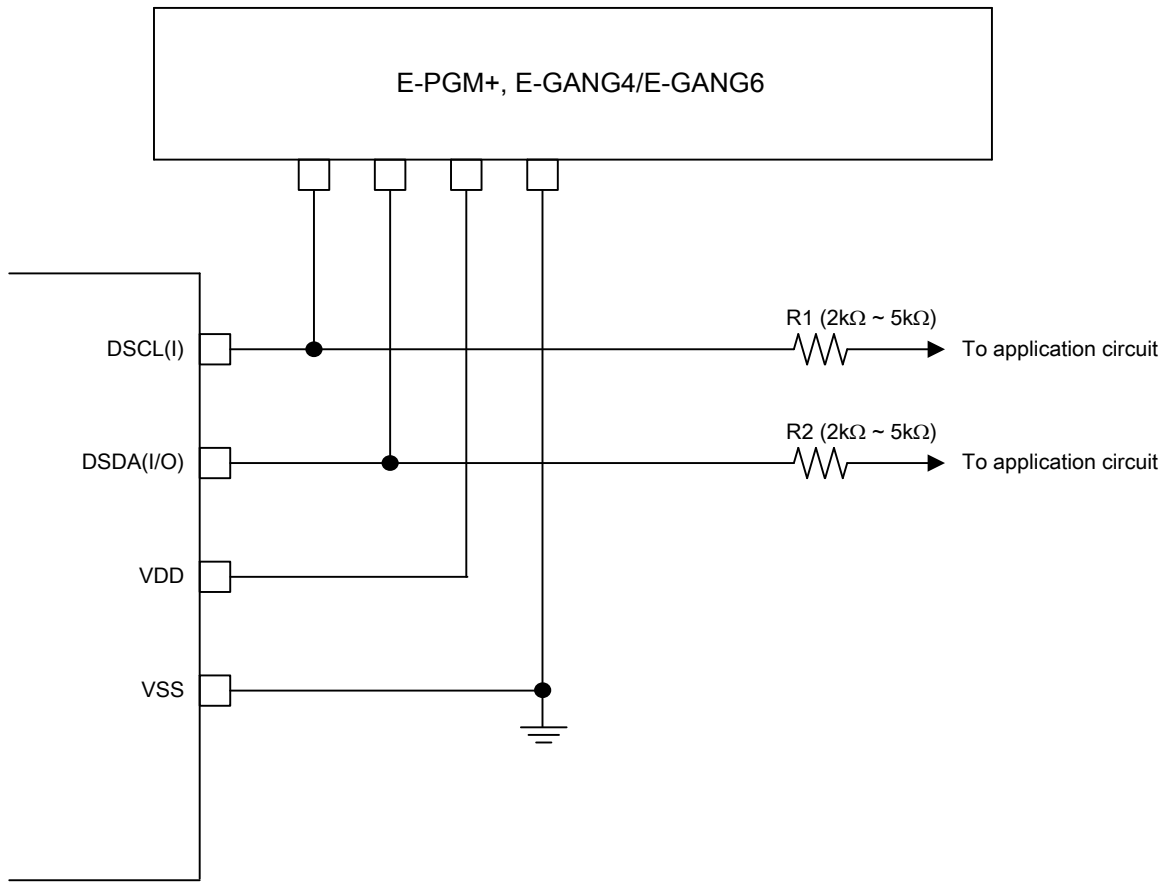
Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	–	Logic power supply pin.

On-board programming

The MC96F8204 needs only four signal lines including VDD and VSS pins for programming flash with serial protocol. Therefore, the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

21.5 Circuit design guide

When programming flash memory, the programming tool needs 4 signal lines, DSCL, DSDA, VDD, and VSS. When you design a PCB circuit, you should consider the usage of these 4 signal lines for the on-board programming.



NOTES:

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high-speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 61. PCB Design Guide for On-Board Programming

21.5.1 On-Chip Debug system

Detail descriptions for programming via the OCD interface can be found in the following figures. Table 37 introduces features of OCD and figure 62 shows a block diagram of the OCD interface and the On-chip Debug system.

Table 37. Features of OCD

Two wire external interface	• 1 for serial clock input • 1 for bi-directional serial data bus
Debugger accesses	• All internal peripherals • Internal data RAM • Program Counter • Flash memory and data EEPROM memory
Extensive On-Chip Debugging supports for Break Conditions	• Break instruction • Single step break • Program memory break points on single address • Programming of Flash, EEPROM, Fuses, and Lock bits through the two-wire interface • On-Chip Debugging supported by Dr. Choice®
Operating frequency	The maximum frequency of a target MCU.

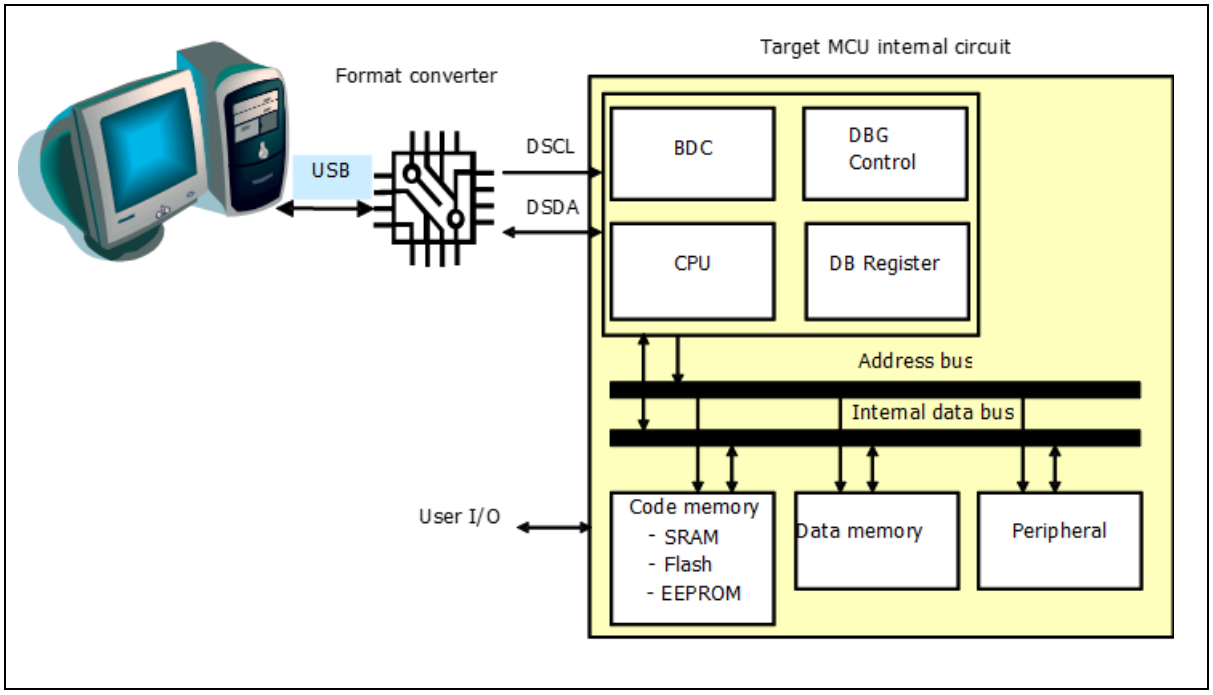


Figure 62. On-Chip Debugging System in Block Diagram

21.5.2 Two-pin external interface

Basic transmission packet

- 10-bit packet transmission using two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- Background debugger command is composed of a bundle of packet.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

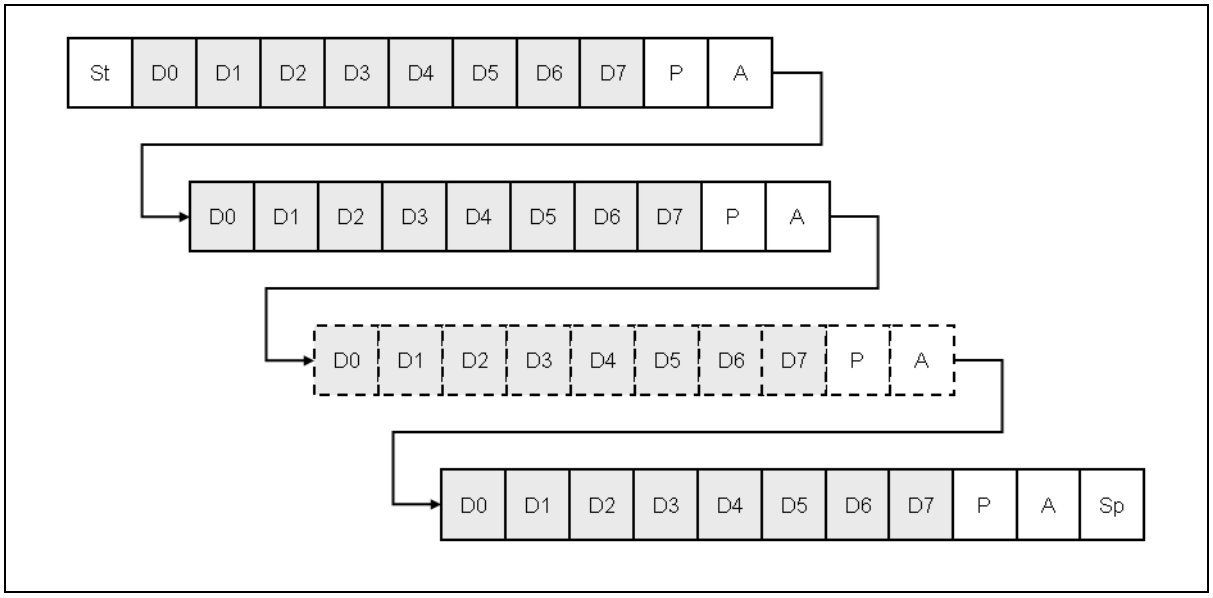


Figure 63. 10-bit Transmission Packet

Packet transmission timing

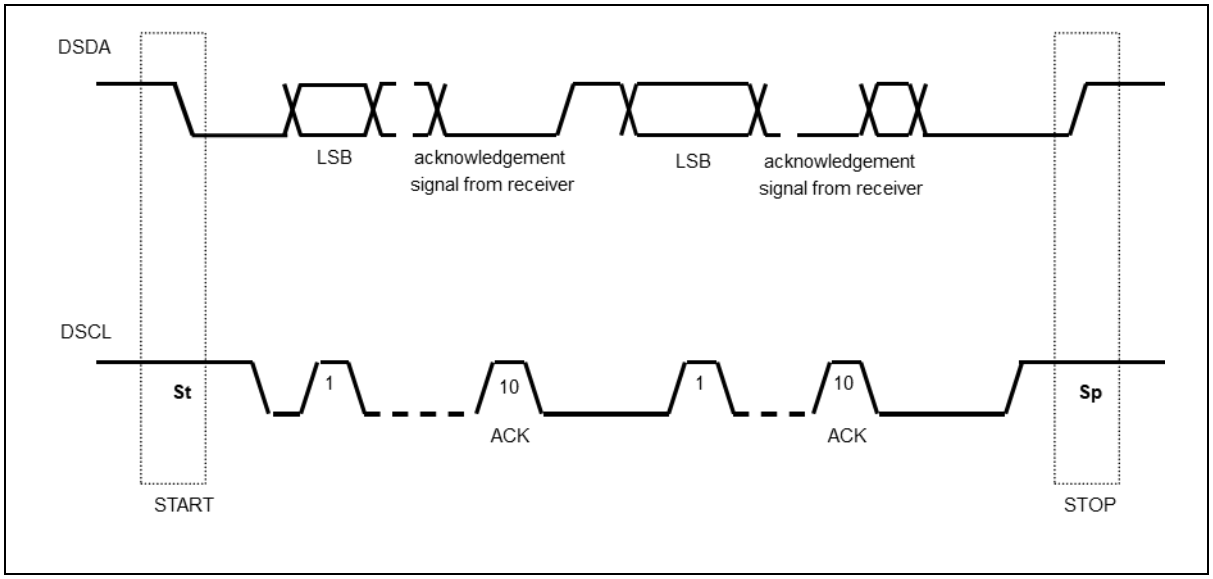


Figure 64. Data Transfer on Twin Bus

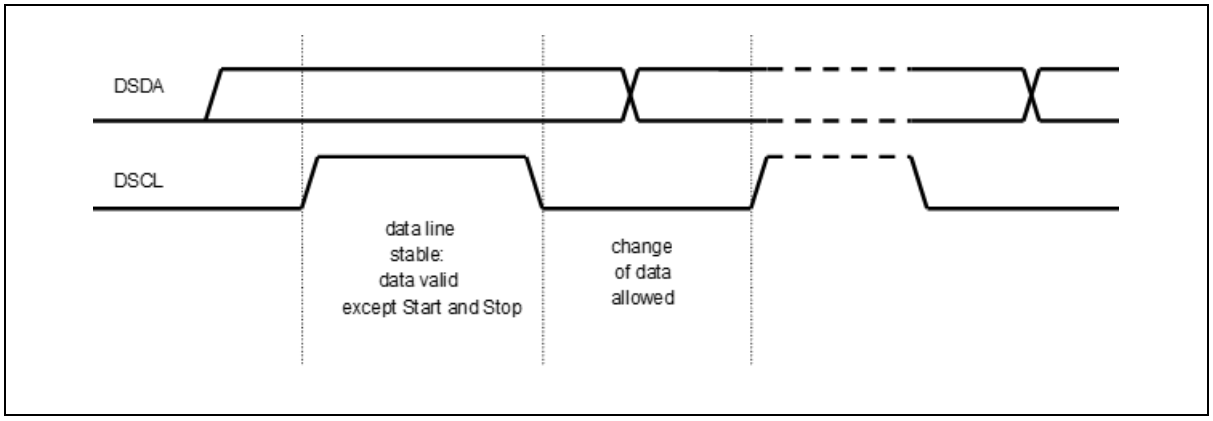


Figure 65. Bit Transfer on Serial Bus

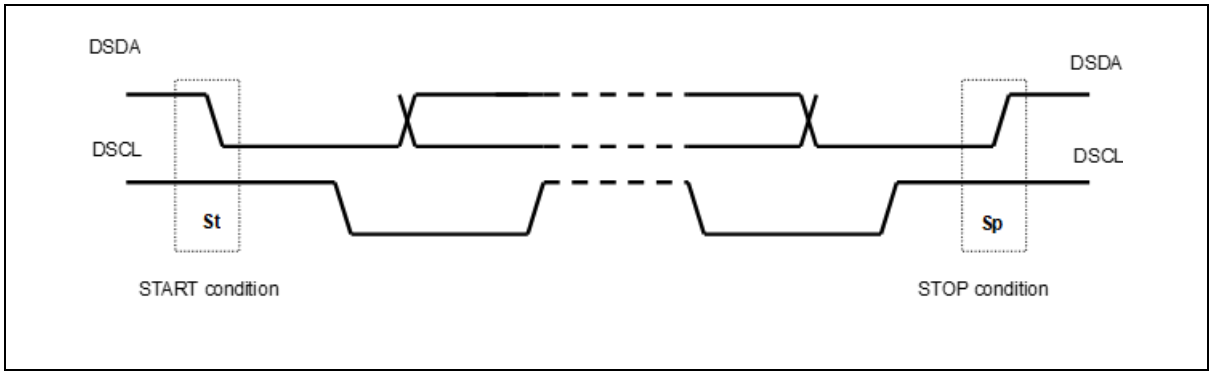


Figure 66. Start and Stop Condition

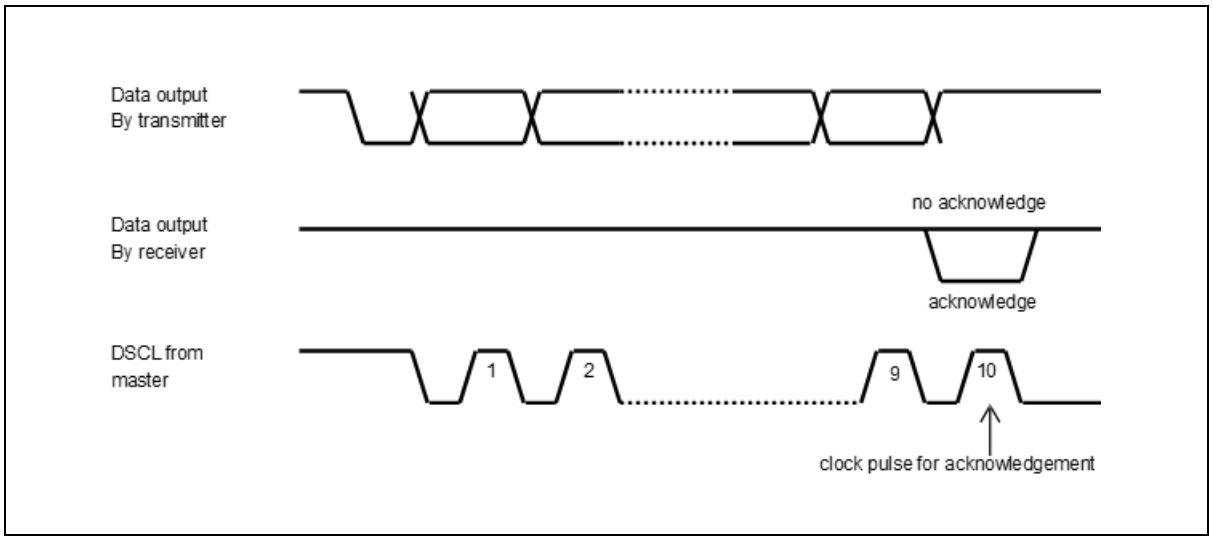


Figure 67. Acknowledge on Serial Bus

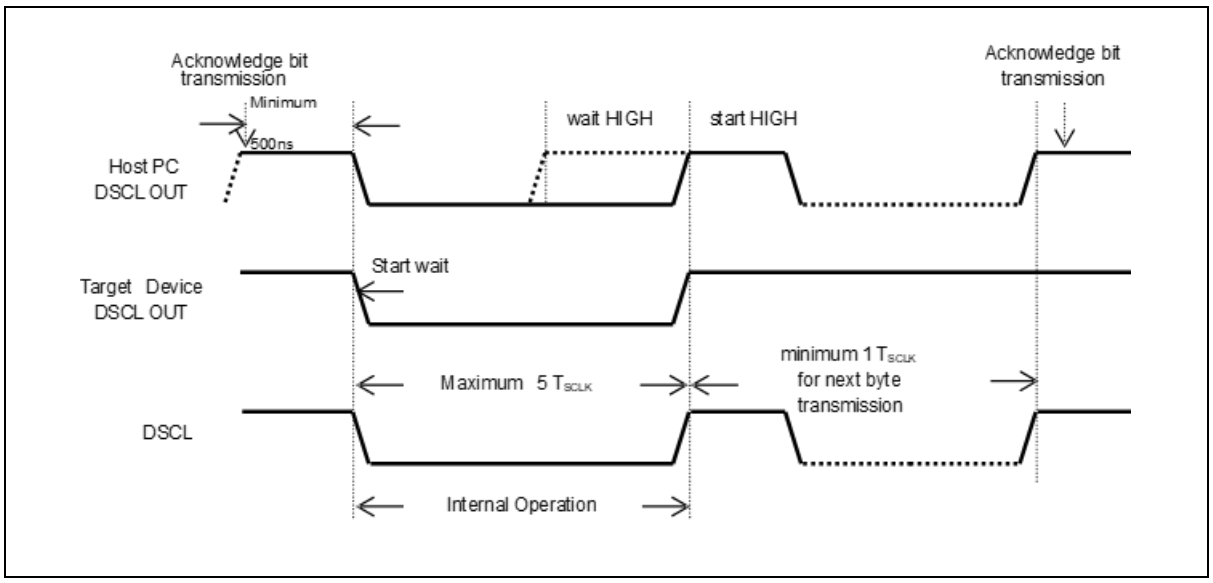


Figure 68. Clock Synchronization during Wait Procedure

21.5.3 Connection of transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

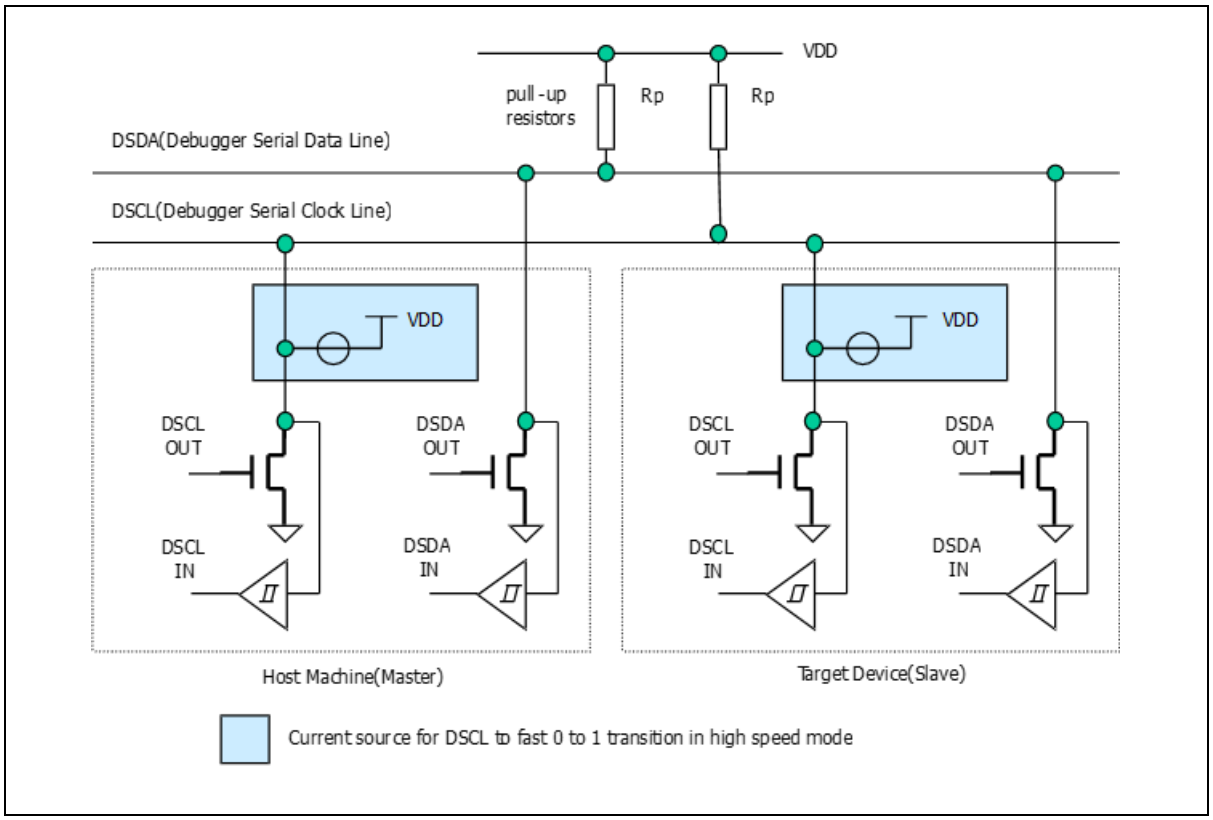


Figure 69. Connection of Transmission

22 Package information

This chapter provides MC96F8204 package information.

22.1 20 SOP package information

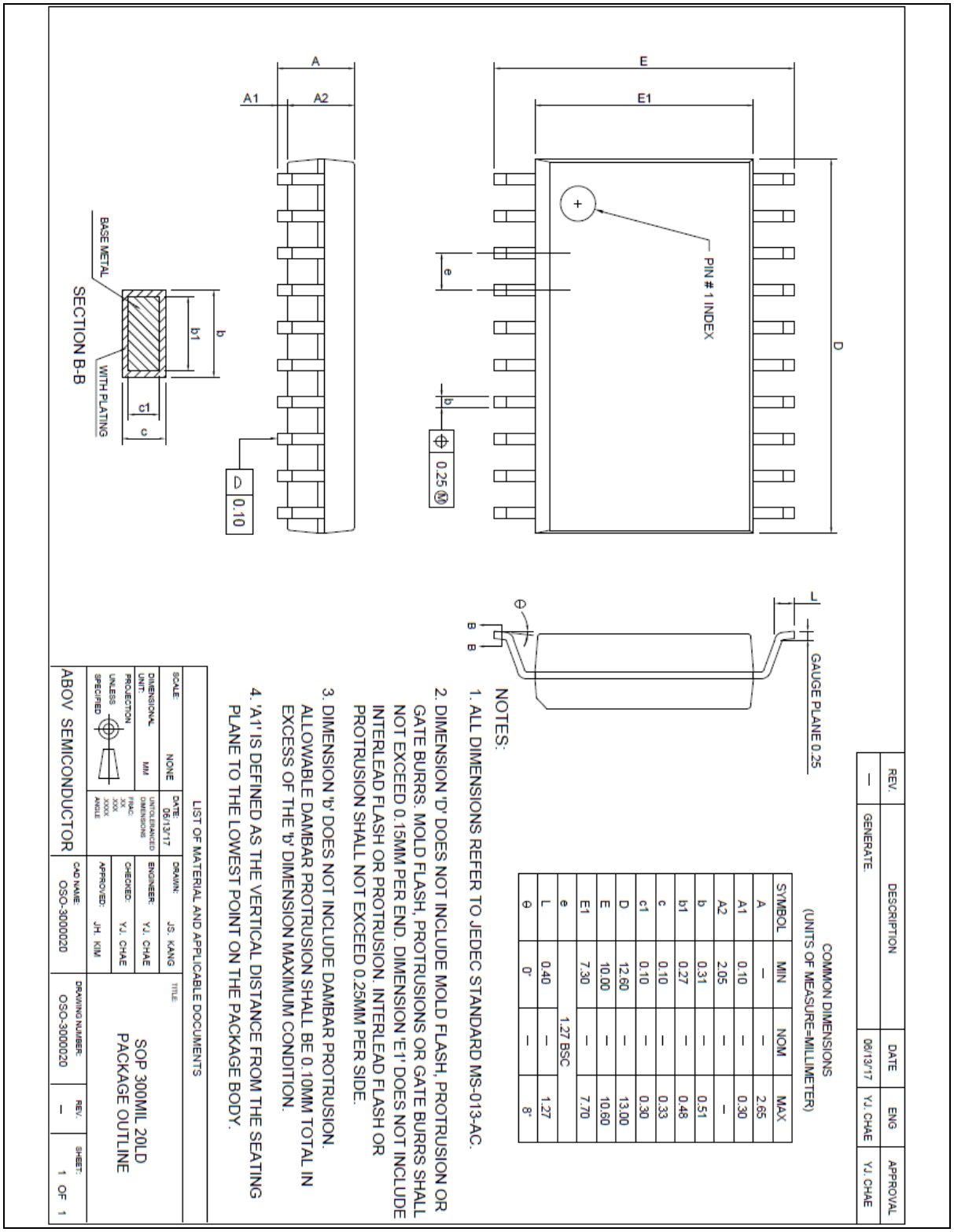


Figure 70. 20 SOP Package Outline

22.2 20 TSSOP package information

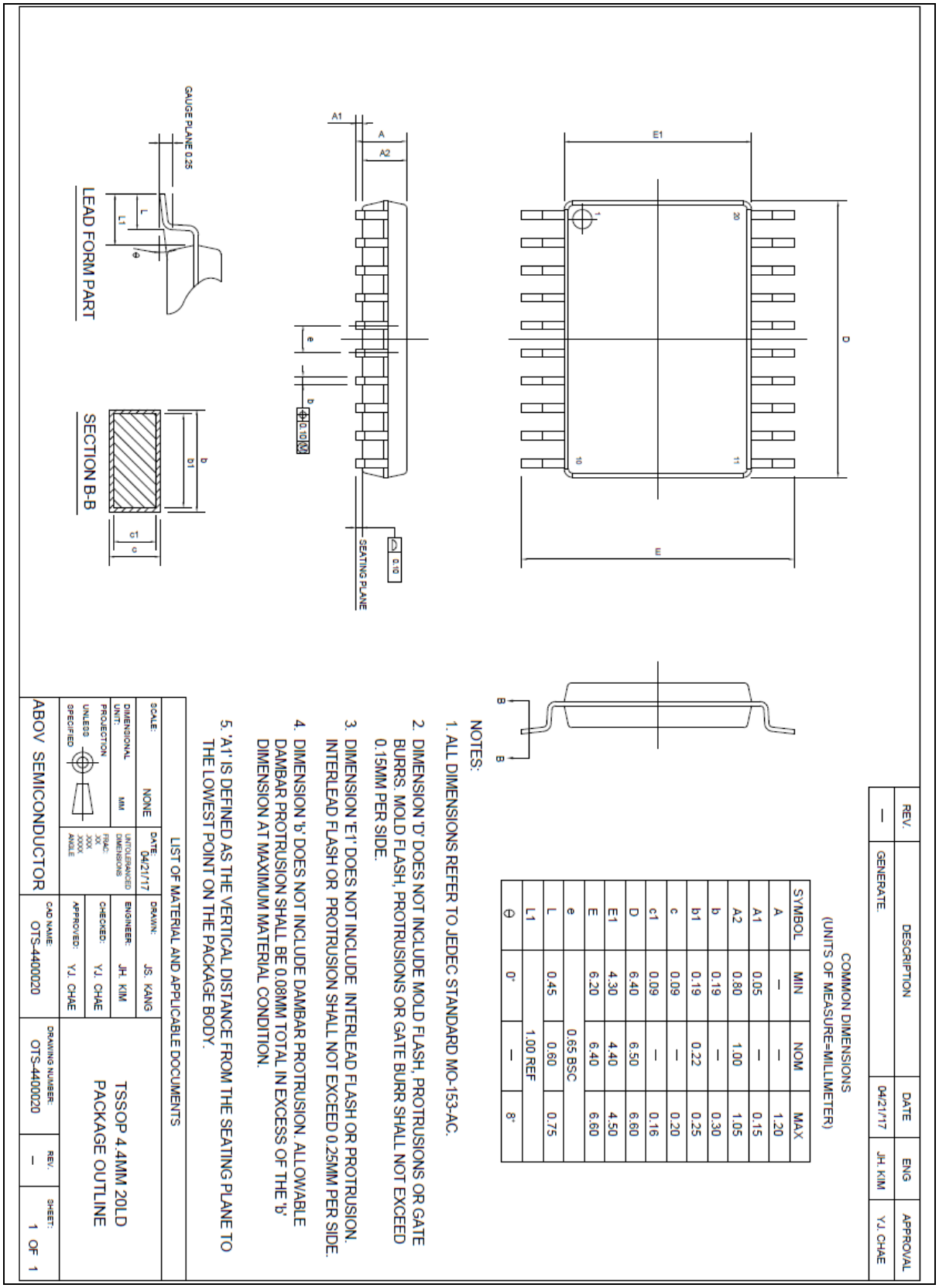


Figure 71. 20 TSSOP Package Outline

22.3 16 SOPN package information

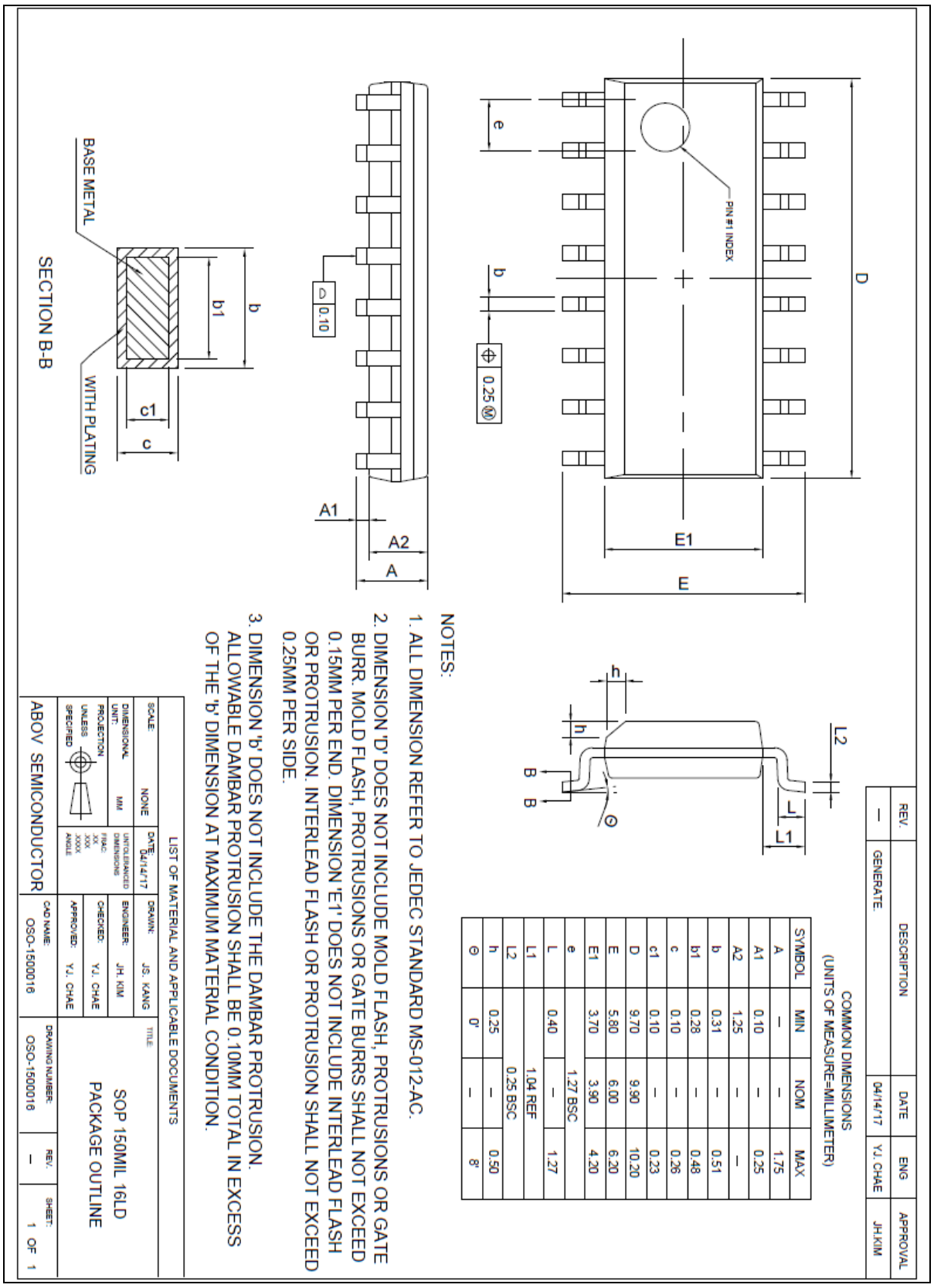
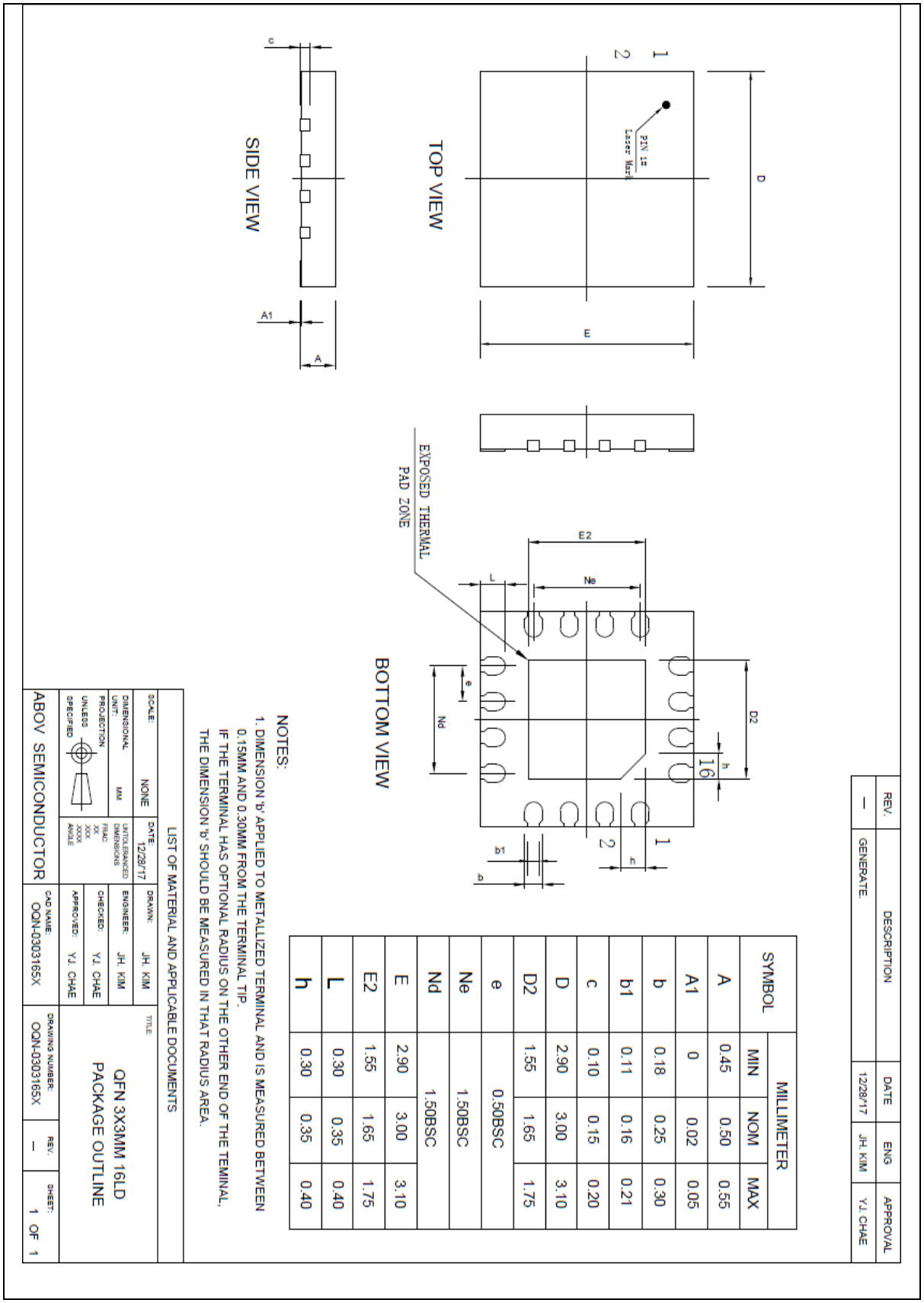


Figure 72. 16 SOPN Package Outline

22.4 16 QFN package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.18	0.25	0.30
b1	0.11	0.16	0.21
c	0.10	0.15	0.20
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e		0.50BSC	
Ne		1.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.30	0.35	0.40
h	0.30	0.35	0.40

Figure 73. 16 QFN Package Outline

22.5 10 SSOP package information

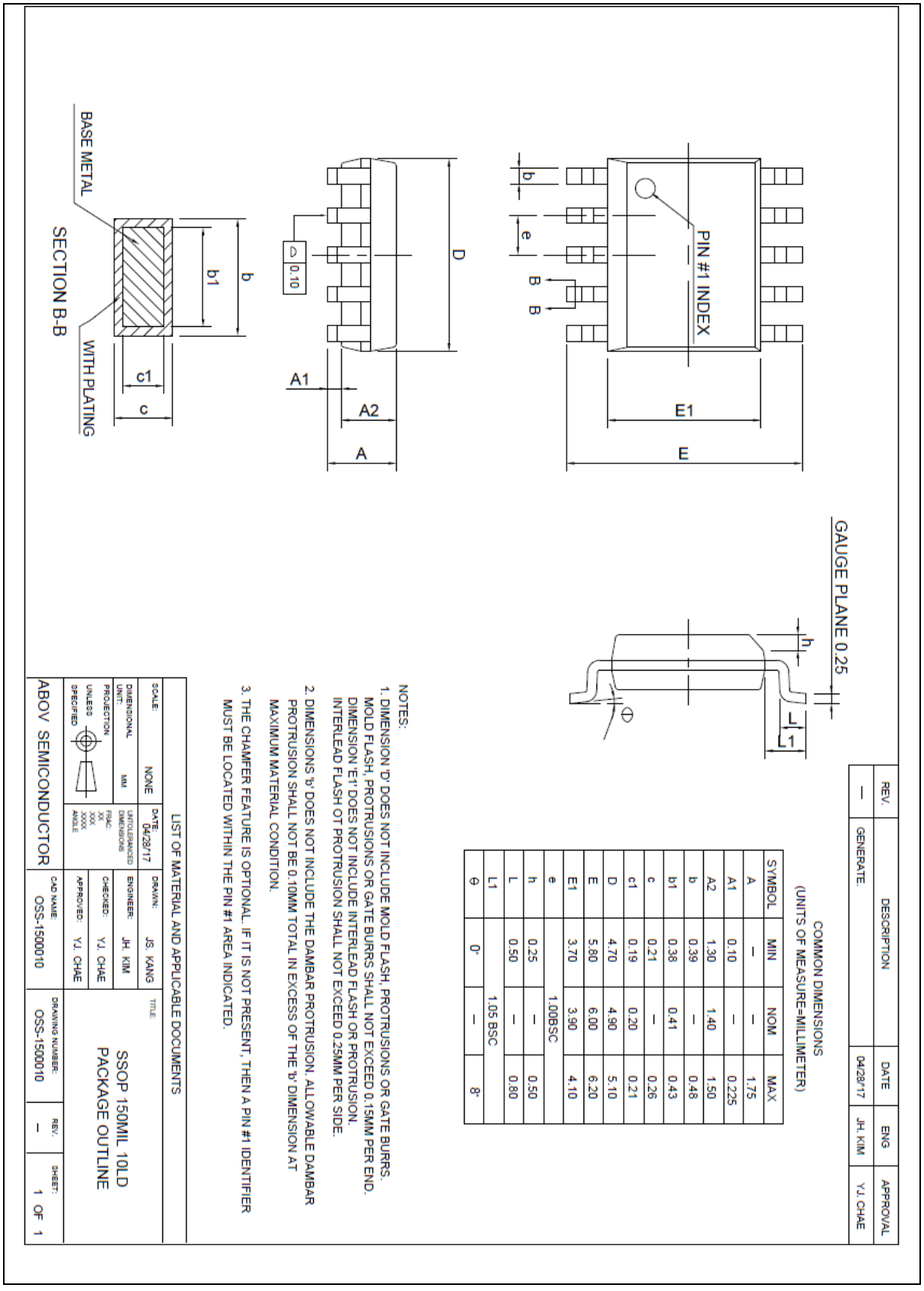


Figure 74. 10 SSOP Package Outline

22.6 8 SOP package information

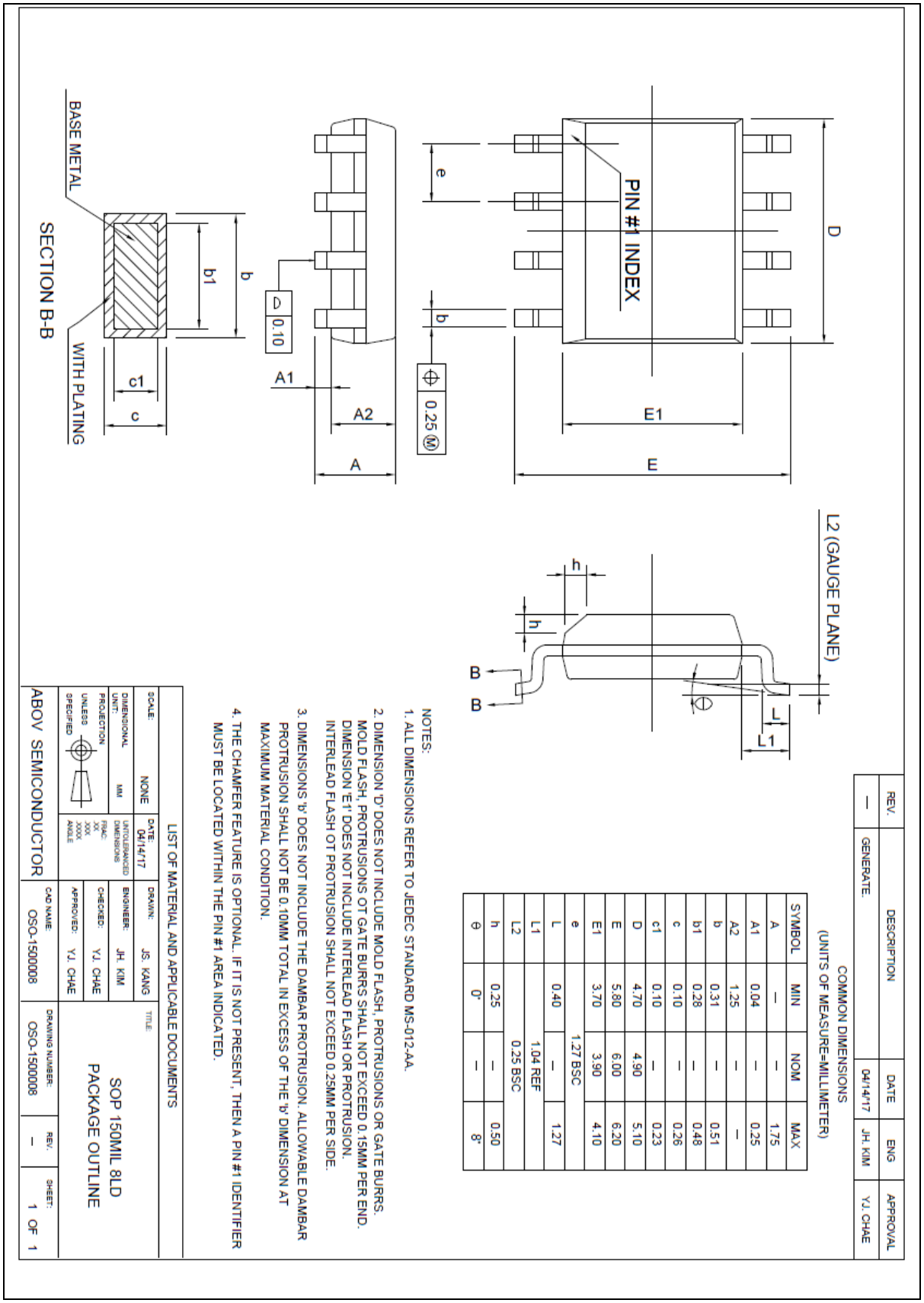


Figure 75. 8 SOP Package Outline

23 Ordering information

Table 38. MC96F8204 Device Ordering Information

Device name	Flash	IRAM	ADC	I/O ports	Package type
MC96F8204D	4 Kbytes	256 bytes	8 inputs	18	20 SOP
MC96F8204R	4 Kbytes	256 bytes	8 inputs	18	20 TSSOP
MC96F8204M	4 Kbytes	256 bytes	8 inputs	14	16 SOPN
MC96F8204U	4 Kbytes	256 bytes	8 inputs	14	16 QFN
MC96F8104S	4 Kbytes	256 bytes	8 inputs	8	10 SSOP
MC96F8104M	4 Kbytes	256 bytes	6 inputs	6	8 SOP

Appendix

A. Configure option

Register description: configure option control

CONFIGURE OPTION 1: ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value: 00H

R_P	Code Read Protection	
	0	Disable
	1	Enable
HL	Code Write Protection	
	0	Disable
	1	Enable
VAPEN	Vector Area (00H – FFH) Write Protection	
	0	Disable Protection (Erasable by instruction)
	1	Enable Protection (Not erasable by instruction)
RSTS	Select RESETB pin	
	0	Disable RESETB pin (P05)
	1	Enable RESETB pin

CONFIGURE OPTION 2: ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	–	PAEN	PASS1	PASS0

Initial value: 00H

PAEN	Enable Specific Area Write Protection		
	0	Disable (Erasable by instruction)	
	1	Enable (Not erasable by instruction)	
PASS[1:0]	Select Specific Area for Write Protection		
	NOTE: When PAEN = '1', it is applied.		
	PASS1	PASS0	Description
	0	0	3.7Kbytes (Address 0100H – 0F7FH)
	0	1	1.7Kbytes (Address 0100H – 07FFH)
	1	0	1Kbytes (Address 0100H – 04FFH)
	1	1	256bytes (Address 0100H – 01FFH)

B. Instruction table

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column in tables shown below.
- Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following tables in this section.
- 1 machine cycle comprises 2 system clock cycles.

Table 39. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DA A	Decimal Adjust A	1	1	D4

Table 40. Instruction Table: Logical

Logical				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 41. Instruction Table: Data Transfer

Data Transfer				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 42. Instruction Table: Boolean

Boolean				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 43. Instruction Table: Branching

Branching				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 44. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
NOP	No operation	1	1	00

Table 45. Instruction Table: Additional Instructions

Additional instructions (selected through EO[7:4])				
Mnemonic	**Description**	**Bytes**	**Cycles**	**Hex code**
MOVC @(DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5

TRAP	Software break command	1	1	A5

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, and the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

C. Flash protection for invalid erase/ write

Appendix C shows example code to prevent code or data from being changed by abnormal operations such as noise, unstable power, and malfunction.

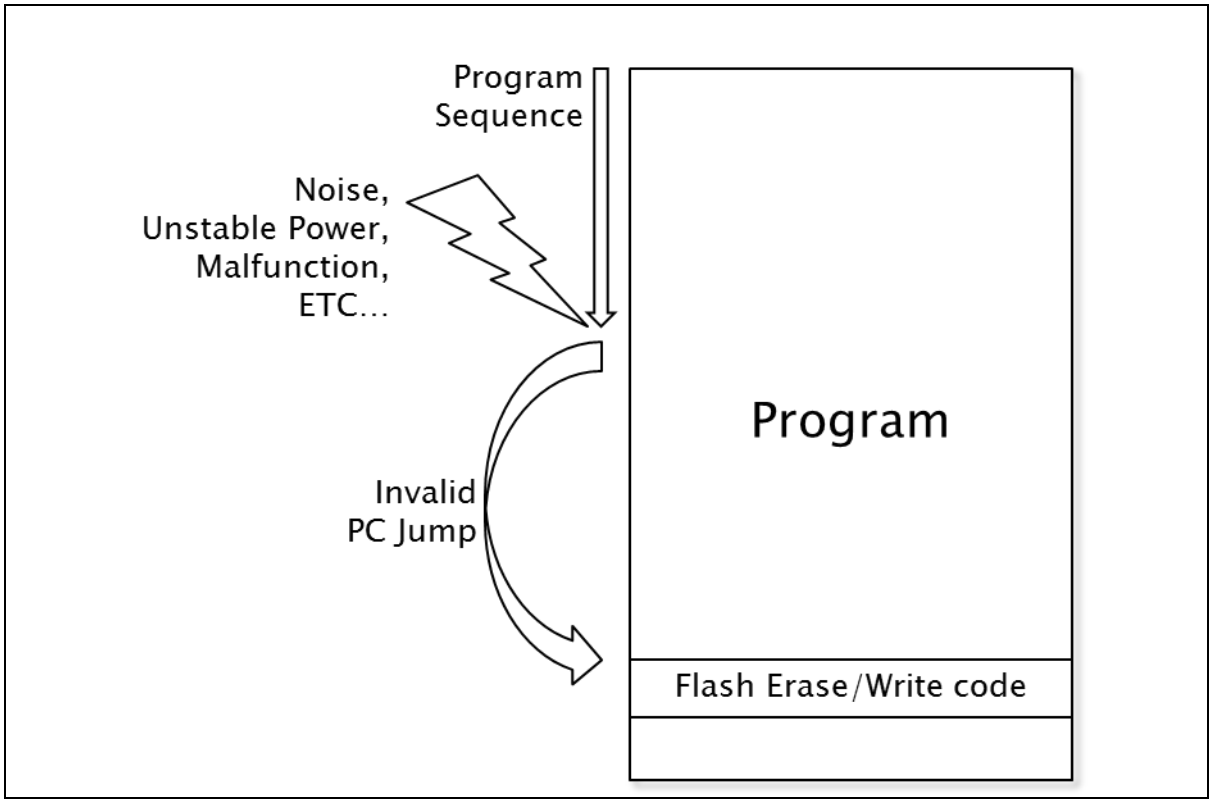


Figure 76. Flash Protection against Abnormal Operations

How to protect the flash

- Divide into decision and execution to Erase/Write in flash.
  - Check the program sequence from decision to execution in order of precedence about Erase/Write.

  - Setting the flags in program and check the flags in main loop at the end
  - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
  - If the flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
  - Set the flash sector address to dummy address in usually run time.
  - Change the flash sector address to real area range shortly before Erase/Write.
  - Even if invalid Erase/Write occurred, it will be Erase/Write in dummy address in flash.
- Use the LVR/LVI
  - Unstable or low powers give an adverse effect on MCU. So, use the LVR/LVI

Protection flow description

The flash protection procedure is described in flowchart in figure 77, and each step in the figure 77 is introduced in the following lists:

1. Initialization
   - Set the LVR/LVI. Check the power by LVR/LVI and do not execute under unstable or low power.
   - Initialize User_ID1/2/3
   - Set Flash Sector Address High/Middle/Low to Dummy address. Dummy address is set to unused area range in flash.
2. Decide to Write
   - When the Erase/Write are determined, set flag. Do not directly Erase/Write in flash.
   - Make the user data.
3. Check and Set User_ID1/2/3
   - In the middle of source, insert code which can check and set the flags.
   - By setting the User_ID 1/2/3 sequentially and identify the flow of the program.
4. Set Flash Sector Address
   - Set address to real area range shortly before Erase/Write in flash.
   - Set to Dummy address after Erase/Write. Even if invalid work occurred, it will be Erase/Write in Dummy address in flash.
5. Check Flags
   - If every flag (User_ID1/2/3, LVI, Flash Address Min/Max) was set, than do Erase/Write.
   - If the Flash Sector Address is outside of Min/Max, do not execute

- Address Min/Max is set to unused area.

6. Initialize Flags
   - Initialize User_ID1/2/3
   - Set Flash Sector Address to Dummy Address

- Sample Source
  - Refer to the ABOV website (www.abovsemi.com).
  - It is created based on the MC97F2664.
  - Each product should be modified according to the Page Buffer Size and Flash Size.

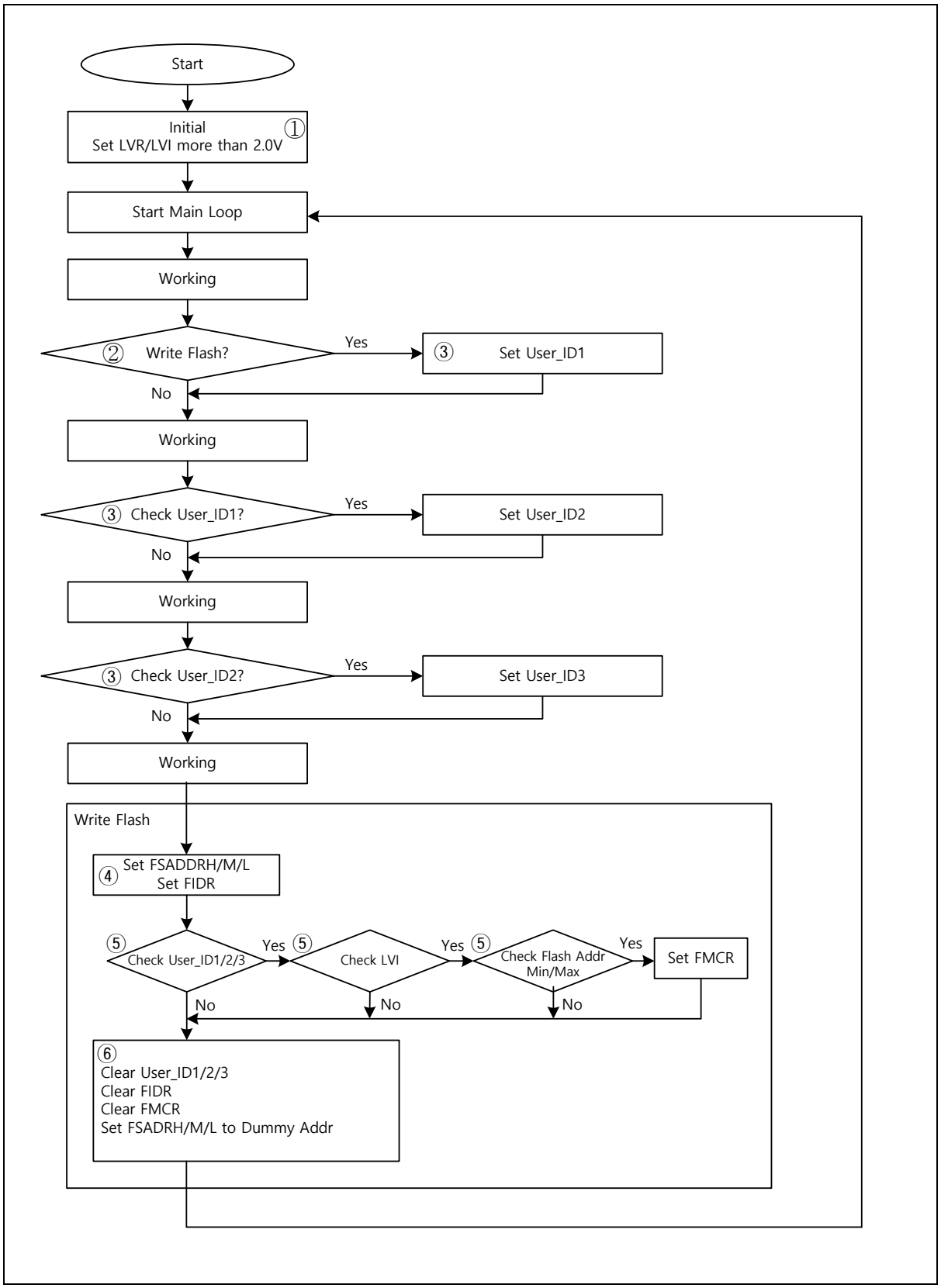


Figure 77. Flowchart of Flash Protection

Other protection by the configure options

- Protection by Configure option
  - Set flash protection by MCU Write Tool (OCD, PGM+, etc.)

    Vector Area:

    00H~FFH

    Specific Area:

    3.7KBytes (Address 0100H – 0F7FH)

    1.7KBytes (Address 0100H – 07FFH)

    1KBytes (Address 0100H – 04FFH)

    256Bytes (Address 0100H – 01FFH)
  - The range of protection may be different each product.

Revision history

Date	Revision	Description
Mar. 14, 2016	1.0	Published this book.
Apr. 8, 2016	1.1	Change tR spec max value from 5.0V/ms to 30.0V/ms in 7.4 Power-On Reset. Add a chapter 7.23 Recommended Circuit and Layout with SMPS Power. Modify the program tips in Chapter 15. Flash Memory. Add an appendix about “Flash Protection for invalid Erase/Write” Fix typos.
Mar. 17, 2016	1.2	Fix typo of 8SOP package device name (MC96F8104M). Fix typos of I2C Status Register in chapter 11.9 I2C.
Sep. 8, 2016	1.3	Remove packages the 20 QFN, 16 TSSOP, 16 QFN, 8 PDIP. Modify package from 16 SOP to 16 SOPN.
Dec. 21, 2016	1.4	Updated OCD dongle image and writing tool images in chapter 1.3 Development tools. Fix typos of T0/T1/T2
Jan. 20, 2017	1.5	Added the note on the flash memory erase and write in chapter 15. Flash Memory. Fix typos of I2C Status Register in chapter 11.9 I2C.
Sep. 29, 2017	1.6	Added the maximum allowable current (IIK) in chapter 7.1 Absolute Maximum Ratings. Updated package diagrams in chapter 4. Package Diagram.
Nov. 3, 2017	1.7	Added table for ADC characteristic under 2.7V. Added program tip for ADC register setting. Added timing chart for Debounce function. Removed the maximum allowable current (IIK) in chapter 7.1 Absolute Maximum Ratings. Added the maximum allowable voltage (VIK) in chapter 7.1 Absolute Maximum Ratings.
Dec. 19, 2017	1.8	Add 16 QFN package type. Add Device Nomenclature.
Dec. 28, 2017	1.9	Added the recommended operating conditions for IRC during power-up in chapter 7.2 Recommended Operating Conditions. Updated 16 QFN package diagram in chapter 4. Package Diagram.
Mar. 21, 2018	1.10	Change tR spec min value in 7.4 Power-On Reset.
Jun. 14, 2018	1.11	Revised this book.

		Change Endurance of Write/Erase times in 7.15 Internal Flash Rom Characteristic.
May. 11, 2020	1.12	Updated new format.

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