

Dual N-Channel 30-V (D-S) MOSFET

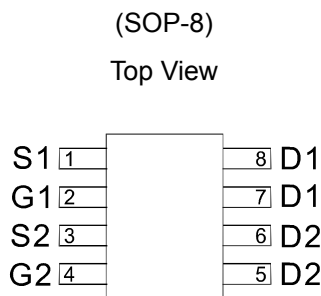
GENERAL DESCRIPTION

The ME4920 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

PIN CONFIGURATION



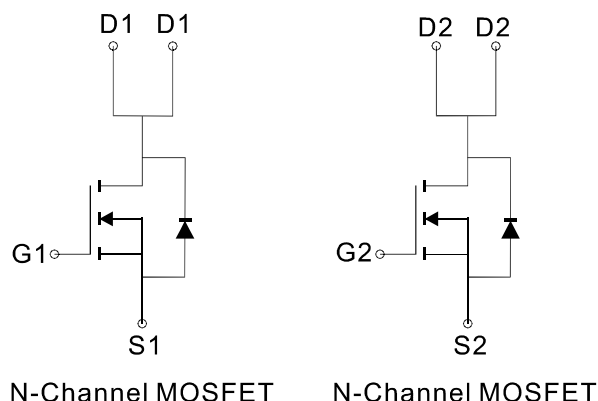
Ordering Information: ME4920 (Pb-free)
ME4920-G (Green product-Halogen free)

FEATURES

- $R_{DS(ON)} \leq 35 \text{ m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} \leq 45 \text{ m}\Omega @ V_{GS}=4.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	6
		$T_A=70^\circ\text{C}$	4.8
Pulsed Drain Current	I_{DM}	24	A
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.3
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =10V, I _D = 6.9A		26	35	mΩ
		V _{GS} =4.5V, I _D = 5.8A		36	45	
V _{SD}	Diode Forward Voltage	I _S =1.7A, V _{GS} =0V		0.75	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =6.9A		11.5		nC
Q _{gs}	Gate-Source Charge			2.7		
Q _{gd}	Gate-Drain Charge			2.3		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		350		pF
C _{oss}	Output Capacitance			65		
C _{rss}	Reverse Transfer Capacitance			16		
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V R _G =6Ω		9		ns
t _r	Turn-On Rise Time			10		
t _{d(off)}	Turn-Off Delay Time			32		
t _f	Turn-Off Fall Time			3.5		

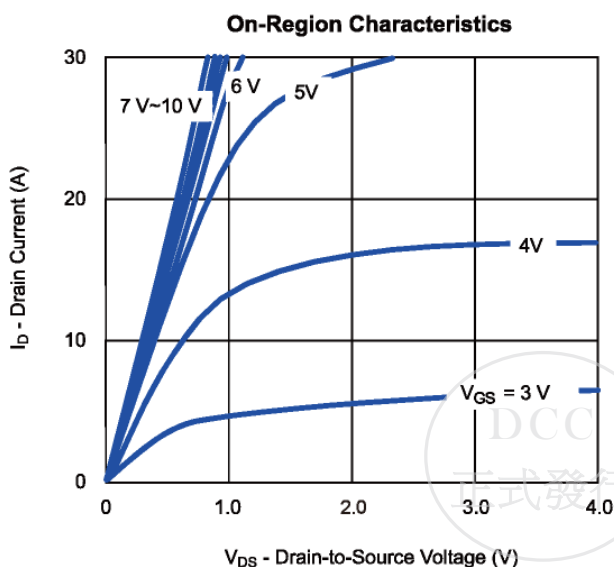
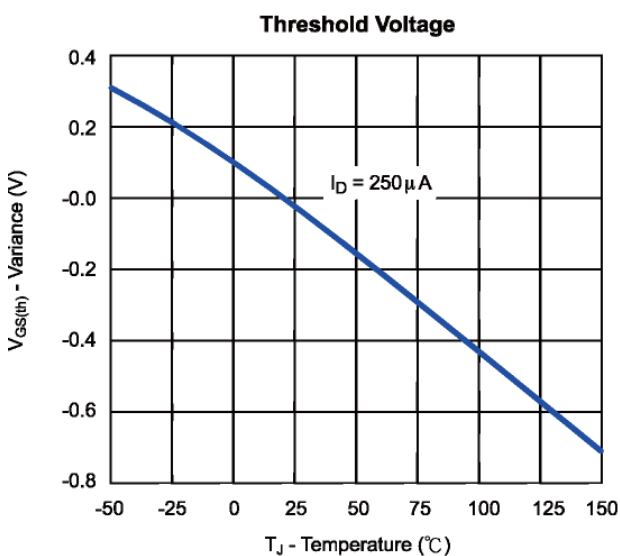
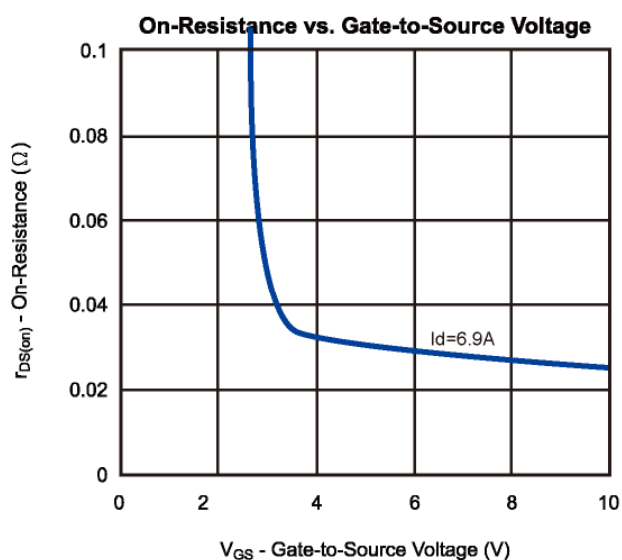
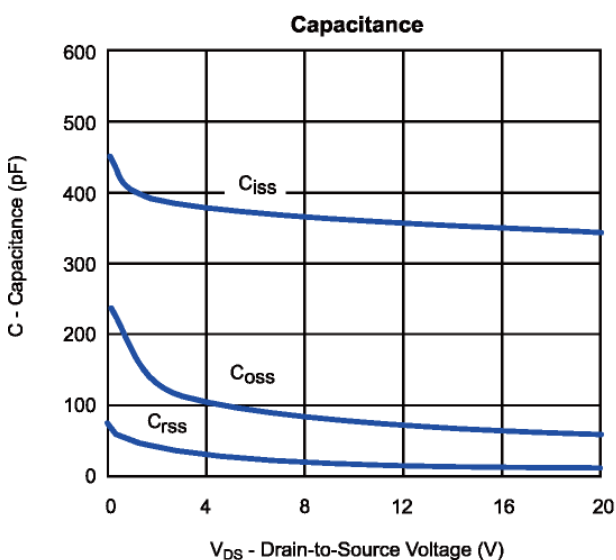
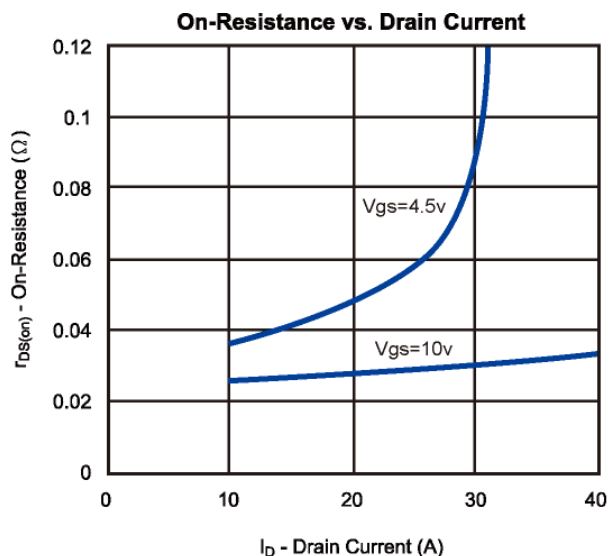
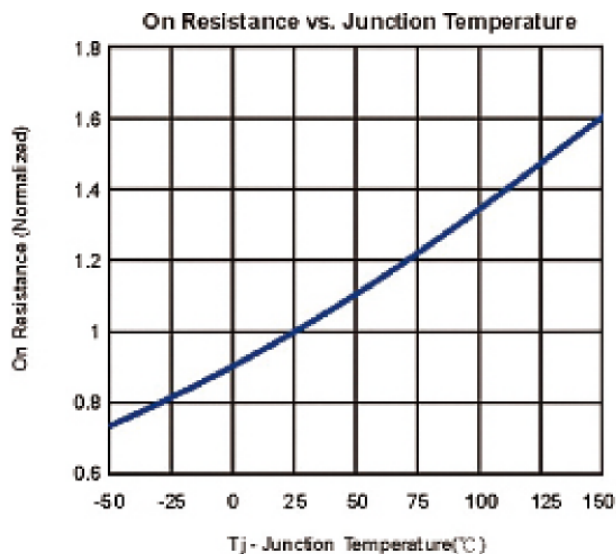
Notes: a. Pulse test:pulse width ≤ 300us, duty cycle ≤ 2%.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



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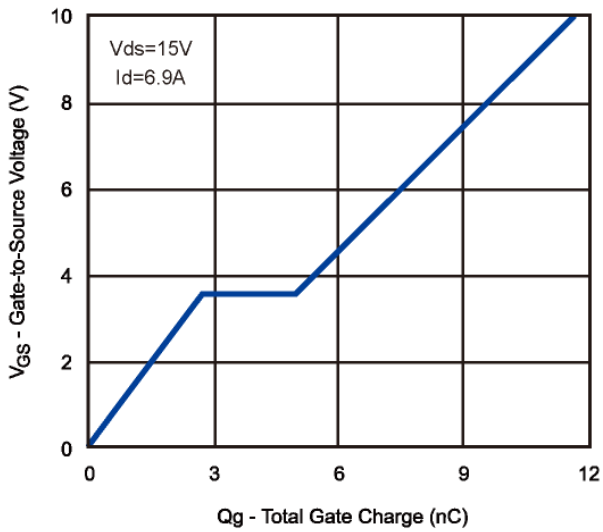
Typical Characteristics (T_J = 25°C Noted)



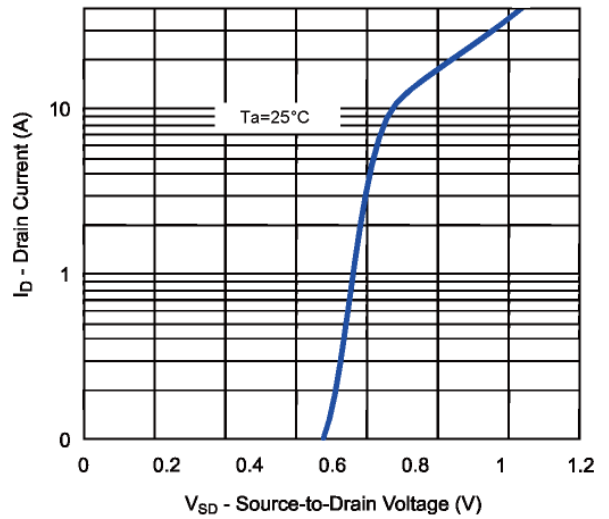
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Typical Characteristics (T_J = 25°C Noted)

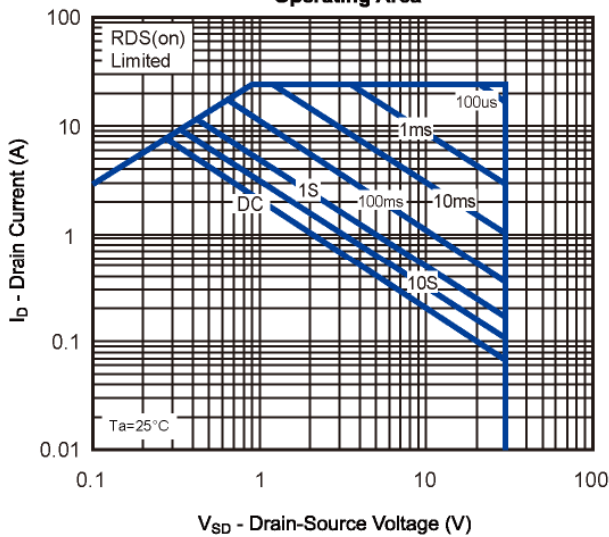
Gate Charge



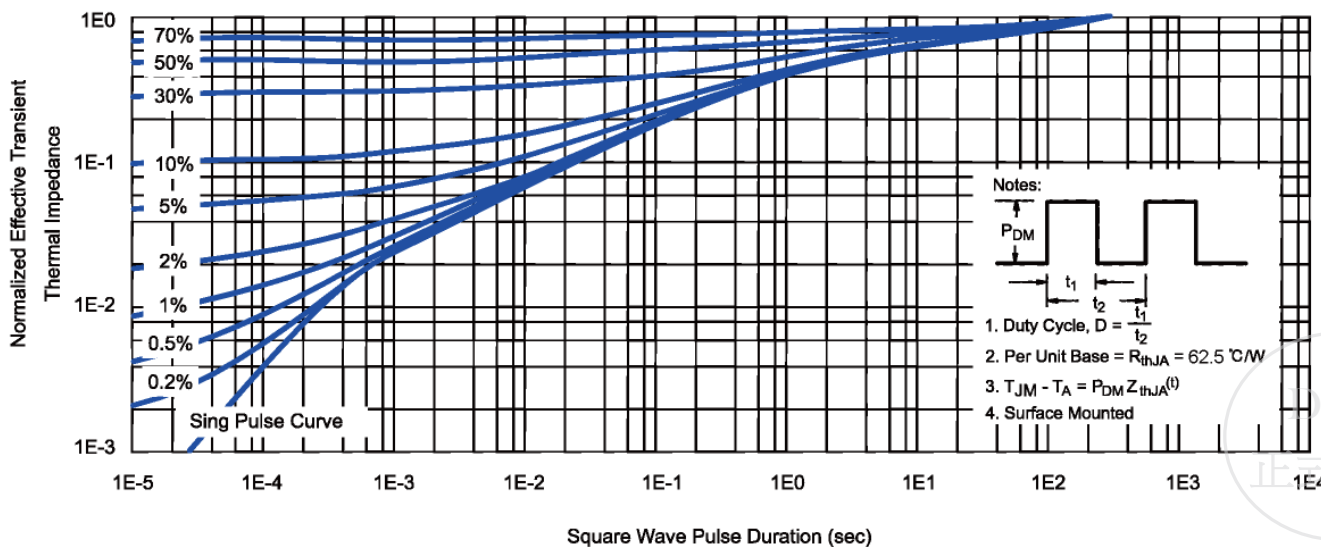
Body-diode characteristics



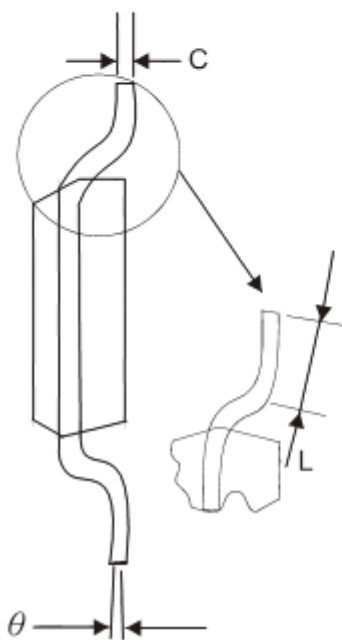
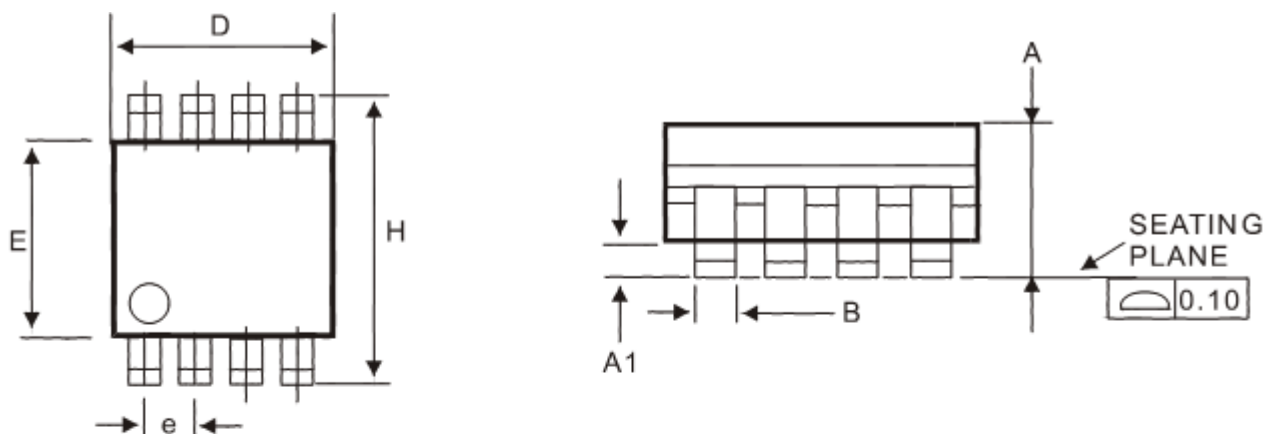
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline



DIM	MILLIMETERS(mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

