ME3424D/ME3424D-G

N-Channel 30V (D-S) MOSFET , ESD Protected

GENERAL DESCRIPTION

The ME3424D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 28m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 42m\Omega @ V_{GS}=4.5V$
- ESD Protected
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

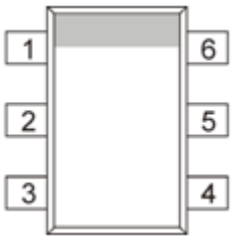
APPLICATIONS

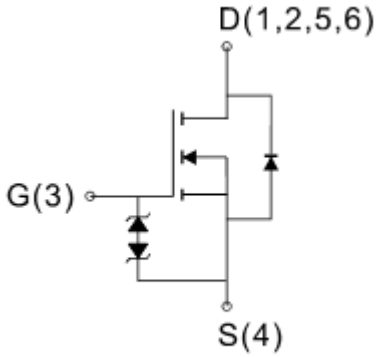
- Power Management in Note book
- Portable Equipment
- Load Switch

PIN CONFIGURATION

(TSOP-6)

Top View





N-Channel

Ordering Information: ME3424D (Pb-free)

ME3424D-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_A=25℃	I_D	5	A
	T_A=70℃		4	
Pulsed Drain Current		I_{DM}	20	A
Maximum Power Dissipation*	T_A=25℃	P_D	1.1	W
	T_A=70℃		0.7	
Operating Junction Temperature		T_J	-55 to 150	℃
Storage Temperature Range		T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	110	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	1.5	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±16V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 6.7A		23	28	mΩ
		V_{GS}=4.5V, I_D= 5.0A		32	42	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHZ		370		pF
Coss	Output Capacitance			68		
Crss	Reverse Transfer Capacitance			21		
Rg	Gate Resistance	f=1MHz		1.9		Ω
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=6.7A		12		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=6.7A		5.7		
Qgs	Gate-Source Charge			3.0		
Qgd	Gate-Drain Charge			2.1		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1.0A, V_{GEN}=10V R_G=6Ω		9.2		ns
t_r	Turn-On Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			33		
t_f	Turn-Off Fall Time			3.7		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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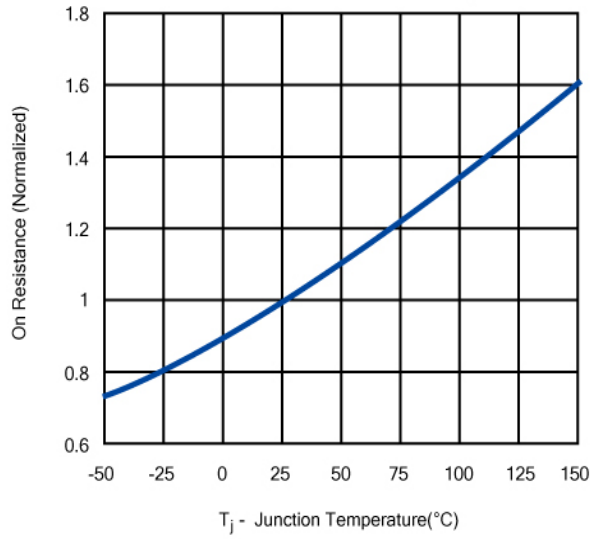
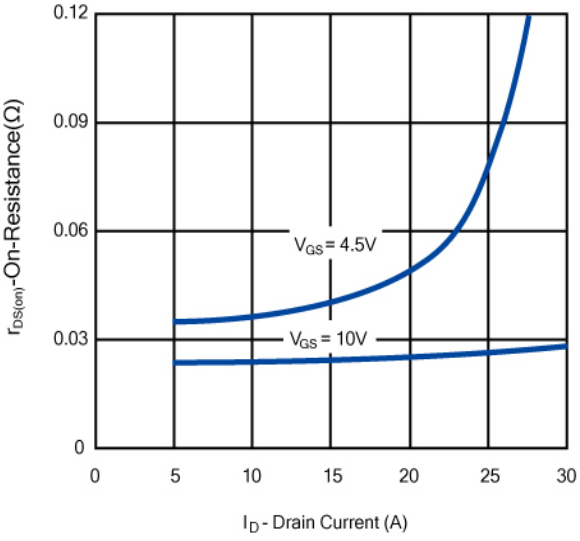
Typical Characteristics (T_J =25℃ Noted)

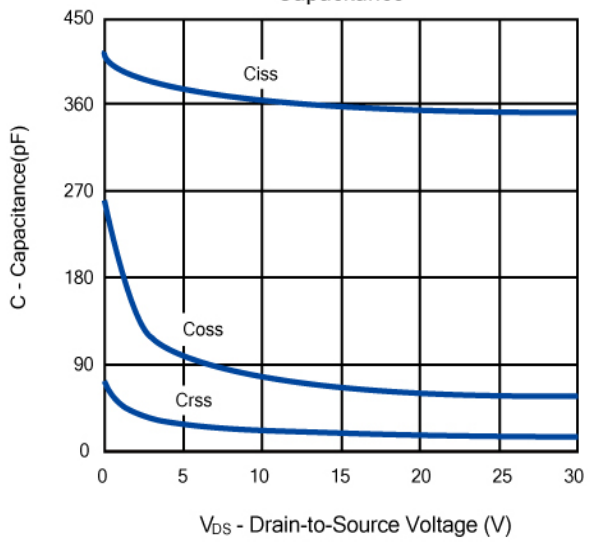
On Resistance vs. Junction Temperature



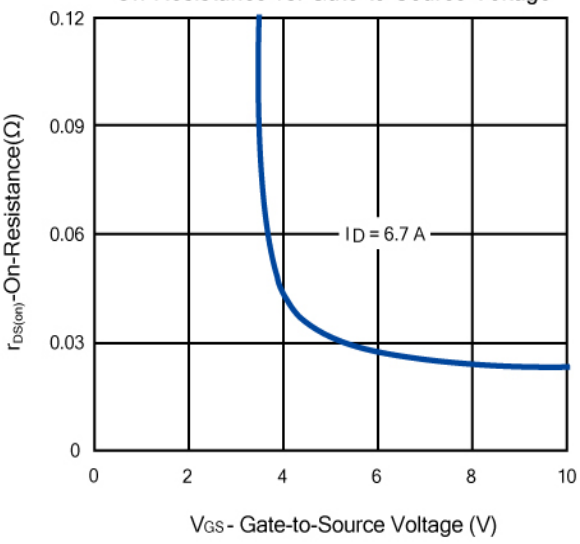
On-Resistance vs. Drain Current



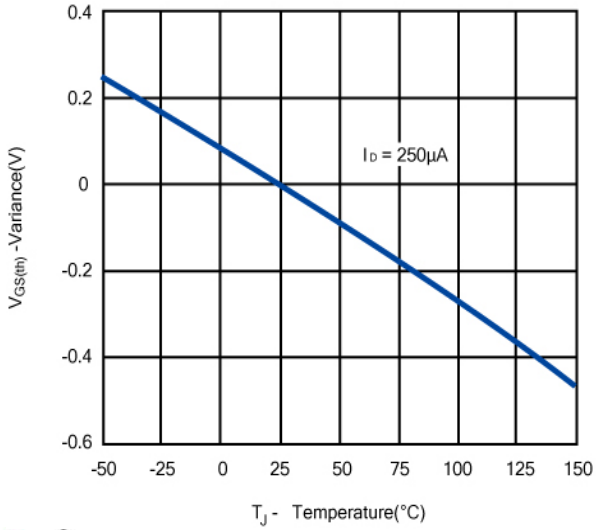
Capacitance



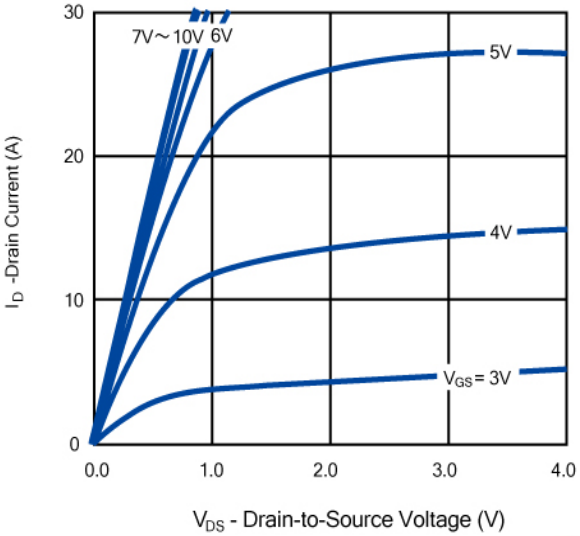
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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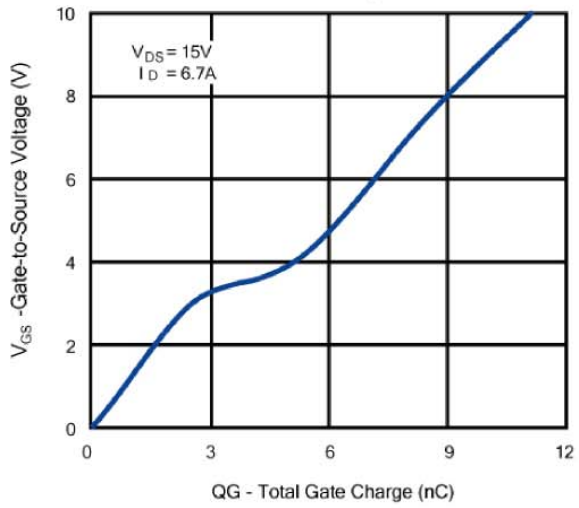
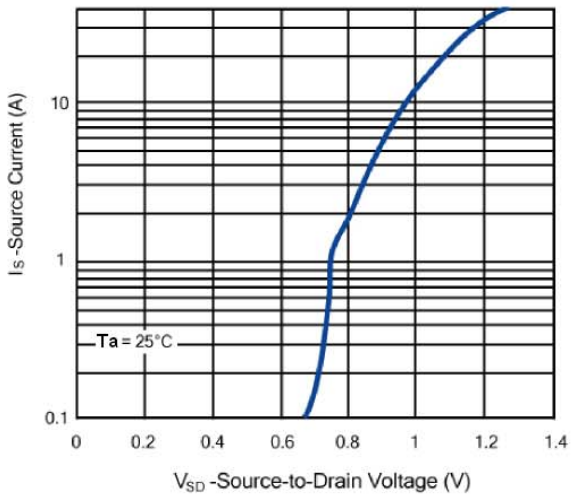
Typical Characteristics (T_J =25℃ Noted)

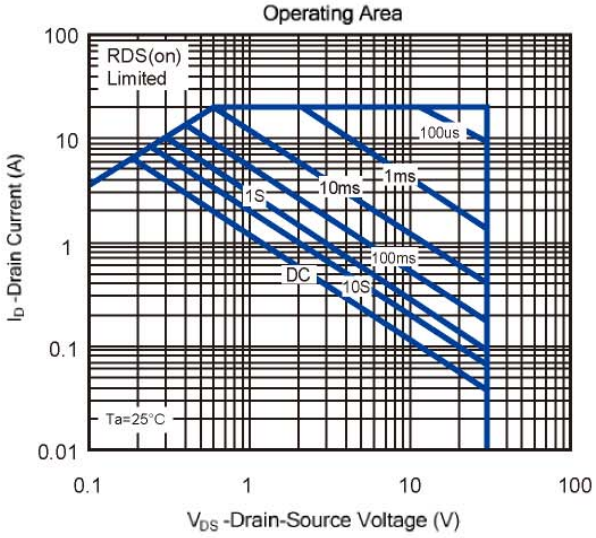
Gate Charge



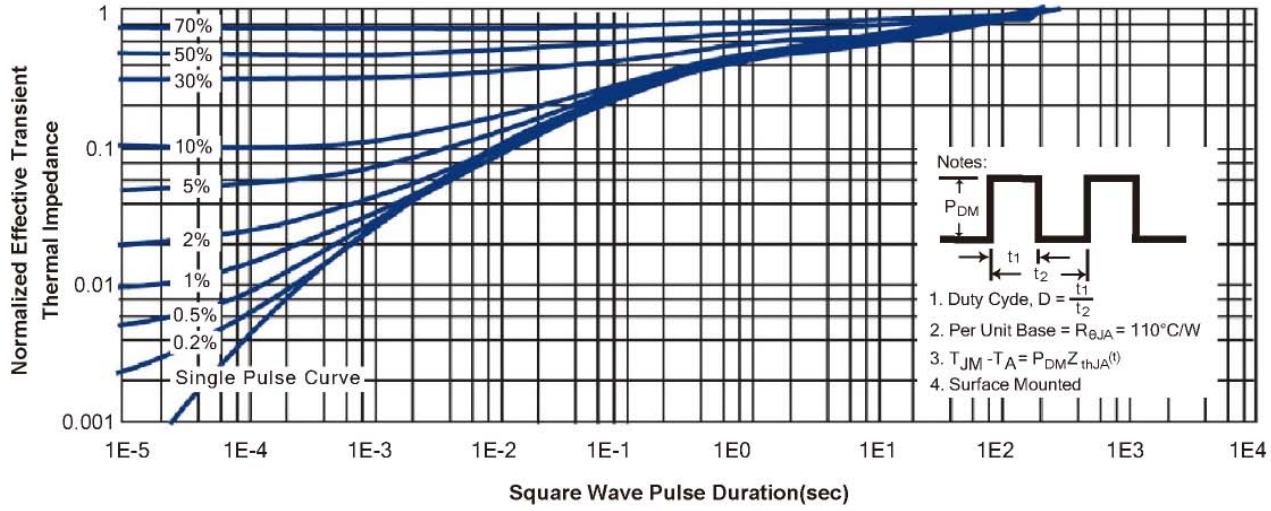
Body-diode characteristics



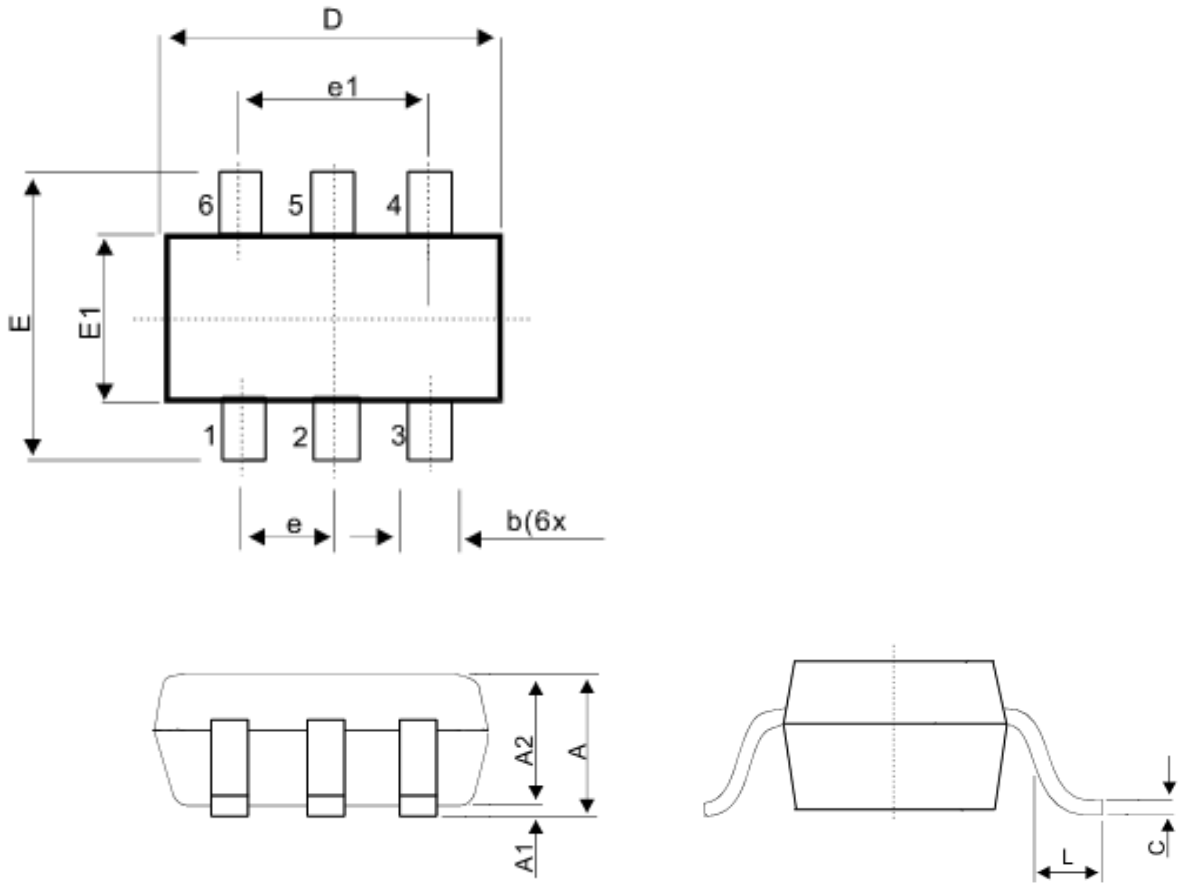
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TSOP-6 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.20
A1	0.01	0.10
A2	0.90	1.15
b	0.25	0.50
C	0.10	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60