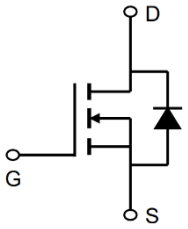
AP100N04NF

40V N-Channel Enhancement Mode MOSFET

Description

The AP100N04NF uses advanced **APM-SGT II** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

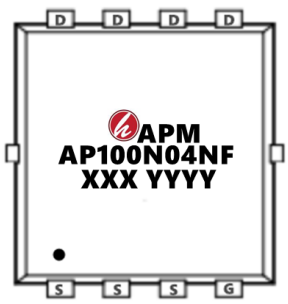


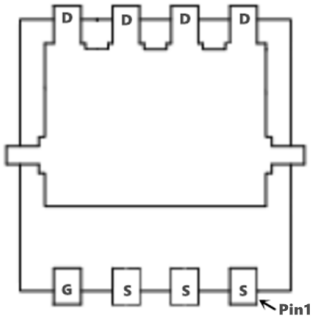
General Features

V_{DS} = 40V I_D =100A

$R_{DS(ON)}$ < 3.2mΩ @ V_{GS}=10V **（Type：2.1mΩ）**

Ciss≈2600PF



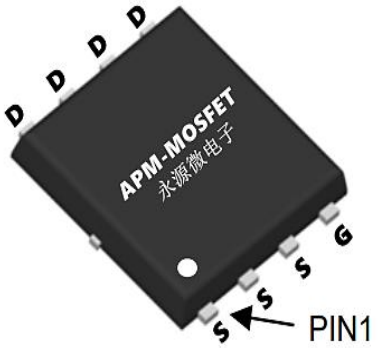


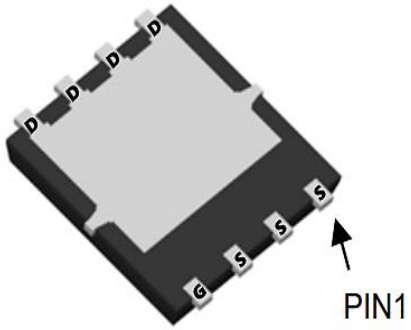
Application

Boost driver

Brushless motor

BLDC





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP100N04NF	DFN5*6-8L	AP100N04NF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	40	V
VGS	Gate-Source Voltage	±20	V
ID@TC=25℃	Continuous Drain Current, VGS @ 10V1	100	A
ID@TC=100℃	Continuous Drain Current, VGS @ 10V1	71	A
IDM	Pulsed Drain Current2	240	A
EAS	Single Pulse Avalanche Energy3	345	mJ
IAS	Avalanche Current	54	A
PD@TC=25℃	Total Power Dissipation4	22	W
TSTG	Storage Temperature Range	-55 to 150	℃
TJ	Operating Junction Temperature Range	-55 to 150	℃
RθJA	Thermal Resistance Junction-Ambient 1	25	℃/W
RθJC	Thermal Resistance Junction-Case1	1.7	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	40	44	---	V
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=20A	---	2.1	3.2	mΩ
		V_{GS}=4.5V , I_D=15A	---	2.7	5.3	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	1.7	2.5	V
IDSS	Drain-Source Leakage Current	V_{DS}=40V , V_{GS}=0V , T_J=25℃	---	---	1	uA
IDSS	Drain-Source Leakage Current	V_{DS}=40V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=20A	---	75	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.5	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=20A	---	22.7	---	nC
Qgs	Gate-Source Charge		---	7.5	---	
Qgd	Gate-Drain Charge		---	5.5	---	
Td(on)	Turn-On Delay Time	V_{DD}=20V , V_{GS}=10V , R_G=3Ω，I_D=20A	---	10	---	ns
T_r	Rise Time		---	5	---	
Td(off)	Turn-Off Delay Time		---	33	---	
T_f	Fall Time		---	6.5	---	
Ciss	Input Capacitance	V_{DS}=20V , V_{GS}=0V , f=1MHz	---	2600	---	pF
Coss	Output Capacitance		---	899	---	
Crss	Reverse Transfer Capacitance		---	71	---	
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	30	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1	V

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD =32V,VGS =10V,L=0.1mH,IAS =54A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

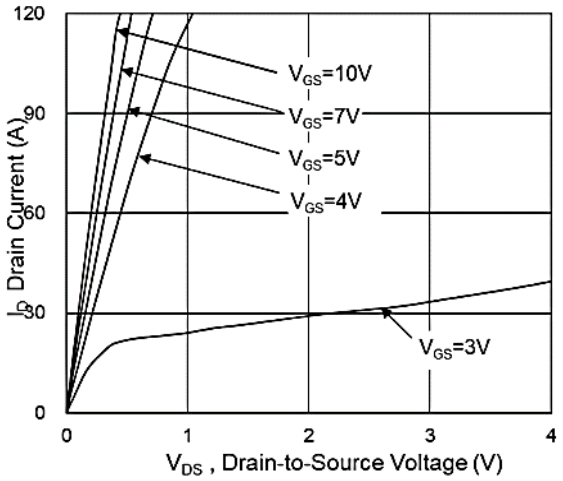


Fig.1 Typical Output Characteristics

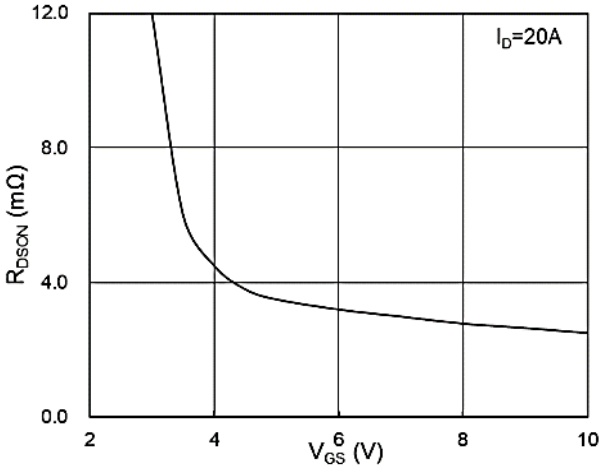


Fig.2 On-Resistance vs G-S Voltage

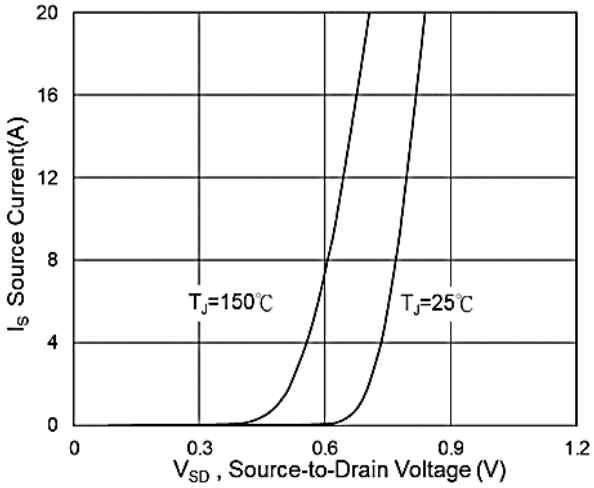


Fig.3 Source Drain Forward Characteristics

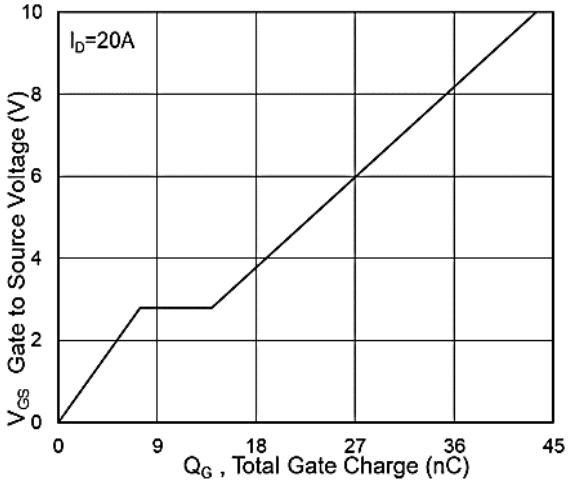


Fig.4 Gate-Charge Characteristics

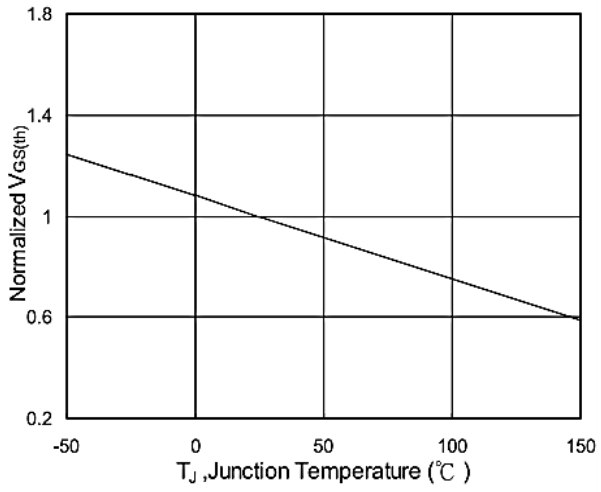


Fig.5 Normalized $V_{GS(th)}$ vs T_J

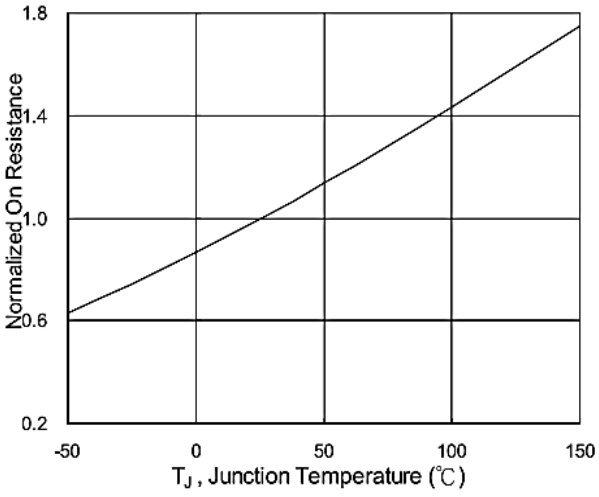


Fig.6 Normalized R_{DSON} vs T_J

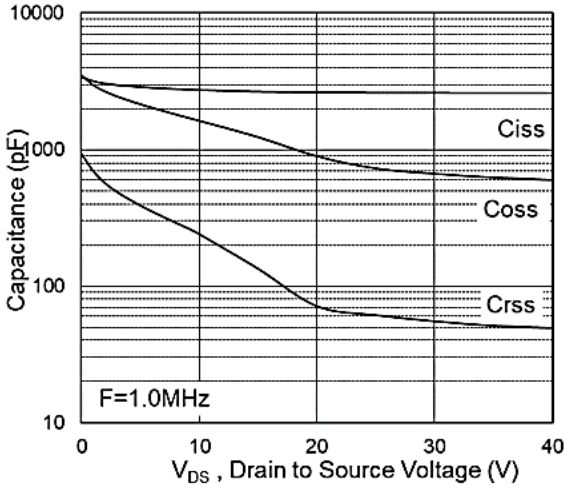


Fig.7 Capacitance

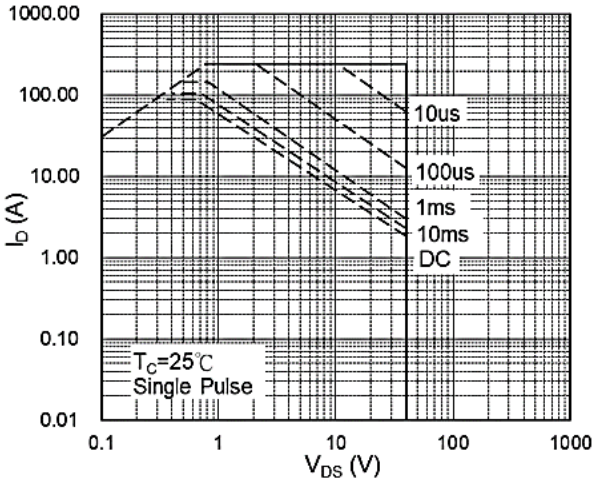


Fig.8 Safe Operating Area

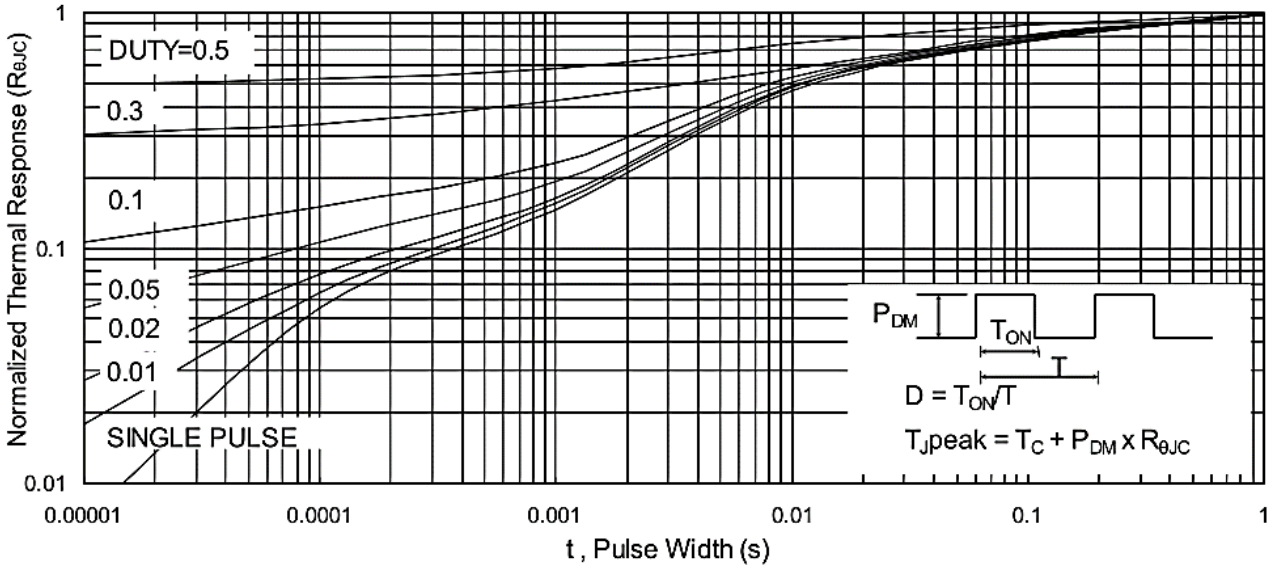


Fig.9 Normalized Maximum Transient Thermal Impedance

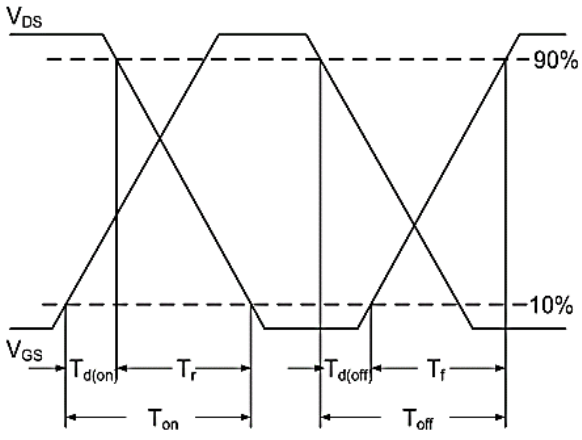


Fig.10 Switching Time Waveform

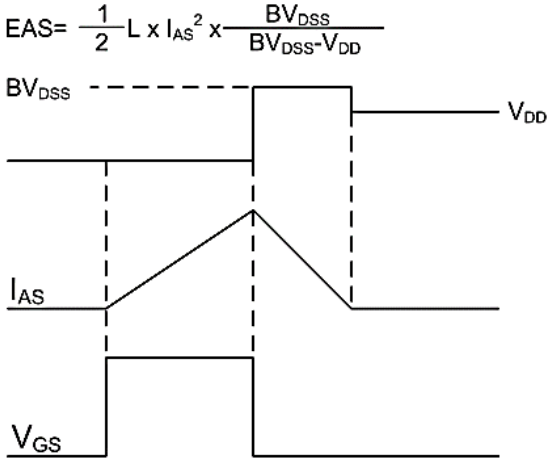
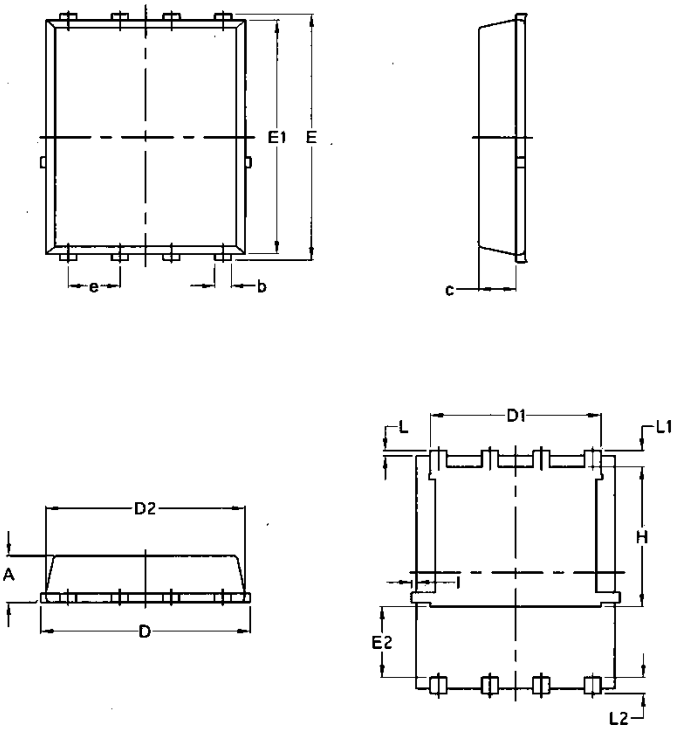


Fig.11 Unclamped Inductive Switching Wave

Package Mechanical Data-PDFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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40V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rev1.0	2021/9/31	Initial release
Rev1.1	2021/4/20	Reduce(RDS)