

-200V P-Channel Enhancement Mode MOSFET

Description

The AP18P20P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

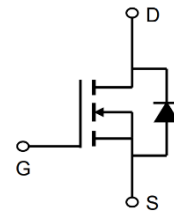
$V_{DS} = -200V$ $I_D = -18A$

$R_{DS(ON)} < 320m\Omega$ @ $V_{GS}=10V$ (Type: 260m Ω)

Application

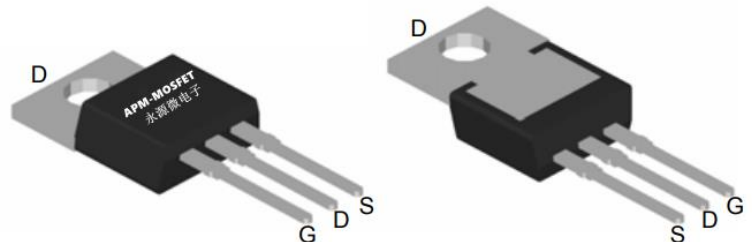
Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Top View

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP18P20P	TO-220-3L	AP18P20P XXXX YYYY	1000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-200	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D $T_C = 25^{\circ}C$	Continuous Drain Current	-18	A
I_D $T_C = 100^{\circ}C$	Continuous Drain Current	-12	A
I_{DM}	Pulsed Drain Current ^a	-65	A
E_{AS}	Single Pulse Avalanche Energy ^b	1200	mJ
I_{AR}	Repetitive Avalanche Current ^a	-15	A
P_D $T_C = 25^{\circ}C$	Maximum Power Dissipation	325	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	$^{\circ}C$
R_{thJA}	Maximum Junction-to-Ambient	62	$^{\circ}C/W$
R_{thJC}	Maximum Junction-to-Case (Drain)	1.0	$^{\circ}C/W$

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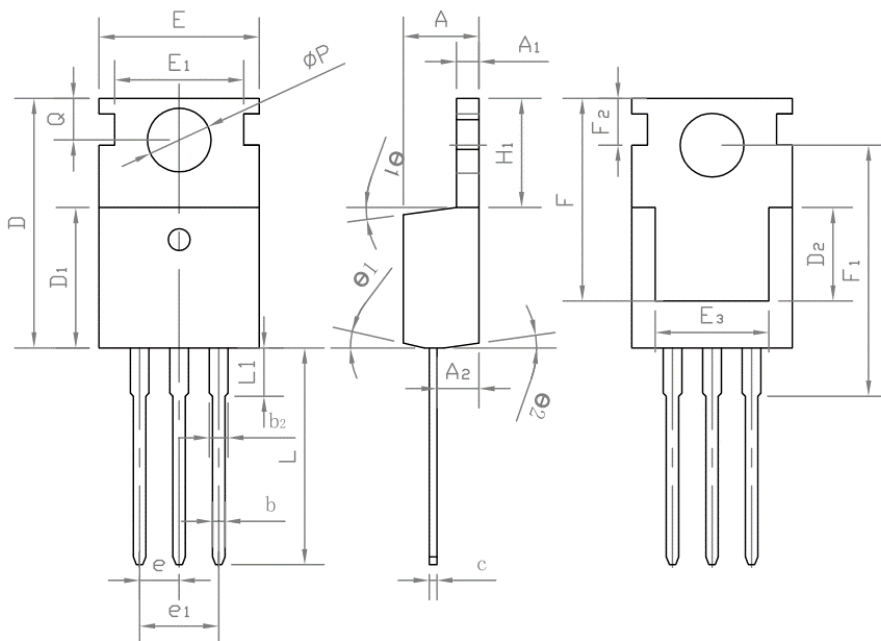
Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{DS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-200	-254	-	V
V _{GS(th)}	Gate-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-2.0	3.5	-5.0	V
I _{GSS}	Gate-Source Leakage	V _{GS} = ± 20 V	-	-	± 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -200 V, V _{GS} = 0 V	-	-	100	μA
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} = -10 V, I _D = -5.5 A	-	260	320	mΩ
g _{fs}	Forward Transconductance	V _{DS} = -50 V, I _D = -6.6 A	4.1	-	-	S
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = -25 V, f = 1.0 MHz,	-	2400	-	pF
C _{oss}	Output Capacitance		-	7400	-	pF
C _{rss}	Reverse Transfer Capacitance		-	182	-	pF
Q _g	Total Gate Charge	V _{GS} = -10 V, I _D = -18A, V _{DS} = -160 V	-	-	88	nC
Q _{gs}	Gate-Source Charge		-	-	14.1	nC
Q _{gd}	Gate-Drain Charge		-	-	54	nC
t _{d(on)}	Turn-On Delay Time	V _{DD} = -100 V, I _D = -18A R _g = 9.1Ω,	-	28	-	ns
t _r	Rise Time		-	86	-	ns
t _{d(off)}	Turn-Off Delay Time		-	78	-	ns
t _f	Fall Time		-	76	-	ns
R _g	Gate Input Resistance	f = 1MHz, open drain	0.3	-	1.7	Ω
V _{SD}	Body Diode Voltage	T _J = 25 °C, I _S = -18A, V _{GS} = 0 V	-	-	-5	V
t _{rr}	Body Diode Reverse Recovery Time	T _J = 25 °C, I _F = -18A, di/dt = 100 A/	-	500	600	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	5.8	7.2	μC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The EAS data shows Max. rating . I_{AS}=-18A, V_{DD}=50V, R_G=25Ω, Starting T_J=25 °C
- 3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Package Mechanical Data-TO-220-3L-SLK



Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.27	4.57	4.87
A1	1.15	1.30	1.45
A2	2.10	2.40	2.70
b	0.70	0.80	1.00
b2	1.17	1.27	1.50
D	0.40	0.50	0.65
D1	8.80	9.10	9.40
D2	5.70	6.70	7.00
E	9.70	10.00	10.30
E1	-	8.70	-
E2	9.63	10.00	10.35
E3	7.00	8.00	8.40
e	0.37		
e1	0.10		
H1	6.00	6.50	6.85
L	12.75	13.50	13.90
L1	-	3.10	3.40
Φp	3.45	3.60	3.75
Q	2.60	2.80	3.00
θ1	4°	7°	10°
θ2	0°	3°	6°
F	13.30	13.50	13.70
F1	15.50	15.90	16.30
F2	2.80	3.00	3.20

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Edition	Date	Change
Rve1.0	2021/1/31	Initial release

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