

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP4606C uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 6.5A$

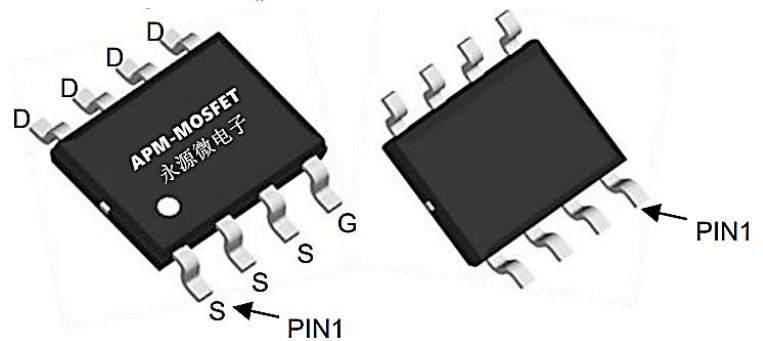
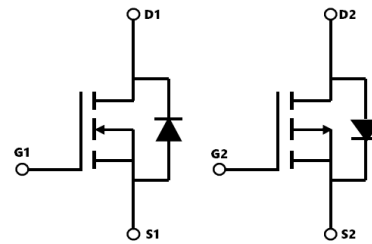
$R_{DS(ON)} < 35m\Omega$ @ $V_{GS}=10V$ (Type: 28m Ω)

$V_{DS} = -20V$ $I_D = -5.8A$

$R_{DS(ON)} < 80m\Omega$ @ $V_{GS}=-10V$ (Type: 55m Ω)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4606C	SOP-8L	AP4606C XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.5	-5.8	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.8	-3.5	A
I_{DM}	Pulsed Drain Current ²	52	-40	A
EAS	Single Pulse Avalanche Energy ³	12	18	mJ
$P_D @ T_A=25^\circ C$	Total Power Dissipation ⁴	1.5	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	105		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	50		$^\circ C/W$

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N-Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	22	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=3A$	---	28	35	m Ω
		$V_{GS}=2.5V, I_D=2A$	---	32	40	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.5	0.75	1.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=16V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=3A$	---	10.5	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=3A$	---	4.6	---	nC
Q_{gs}	Gate-Source Charge		---	0.7	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega, I_D=3A$	---	1.6	---	ns
T_r	Rise Time		---	42	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	7	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	310	---	pF
C_{oss}	Output Capacitance		---	49	---	
C_{rss}	Reverse Transfer Capacitance		---	35	---	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V, \text{Force Current}$	---	---	3.6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、 The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-22	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5V, I_D=-3A$	---	55	80	m Ω
		$V_{GS}=-2.5V, I_D=-2A$	---	75	100	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.45	-0.6	-1.0	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-20V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	uA
		$V_{DS}=-20V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	---	12.2	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-3A$	---	10.1	---	nC
Q_{gs}	Gate-Source Charge		---	1.21	---	
Q_{gd}	Gate-Drain Charge		---	2.46	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-10V, V_{GS}=-4.5V, R_G=3.3\Omega, I_D=-3A$	---	5.6	---	ns
T_r	Rise Time		---	32.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	45.6	---	
T_f	Fall Time		---	29.2	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	677	---	pF
C_{oss}	Output Capacitance		---	82	---	
C_{riss}	Reverse Transfer Capacitance		---	73	---	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V, \text{Force Current}$	---	---	-3	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、 The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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N-Channel Typical Characteristics

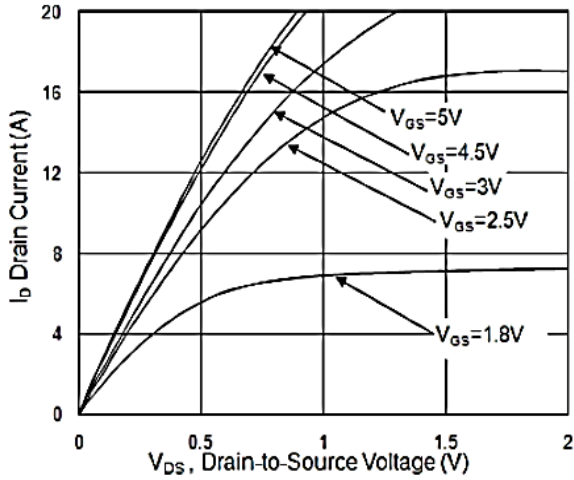


Fig.1 Typical Output Characteristics

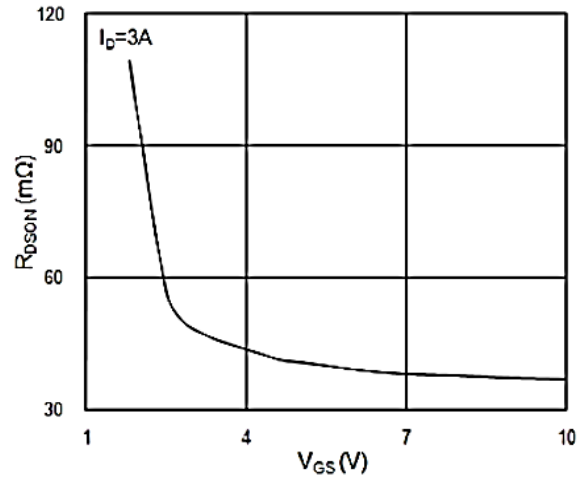


Fig.2 On-Resistance vs. G-S Voltage

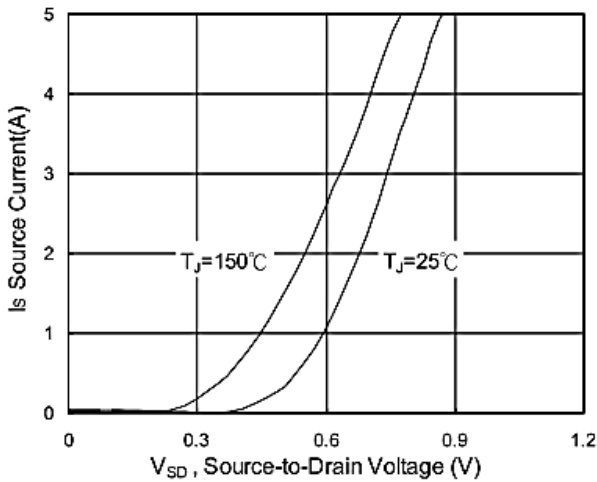


Fig.3 Source Drain Forward Characteristics

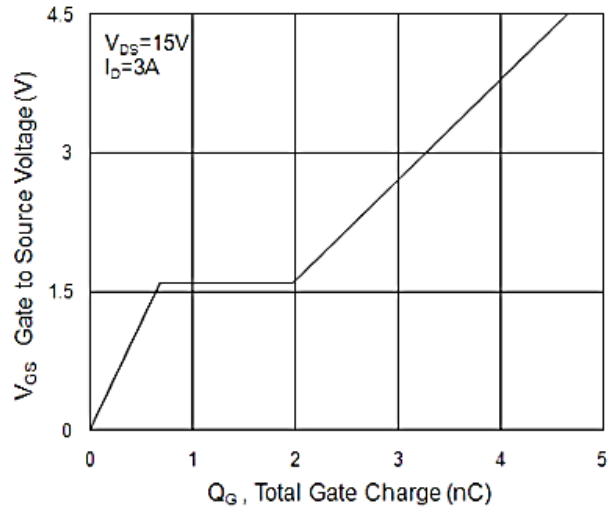


Fig.4 Gate-Charge Characteristics

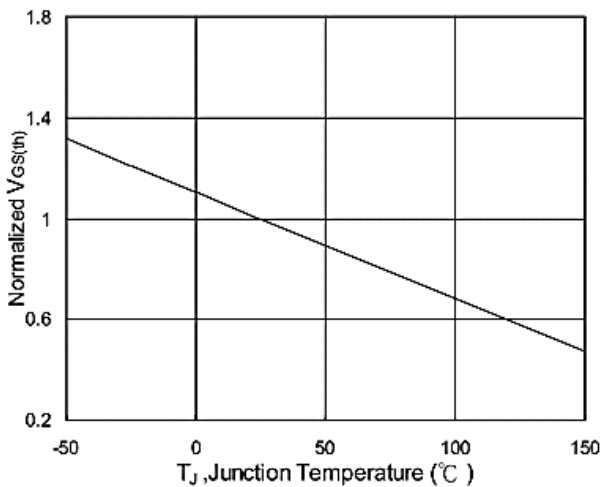


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

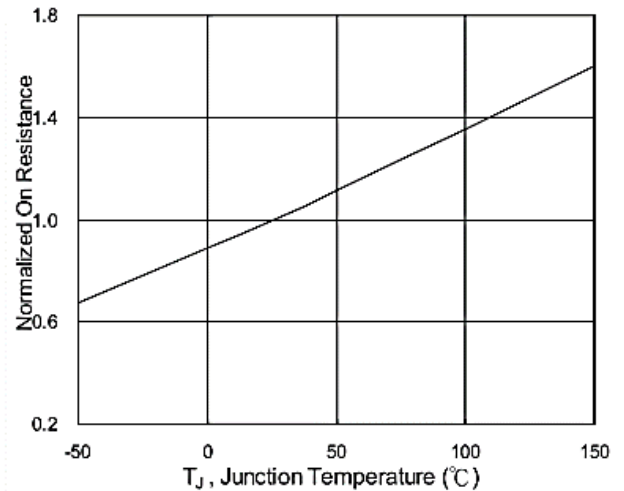


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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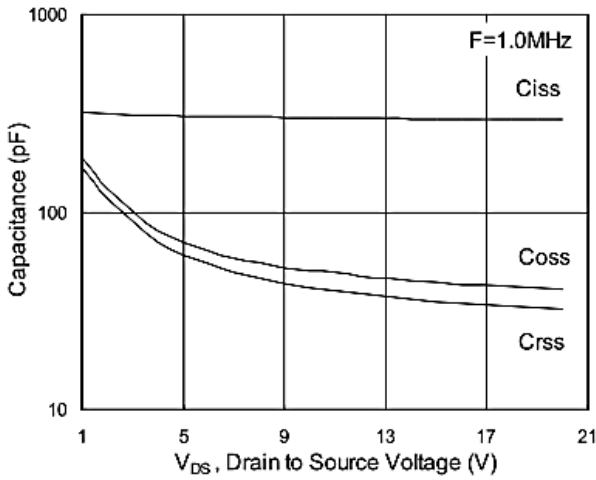


Fig.7 Capacitance

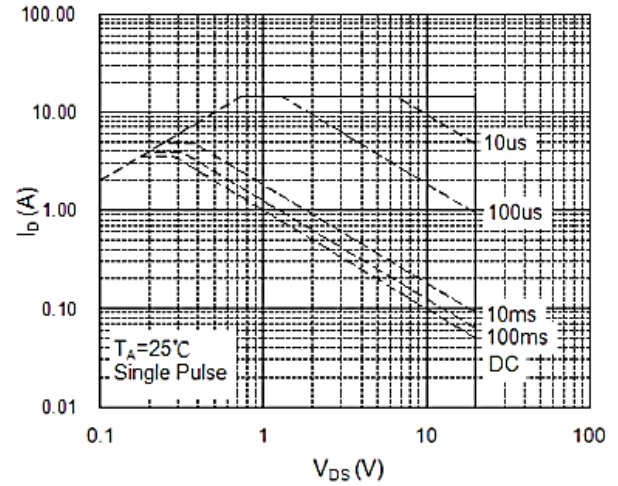


Fig.8 Safe Operating Area

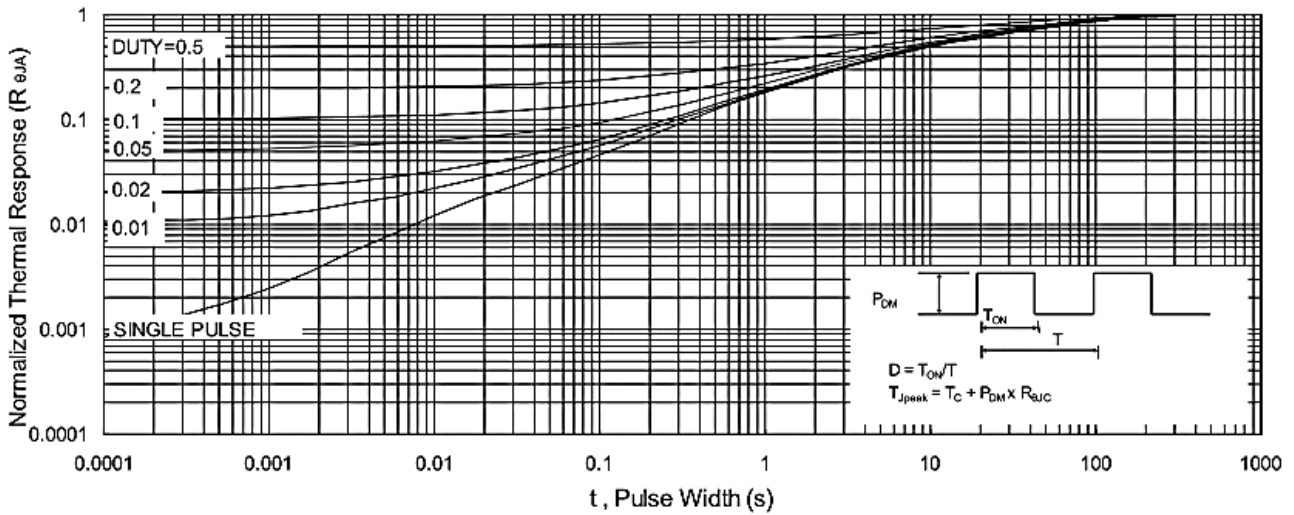


Fig.9 Normalized Maximum Transient Thermal Impedance

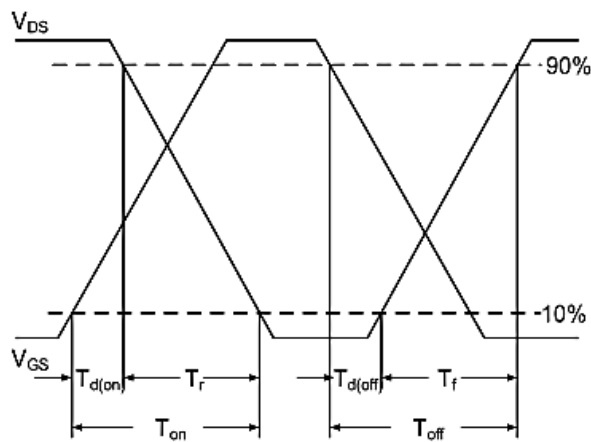


Fig.10 Switching Time Waveform

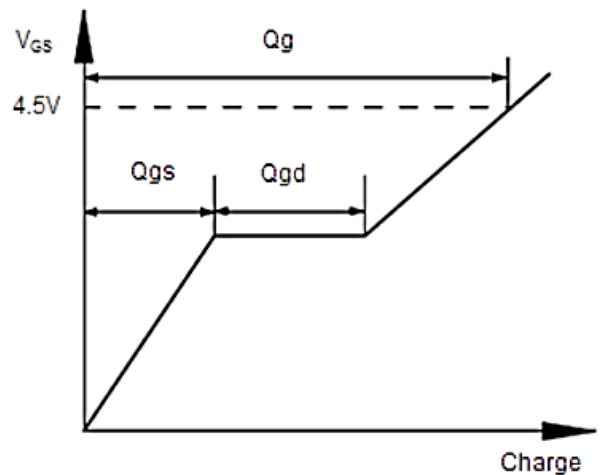


Fig.11 Gate Charge Waveform

P-Channel Typical Characteristics

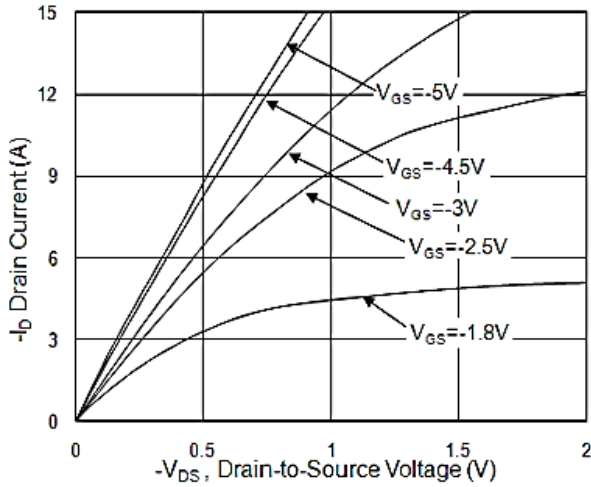


Fig.1 Typical Output Characteristics

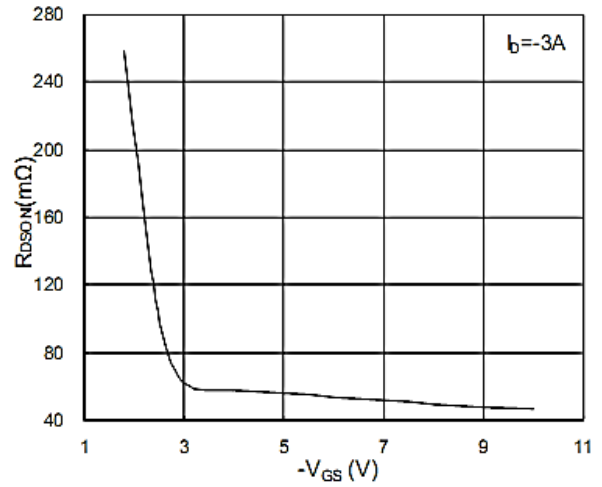


Fig.2 On-Resistance vs. Gate-Source

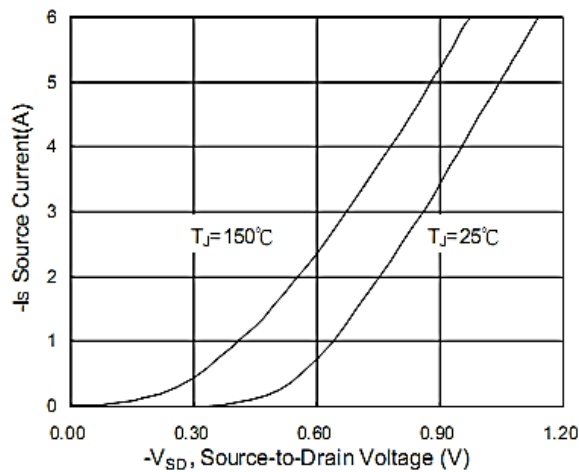


Fig.3 Forward Characteristics Of Reverse

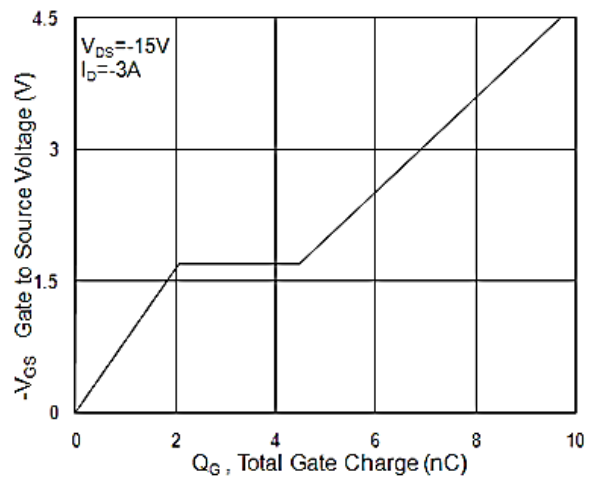


Fig.4 Gate-Charge Characteristics

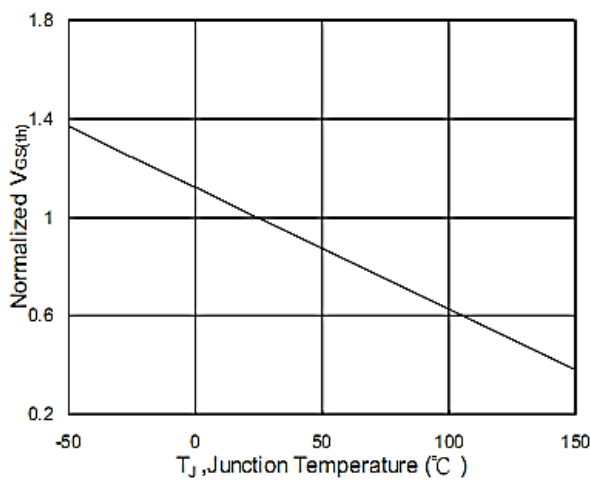


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

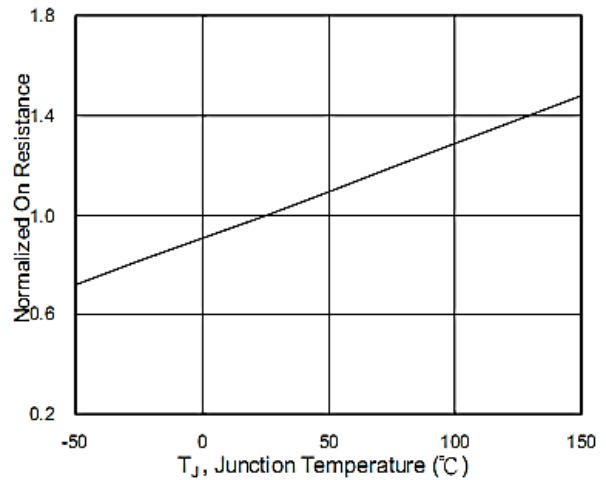


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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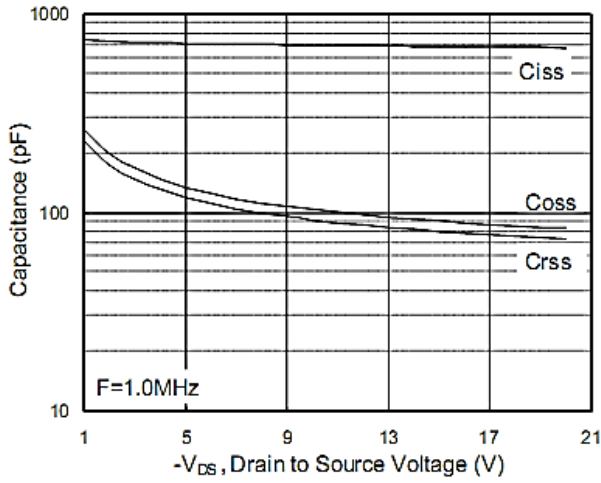


Fig.7 Capacitance

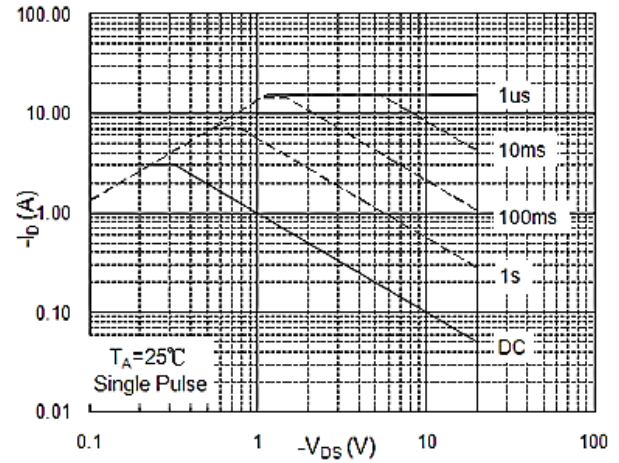


Fig.8 Safe Operating Area

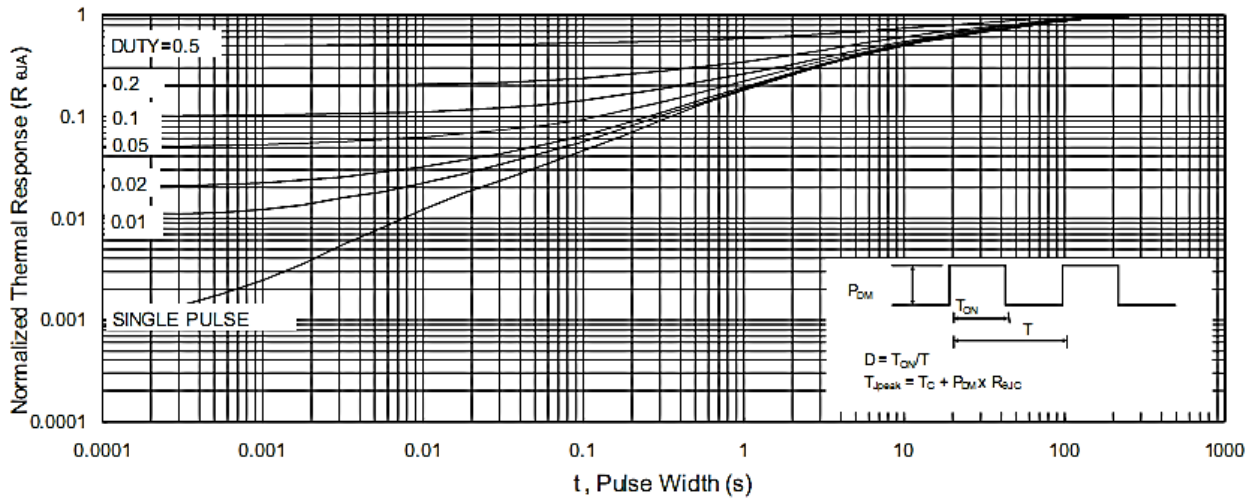


Fig.9 Normalized Maximum Transient Thermal Impedance

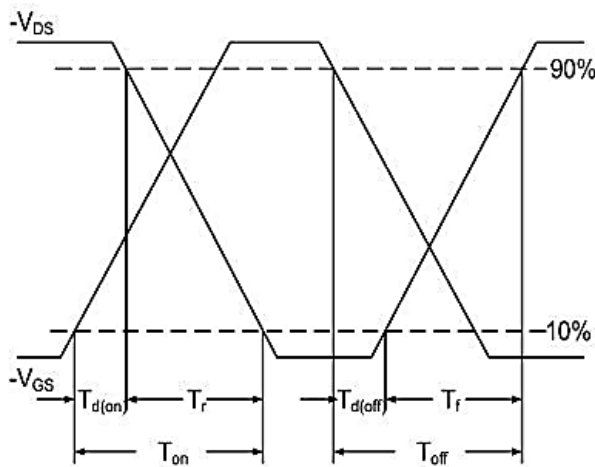


Fig.10 Switching Time Waveform

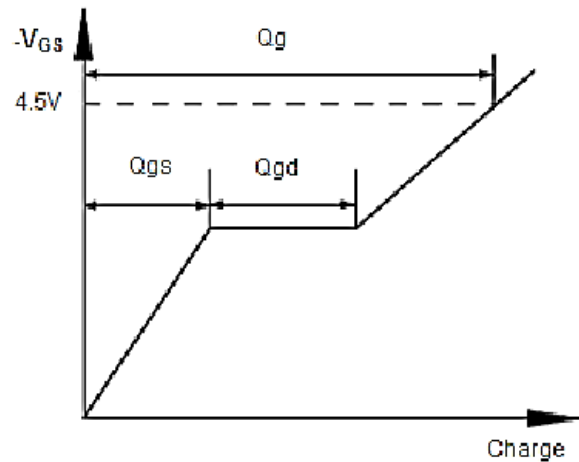
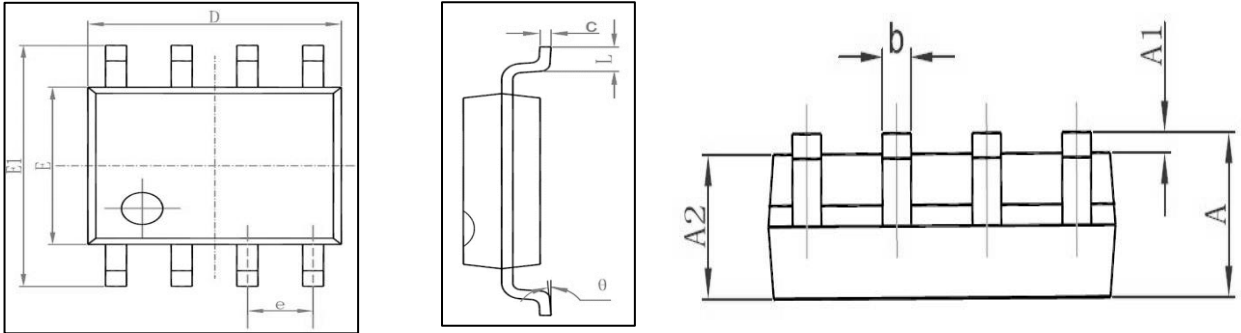


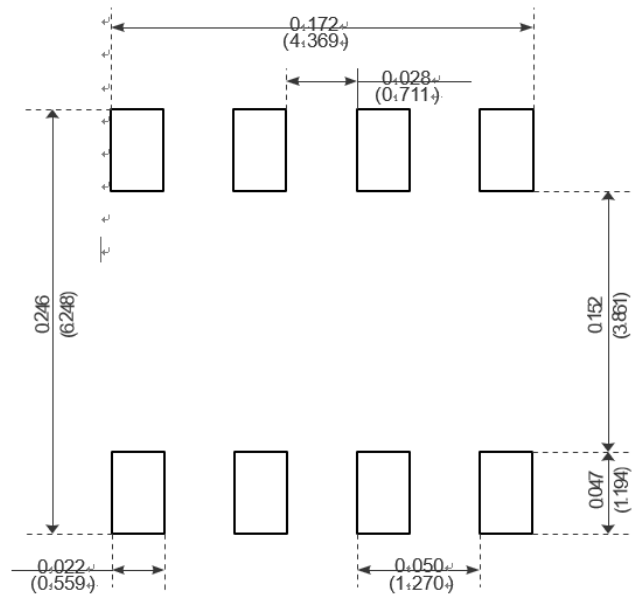
Fig.11 Gate Charge Waveform



Package Mechanical Data-SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2021/12/21	Initial release

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