

650V N-Channel Enhancement Mode MOSFET

Description

The AP4N65F/P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

$V_{DS} = 650V, I_D = 4A$

$R_{DS(ON)} < 2.4\Omega @ V_{GS} = 10V$

Application

Uninterruptible Power Supply(UPS)

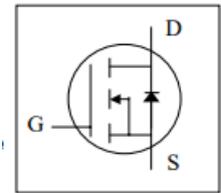
Power Factor Correction (PFC)

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4N65F	TO-220F-3L	AP4N65F XXX YYYY	1000
AP4N65P	TO-220-3L	AP4N65P XXX YYYY	1000

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	Value		Unit
		TO-220F	TO-220	
Drain-Source Voltage ($V_{GS} = 0V$)	V_{DSS}	650		V
Continuous Drain Current	I_D	4		A
Pulsed Drain Current (note1)	I_{DM}	16		A
Gate-Source Voltage	V_{GSS}	± 30		V
Single Pulse Avalanche Energy (note2)	E_{AS}	160		mJ
Avalanche Current (note1)	I_{AR}	4		A
Repetitive Avalanche Energy (note1)	E_{AR}	20		mJ
Power Dissipation ($T_C = 25^\circ C$)	P_D	36		W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+150		$^\circ C$
Thermal Resistance, Junction-to-Case	R_{thJC}	3.47		KW
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62.5		



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Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	650	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650V, V _{GS} = 0V, T _J = 25°C	--	--	1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±30V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	3.0	--	4.0	V
Drain-Source On-Resistance (Note3)	R _{DS(on)}	V _{GS} = 10V, I _D = 2.0A	--	2	2.4	Ω
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	--	580	--	pF
Output Capacitance	C _{oss}		--	69.5	--	
Reverse Transfer Capacitance	C _{rss}		--	10.9	--	
Total Gate Charge	Q _g	V _{DD} = 520V, I _D = 4.0A, V _{GS} = 10V	--	15	--	nC
Gate-Source Charge	Q _{gs}		--	2.5	--	
Gate-Drain Charge	Q _{gd}		--	7.5	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 400V, I _D = 4.0A, R _G = 25 Ω	--	12	--	ns
Turn-on Rise Time	t _r		--	22	--	
Turn-off Delay Time	t _{d(off)}		--	50	--	
Turn-off Fall Time	t _f		--	48	--	
Continuous Body Diode Current	I _S	T _C = 25 °C	--	--	4	A
Pulsed Diode Forward Current	I _{SM}		--	--	16	
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = 4.0A, V _{GS} = 0V	--	--	1.4	V
Reverse Recovery Time	t _{rr}	V _{GS} = 0V, I _S = 4.0A, di _F /dt = 100A/μs	--	250	--	ns
Reverse Recovery Charge	Q _{rr}		--	3.5	--	μC

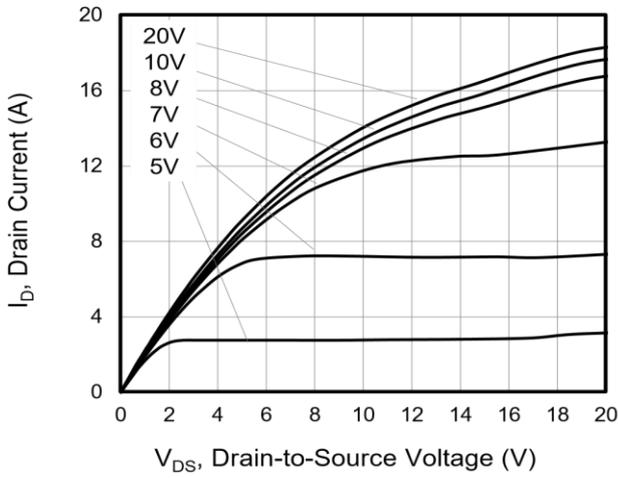
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 4A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 °C
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

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Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)



1.2

Figure 2. Body Diode Forward Voltage

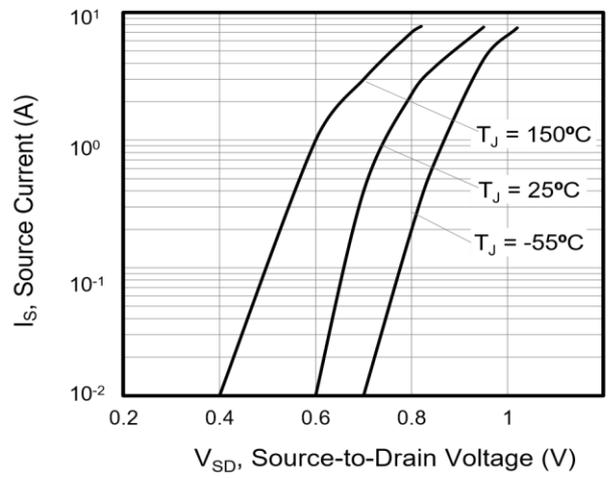


Figure 3. Drain Current vs. Temperature

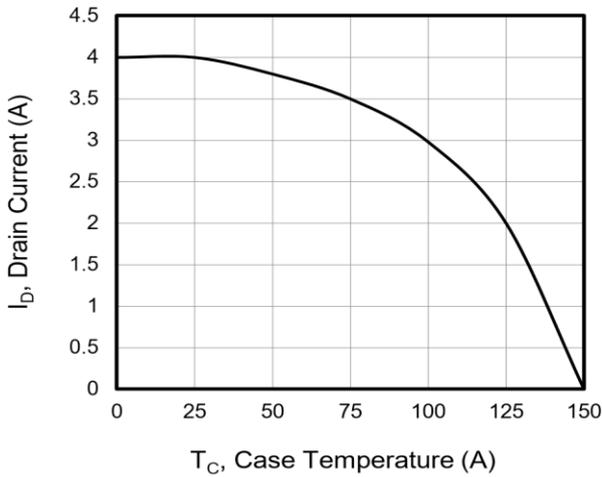


Figure 4. Power Dissipation vs. Temperature

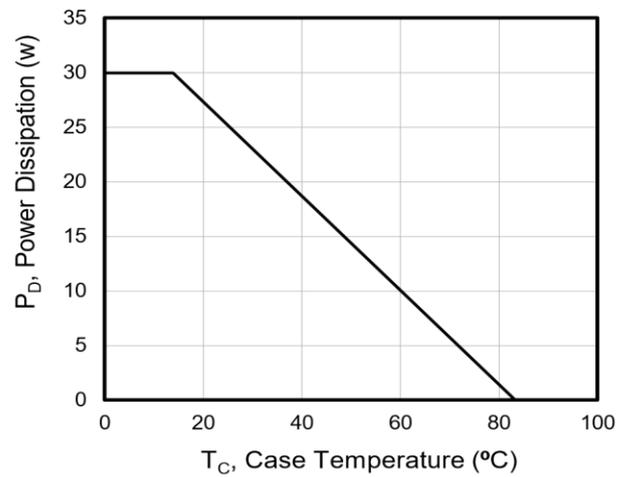


Figure 5. Transfer Characteristics

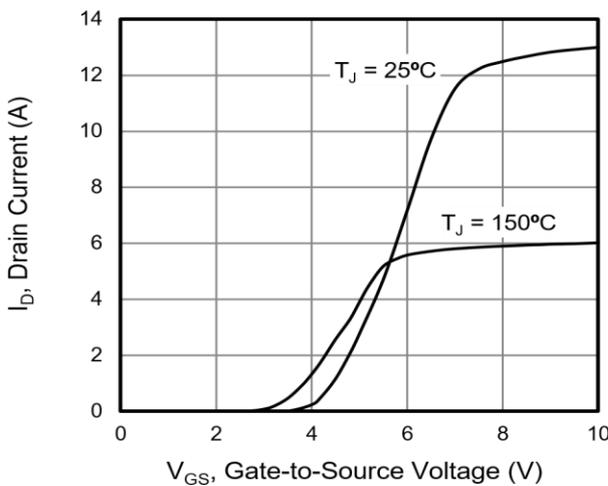
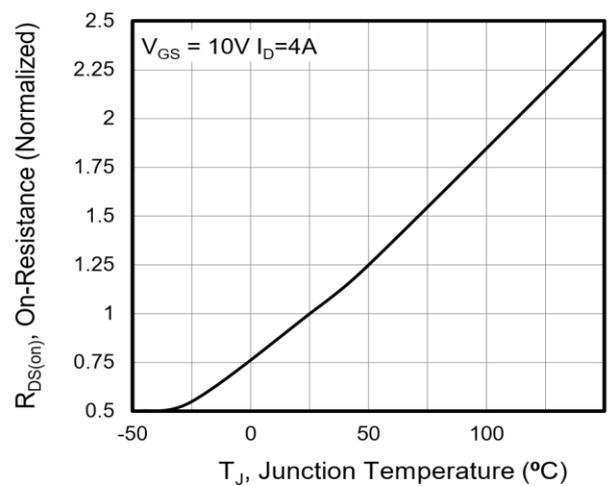


Figure 6. On-Resistance vs. Temperature



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Figure 7. Capacitance

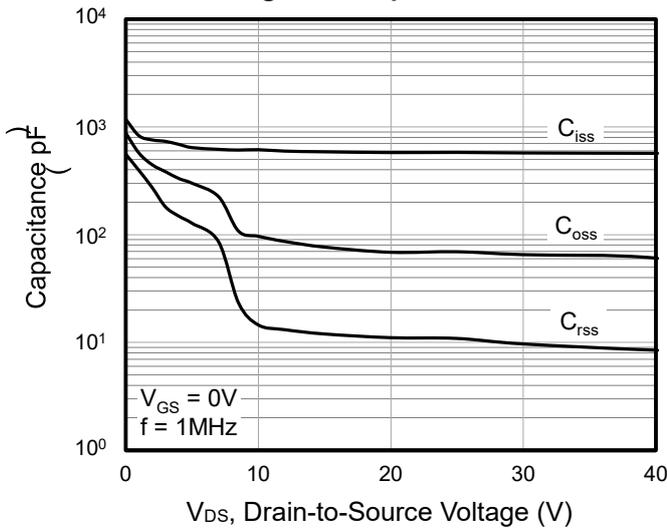


Figure 8. Gate Charge

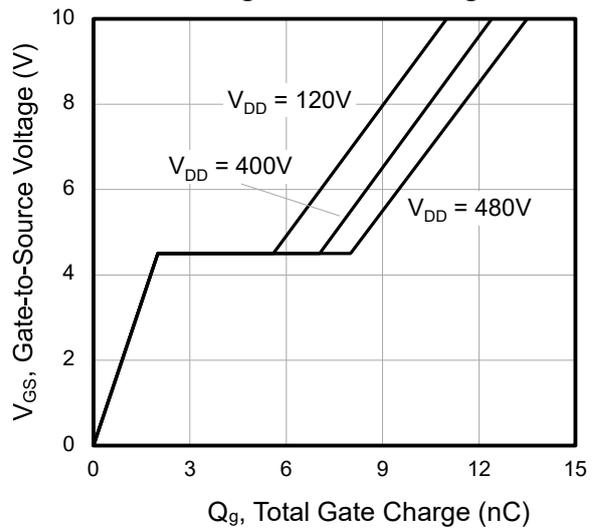


Figure 9. Transient Thermal Impedance TO-220F

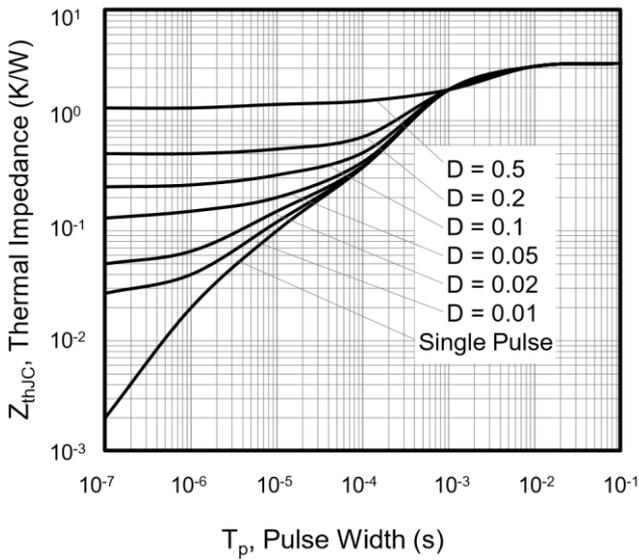
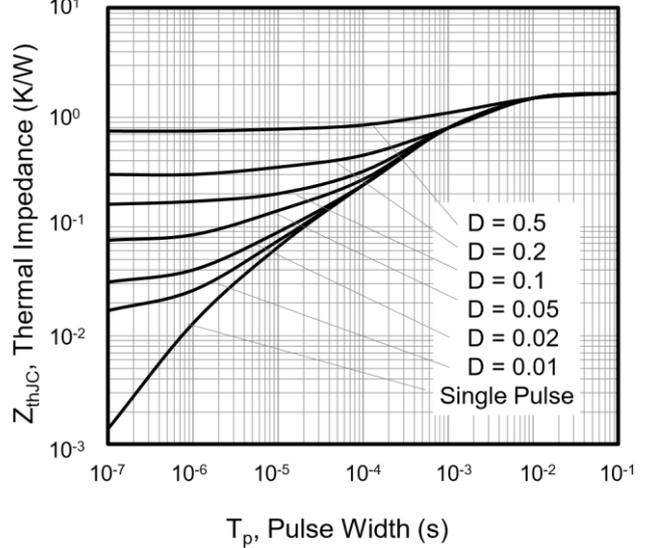


Figure 10. Transient Thermal Impedance TO-220



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Figure A: Gate Charge Test Circuit and Waveform

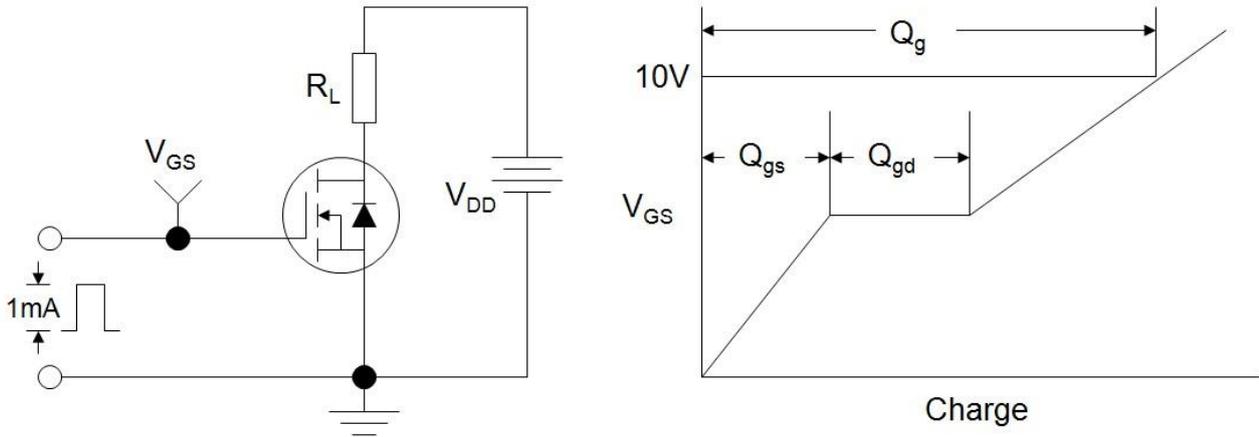


Figure B: Resistive Switching Test Circuit and Waveform

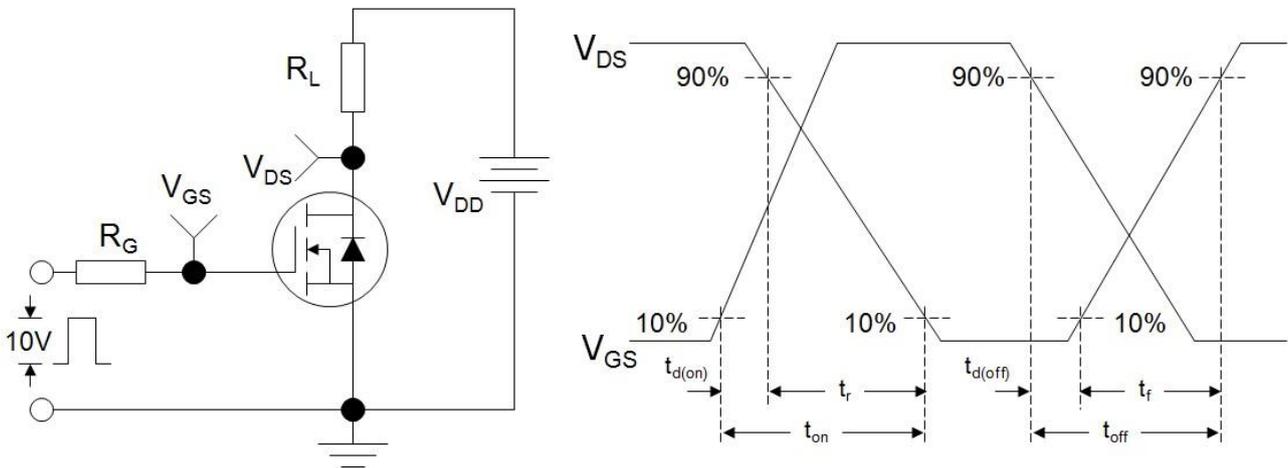
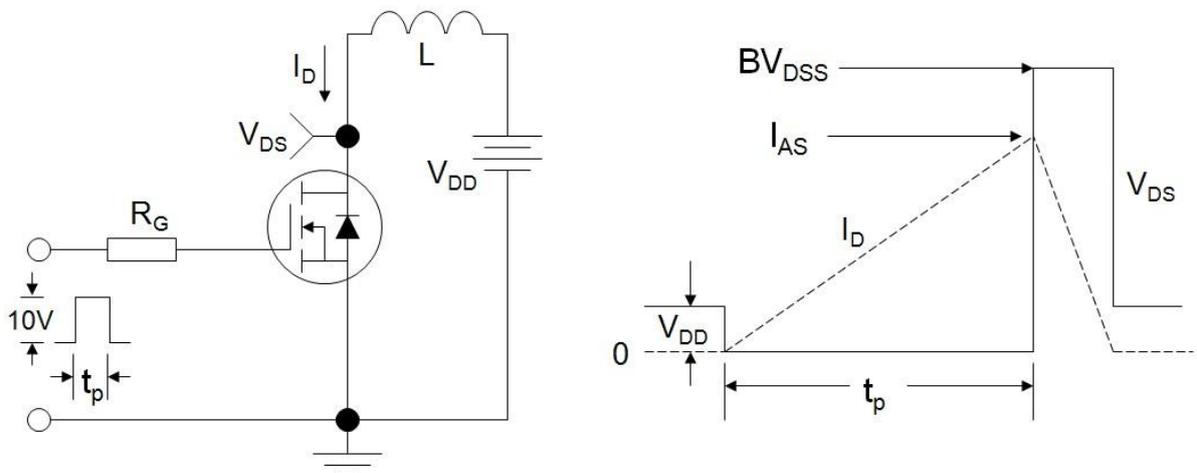
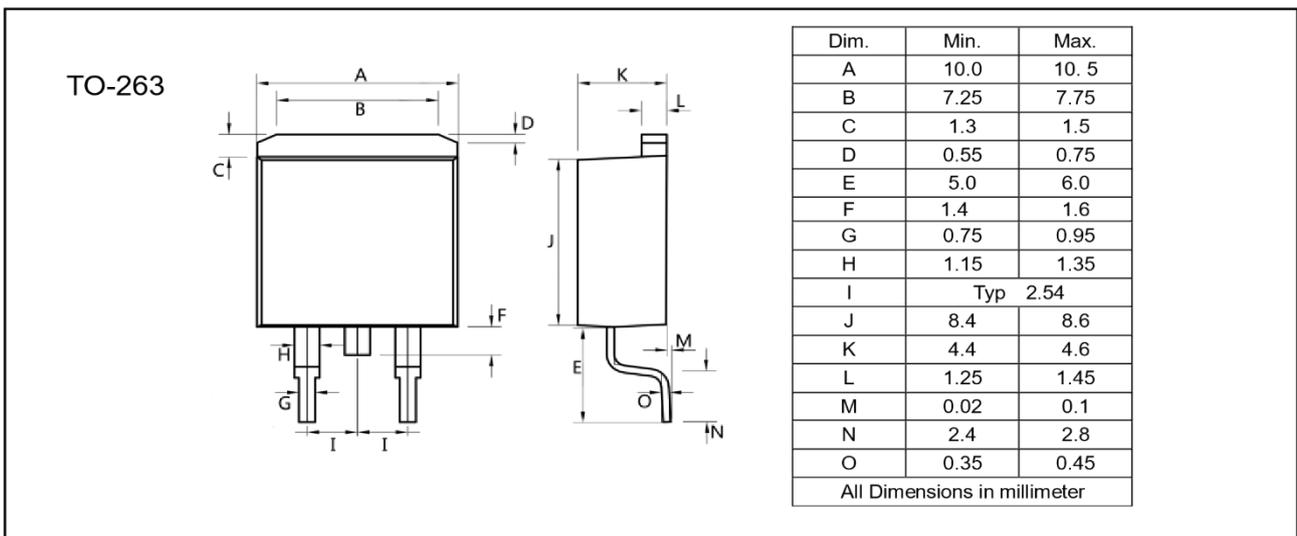
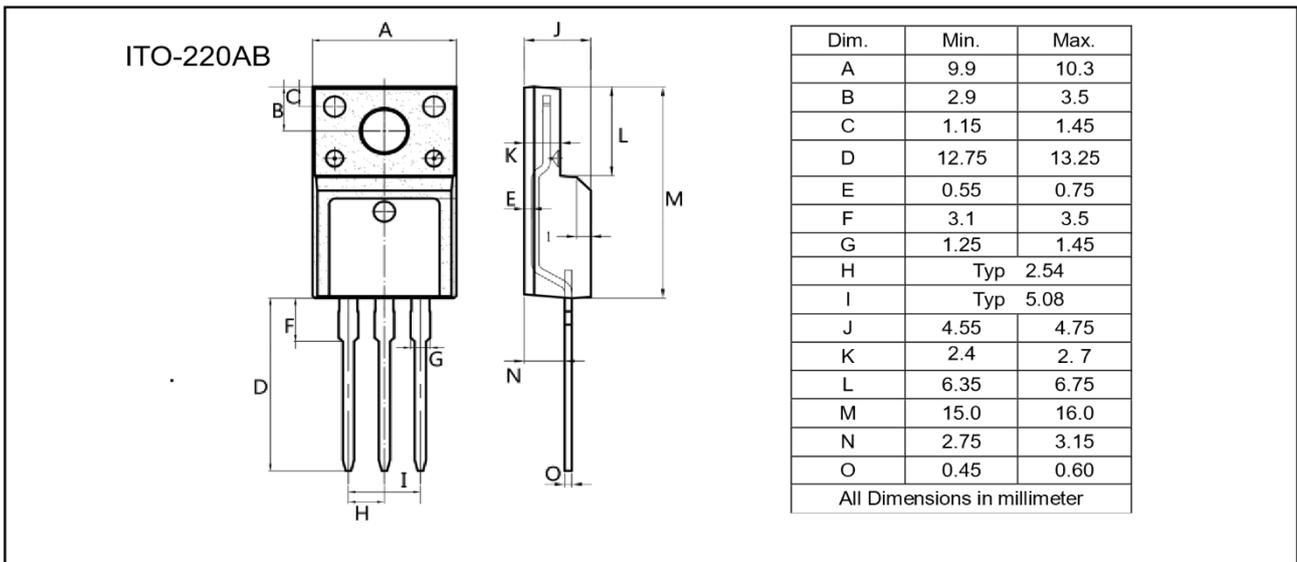
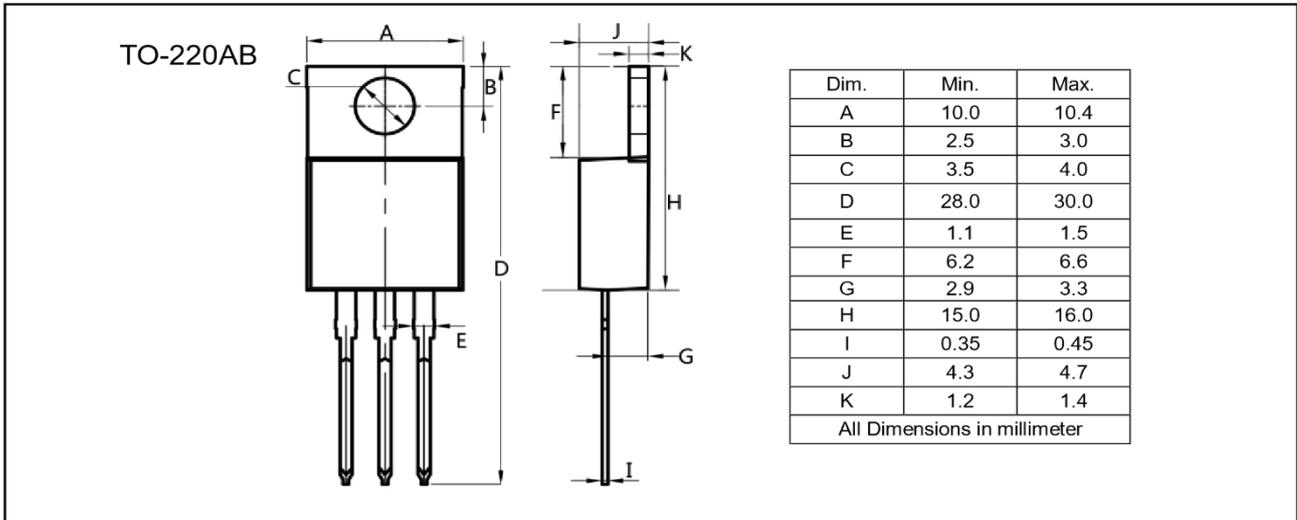


Figure C: Unclamped Inductive Switching Test Circuit and Waveform



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