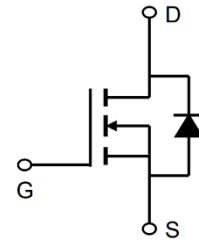


## 80V N- Channel Enhancement Mode MOSFET

### Description

The AP80N08NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = 80V$   $I_D = 80A$

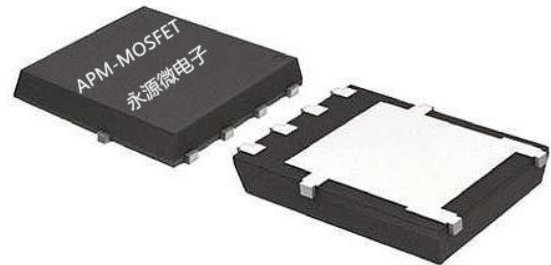
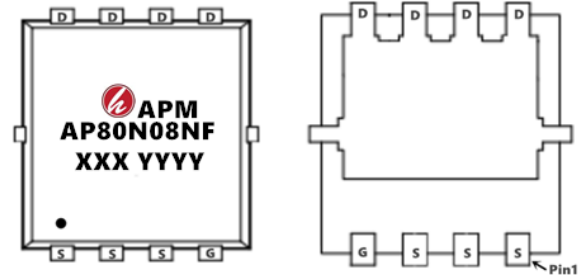
$R_{DS(ON)} < 5.5m\Omega$   $V_{GS} = 10V$

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N08NF	PDFN5*6-8L	AP80N08NF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	80	V
VGS	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	80	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	42.5	A
IDM	Pulsed Drain Current <sup>2</sup>	170	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	57.8	mJ
IAS	Avalanche Current	34	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>4</sup>	56	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.2	$^\circ C/W$

## 80V N- Channel Enhancement Mode MOSFET

### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

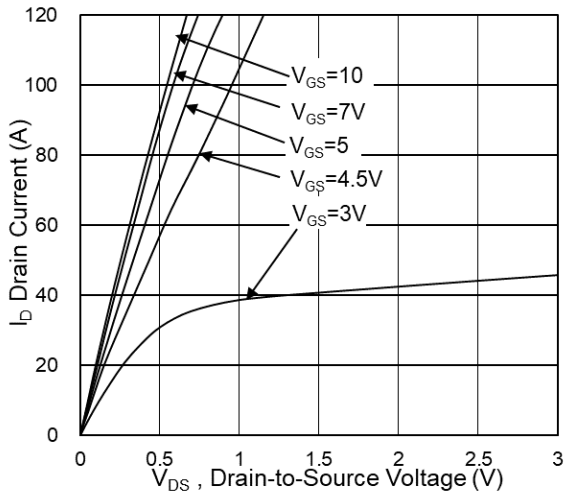
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	80	88	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =20A	---	3.9	5.5	mΩ
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =20A	---	5.5	8.5	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.9	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =64V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =64V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =20A	---	75	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz	---	0.5	---	Ω
Q <sub>g</sub>	Total Gate Charge (10V)	V <sub>DS</sub> =40V , V <sub>GS</sub> =10V , I <sub>D</sub> =20A	---	40	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	7.2	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	6.5	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =40V , V <sub>GS</sub> =10V , R <sub>G</sub> =3Ω, I <sub>D</sub> =20A	---	8.3	---	ns
T <sub>r</sub>	Rise Time		---	4.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	36	---	
T <sub>f</sub>	Fall Time		---	6.9	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =40V , V <sub>GS</sub> =0V , f=1MHz	---	2860	---	pF
C <sub>oss</sub>	Output Capacitance		---	410	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	38	---	
I <sub>s</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	48	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>s</sub> =A , T <sub>J</sub> =25°C	---	0.77	1.0	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =20A , di/dt=100A/μs , T <sub>J</sub> =25°C	---	27	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	89	---	nC

Note :

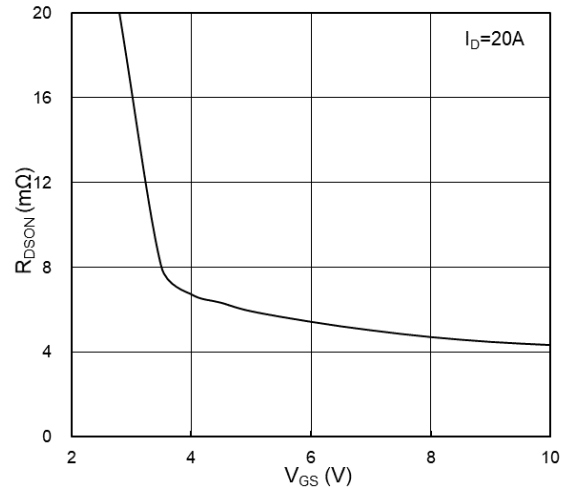
- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V,V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=34A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.
- 6.The maximum current rating is package limited.

## 80V N- Channel Enhancement Mode MOSFET

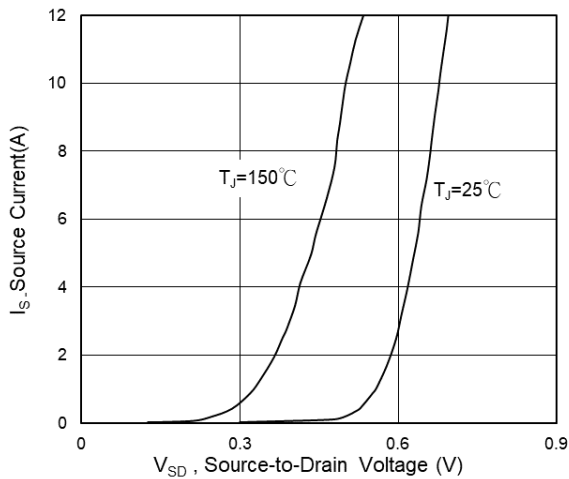
### Typical Characteristics



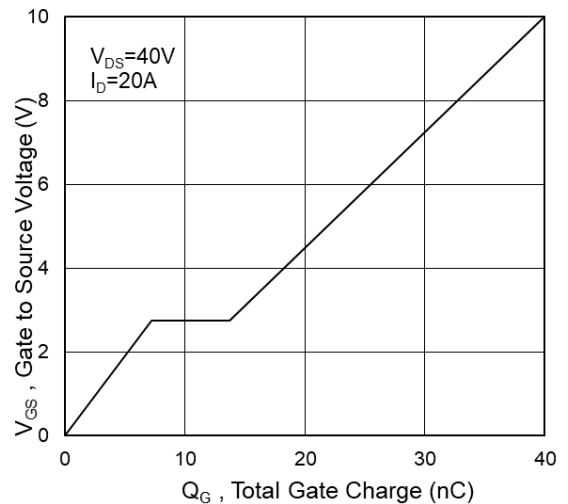
**Fig.1 Typical Output Characteristics**



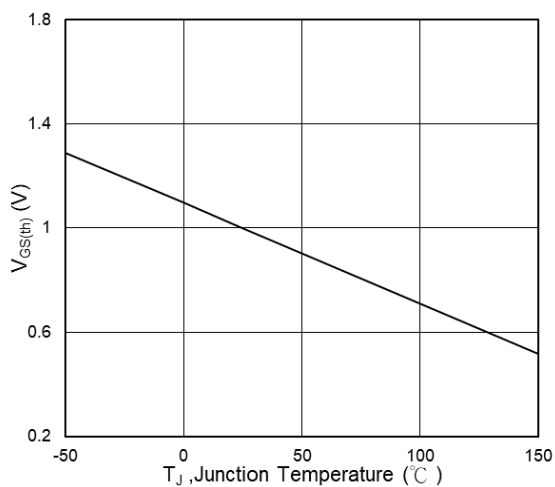
**Fig.2 On-Resistance vs G-S Voltage**



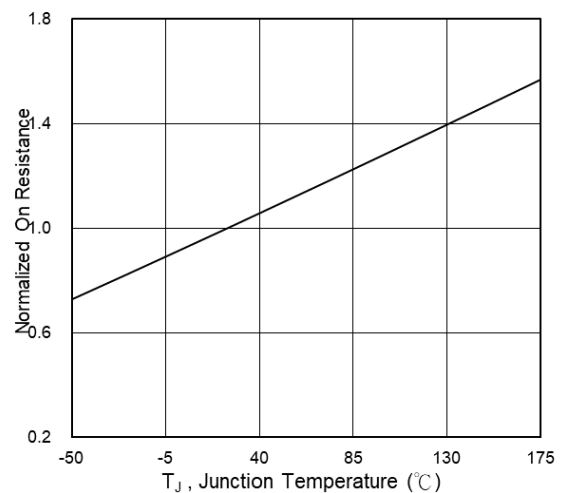
**Fig.3 Source Drain Forward Characteristics**



**Fig.4 Gate-Charge Characteristics**

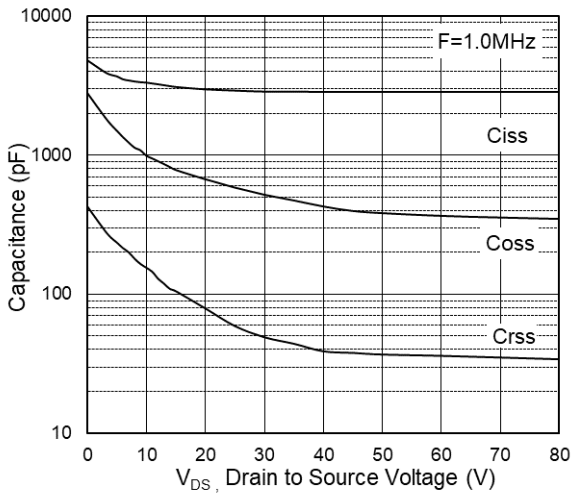


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

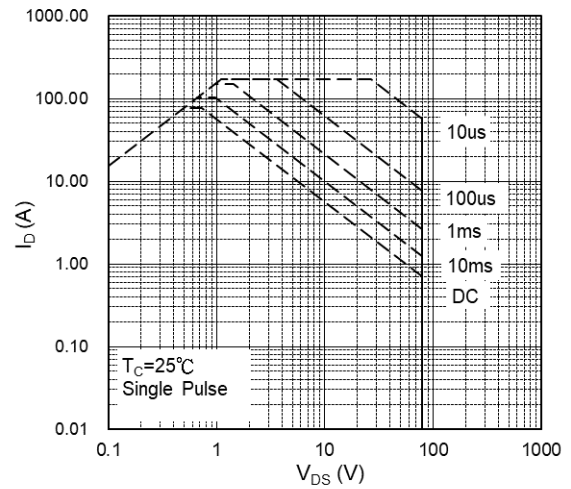


**Fig.6 Normalized  $R_{DSON}$  vs.  $T_J$**

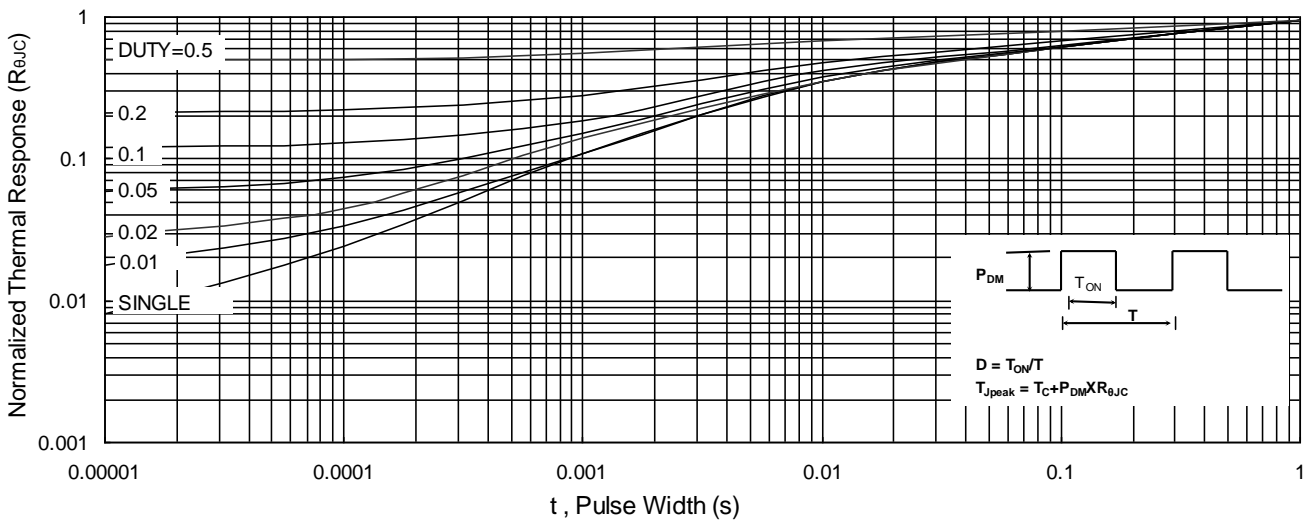
## 80V N- Channel Enhancement Mode MOSFET



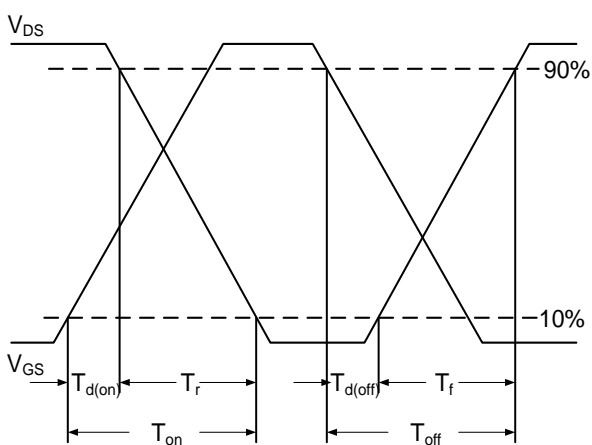
**Fig.7 Capacitance**



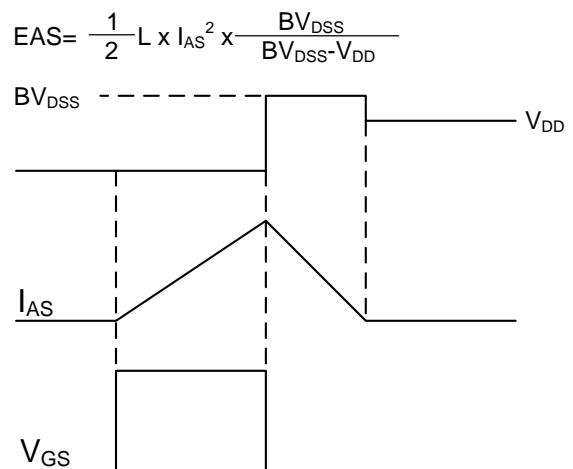
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

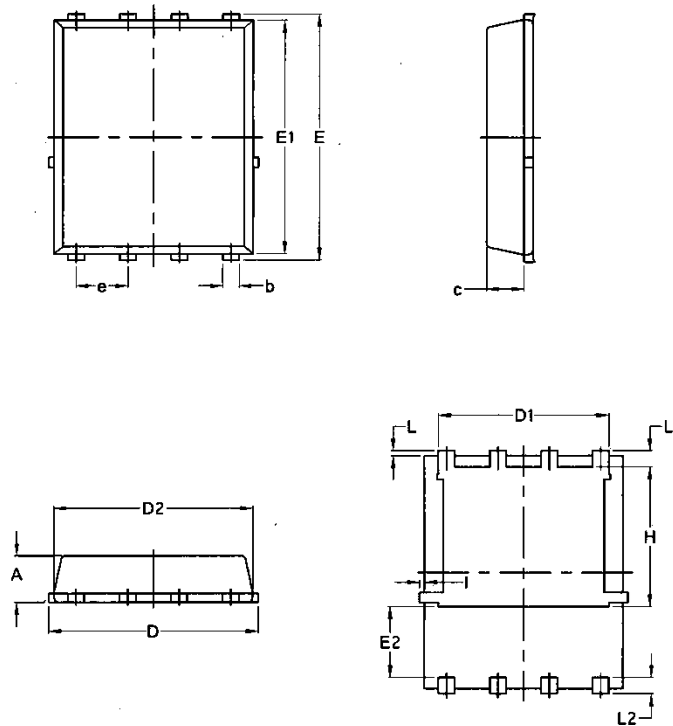


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

## 80V N- Channel Enhancement Mode MOSFET Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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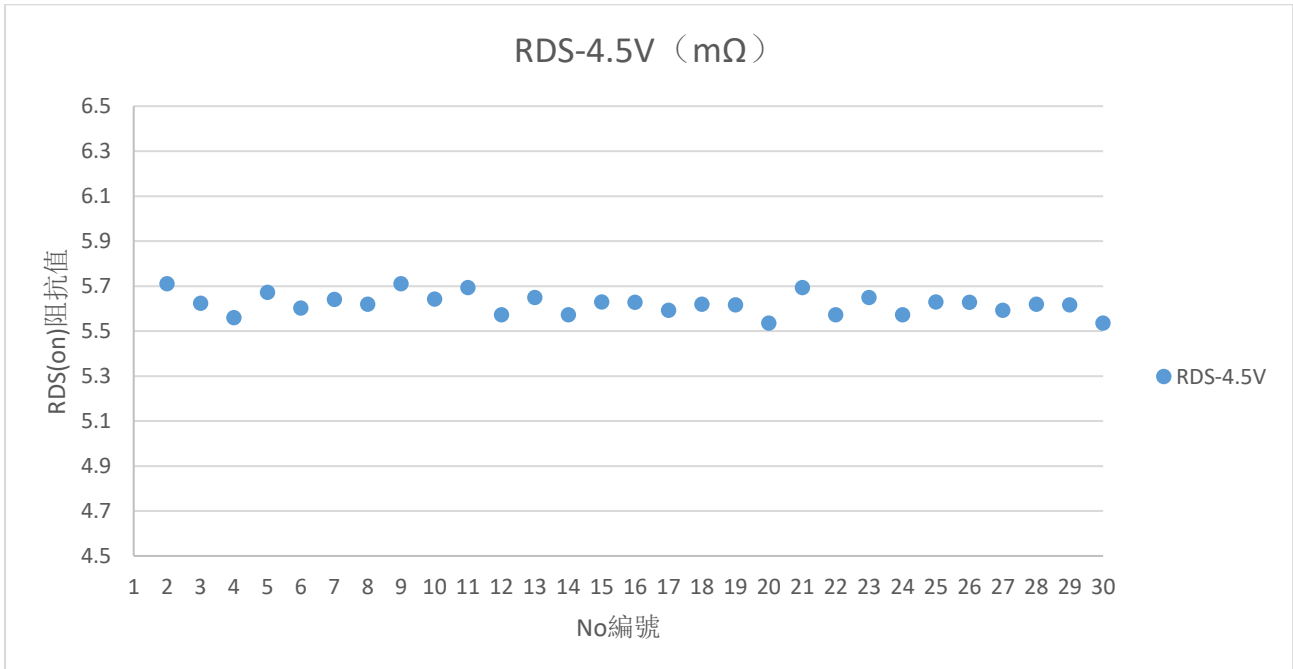
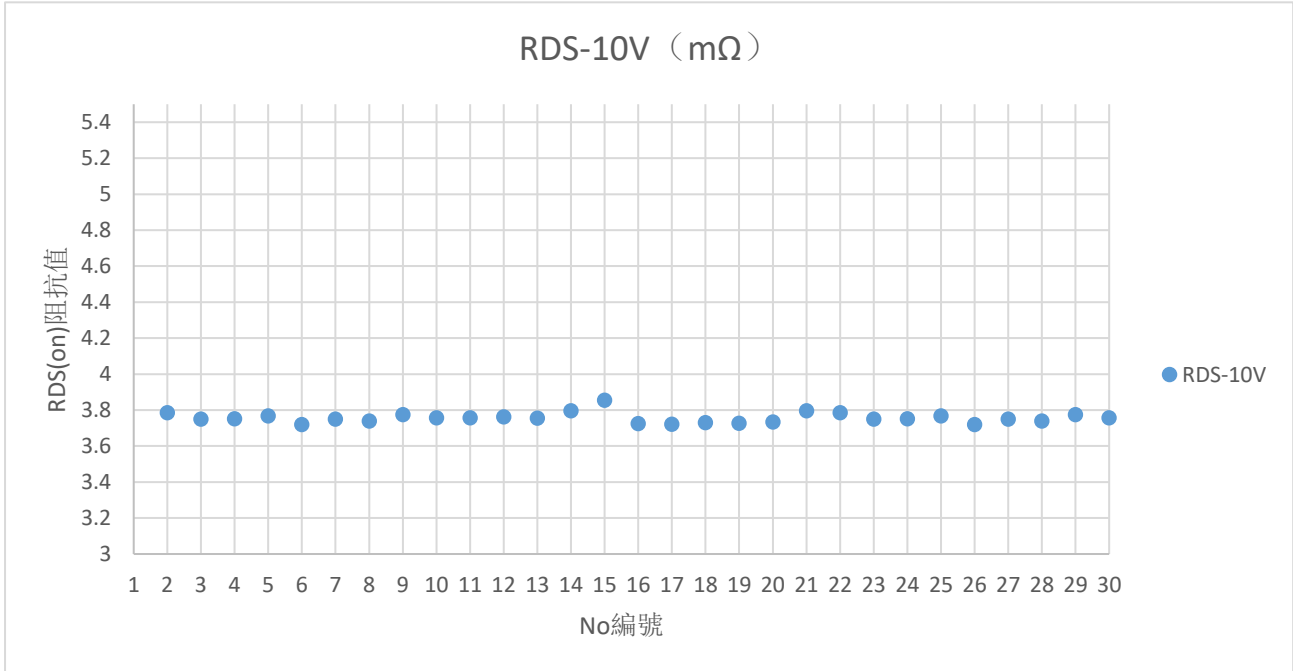
Edition	Date	Change
Rve1.0	2019/8/1	Initial release
Rve2.0	2020/1/01	Reduce RDS(on)

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## 80V N- Channel Enhancement Mode MOSFET

### Test Report For 30PCS (30pcs 典型測試報告)







## 80V N- Channel Enhancement Mode MOSFET

