MXD2660 BLE MCU

Table of Contents

Table of Figures

Table of Tables

Revision History

Version	Date	Description of Change
1.0	Feb 8, 2017	First version
1.1	Mar 15, 2017	Added 2660C package
1.2	Jul 13, 2017	Flash version, F128/F256

Table 1-1 Revision History

1 Overview

MXD2660 is a fully-integrated, single-chip Bluetooth Low Energy (BLE) MCU. It can be used as a standalone application processor or as a wireless connection working with more advanced MCU.

Figure 1-1 MXD2660 Application

2 Features

High level product features

- BLE
  - Compiles with Bluetooth V4.2, and 2Mbps data rate support of BLE 5.0
  - TX: Up to +7dBm transceiver output power
  - RX: -95dBm sensitivity @ 1Mbps
  - Link layer and AES/CCM integrated
- CPU
  - Cortex M0+ @ 48MHz
  - Single cycle multiplier
  - 32 interrupts
- Memory
  - ROM 64KB
  - SRAM 32KB
  - Flash 128KB/256KB
- Power
  - Power supply range: 1.6V ~ 3.6V
  - Hibernation mode (GPIO retention): 0.7uA
  - Sleep mode (BLE linked, 32KB SRAM data retention): 1.2uA
  - BLE TX (with DCDC): 5.8mA @ 0dBm
  - BLE RX (with DCDC): 5.0mA @ 1Mbps
- Clock
  - 16MHz crystal and RC oscillator
  - 32KHz crystal and RC oscillator
  - 16MHz to 32MHz/48MHz PLL
- Timer
  - 32-bit timer
  - Six 16-bit general purpose timers (PWM/Infra-Red generator)
  - Real timer clock
  - Watchdog
- Digital Interface
  - 31 general purpose I/Os. Function IO any-route support
  - 2 UARTs with hardware flow control up to 1MBd
  - 2 SPIs with master/slave configurable
  - 2 I2Cs with master/slave configurable
  - I2S data in interface
  - 7816 T-0 master interface
  - Keyboard interface
- Analog Interface
  - 8-channel 10-bit ADC

- Temperature sensor
- DMA
  - 5-channel
- Packages
  - MXD2660A (2660A-F128, 2660A-F256), QFN 40 pins, 5 mm x 5 mm
  - MXD2660B (2660B-F128, 2660B-F256), QFN 48 pins, 6 mm x 6 mm
  - MXD2660C (2660C-F256), LGA 49 pins, 3 mm x 3 mm

3 Block Diagram

MXD2660 top level functional block diagram is shown below in Figure 2-1.

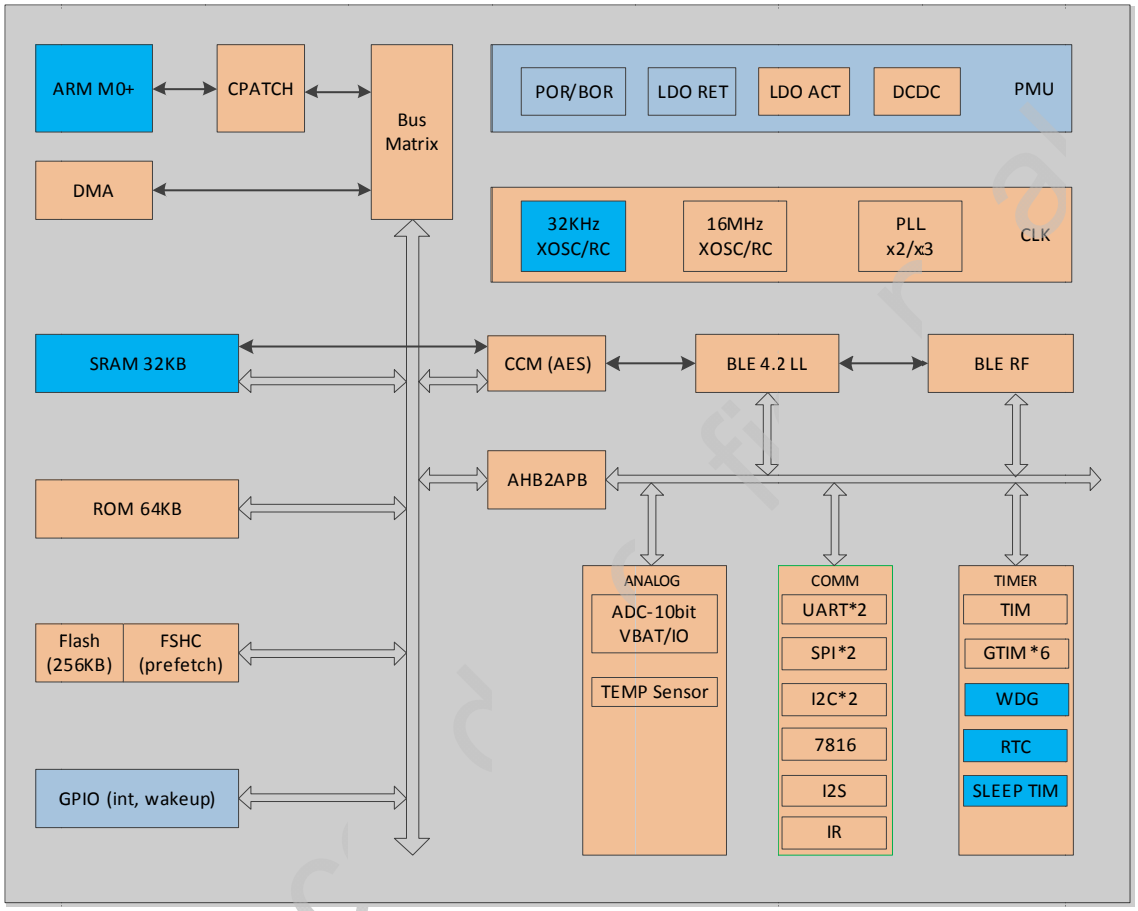


Figure 3-1 MXD2660 Functional Block Diagram

4 Pinout

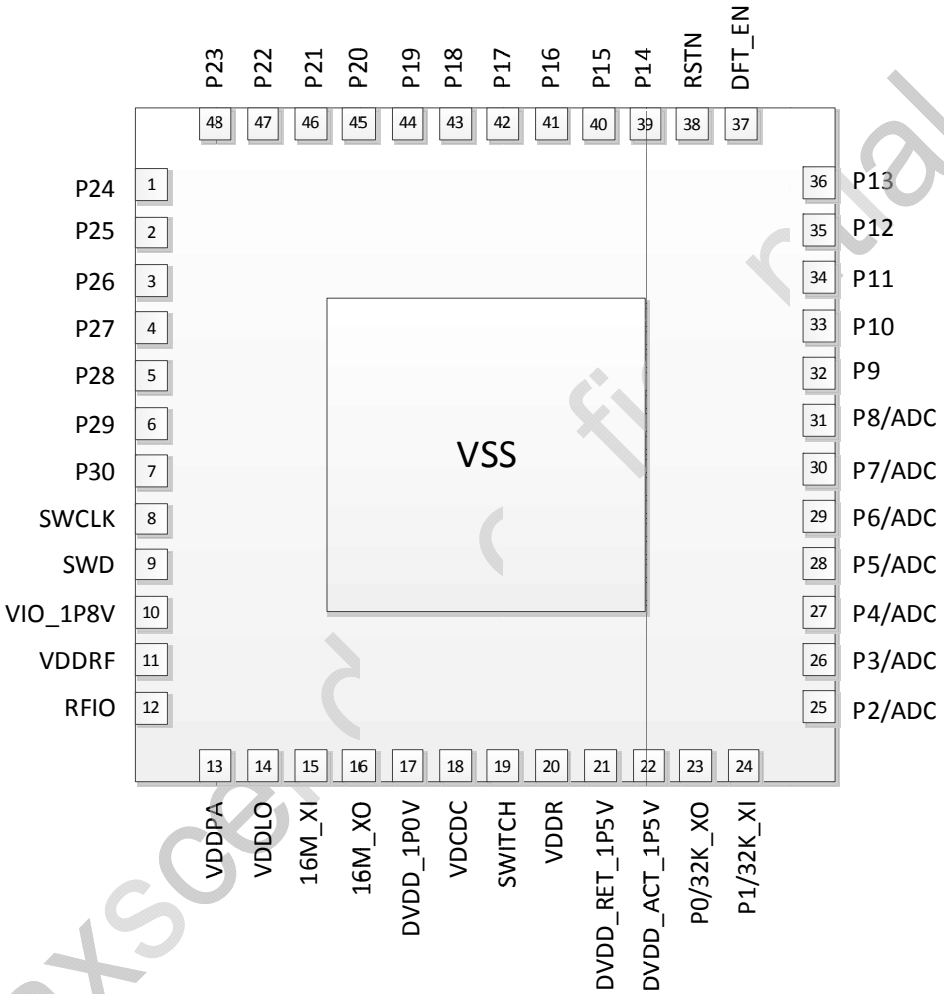


Figure 4-1 MXD2660B QFN48 6x6 Package Top View

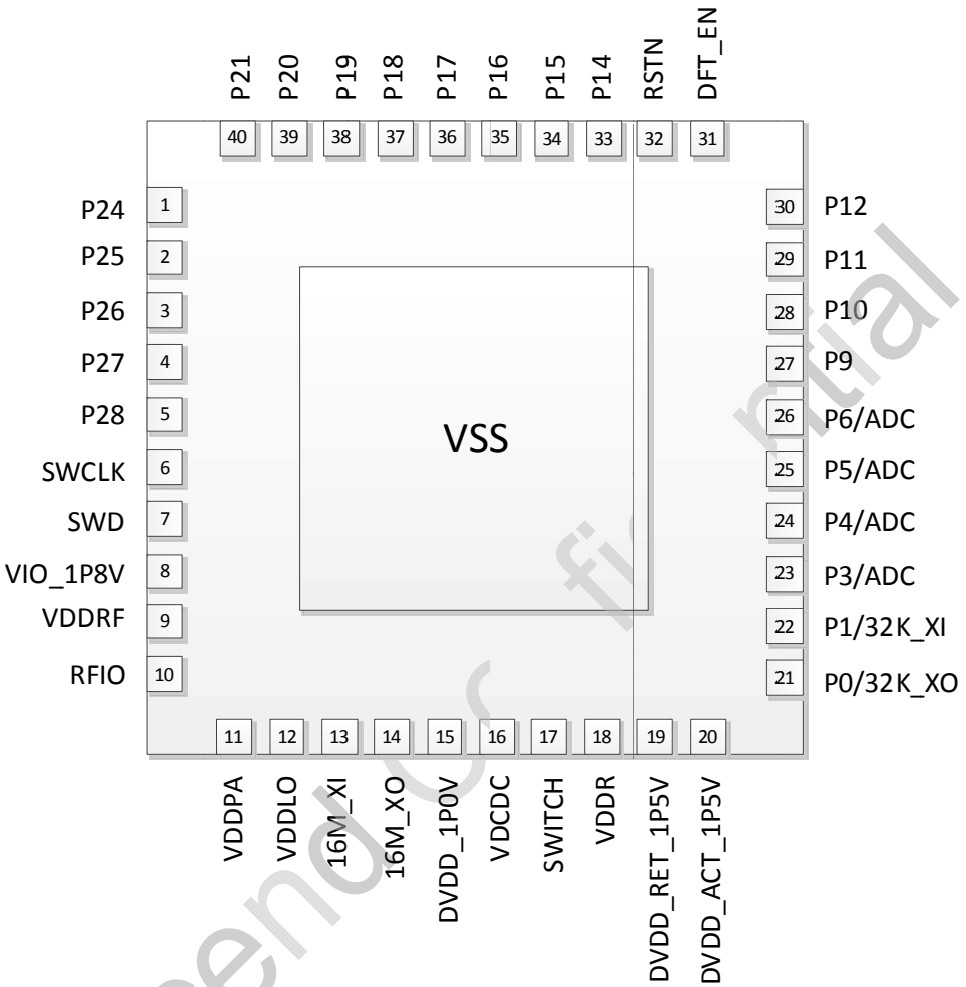


Figure 4-2 MXD2660A QFN40 5x5 Package Top View

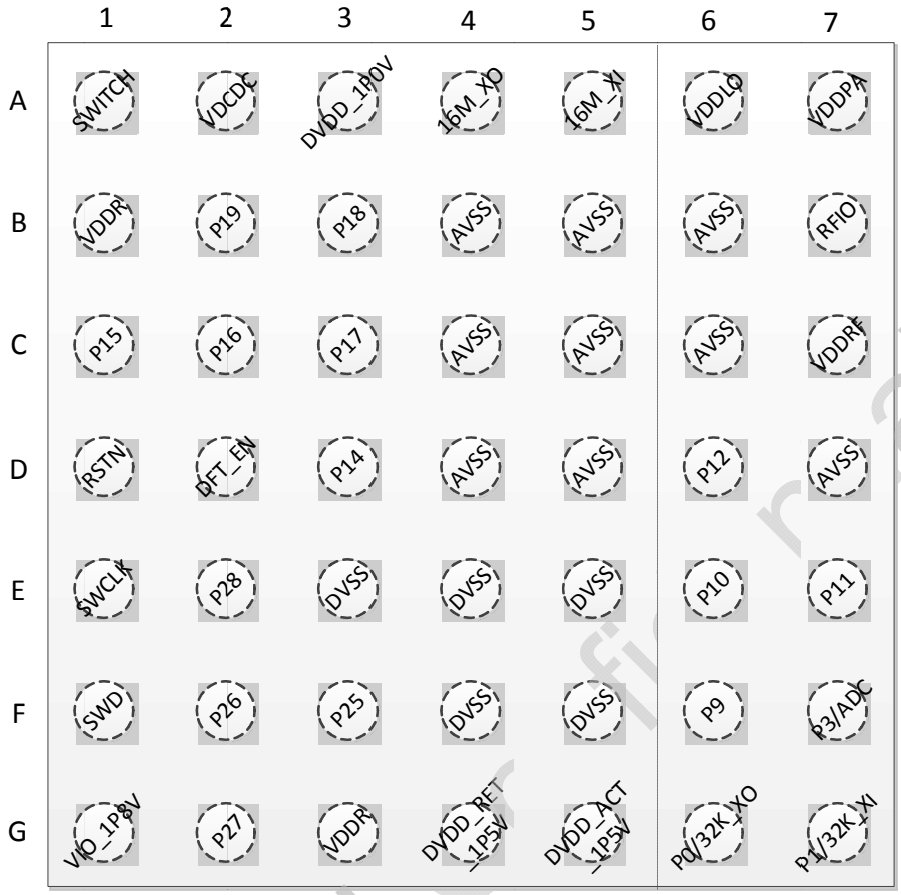


Figure 4-3 MXD2660C LGA49 3x3 Package Top View

Note

DIO (digital bidirectional), *DI* (digital input), *AI* (analog input), *AIO* (analog bidirectional).

I- *PD* (input pull-down), *I-PU* (input pull-up).

Table 4-1 Pin Description

Pin Name	Type	Drive (Ma)	Reset State	Description
General Purpose I/Os				
P9 ~ P30	DIO	4/8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. Pull-down enabled during and after reset. Contains state retention mechanism during power down. Digital interface can be routed to any IO of P0 ~ P30.
General Purpose I/Os with analog function				
P0/32K_XO	DIO	4/8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. Pull-down enabled during and after reset. Contains state retention mechanism during power down. Digital interface can be routed to any IO of P0 ~ P30.

				It can be used as 32K XO too.
P1/32K_XI	DIO	4/8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. Pull-down enabled during and after reset. Contains state retention mechanism during power down. Digital interface can be routed to any IO of P0 ~ P30. It can be used as 32K XI too.
P2/ADC, P4/ADC ~ P8/ADC	DIO	4/8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. Pull-down enabled during and after reset. Contains state retention mechanism during power down. Digital interface can be routed to any IO of P0 ~ P30. It can be used as ADC input too.
P3/ADC	DIO	4/8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. Pull-up enabled during and after reset. Contains state retention mechanism during power down. Digital interface can be routed to any IO of P0 ~ P30. It can be used as ADC input too.
Debug Interface				
SWCLK	DIO	4/8	I-PD	INPUT/OUTPUT. Serial wire clock signal. Can also be used as a GPIO (digital interface any route is not supported).
SWD	DIO	4/8	I-PU	INPUT/OUTPUT. Serial wire data signal. Can also be used as a GPIO (digital interface any route is not supported).
Clocks				
16M_XI	AI			INPUT. Crystal input for the 16MHz XTAL.
16M_XO	AO			OUTPUT. Crystal output for the 16MHz XTAL.
Radio transceiver				
RFIO	AIO			RF input/output.
Miscellaneous				
RSTN	DI			INPUT. Reset signal (active low). Must be connected to VDDR if not used.
DFT_EN	DI			INPUT. Must be connected to GND for application.
VIO_1P8V	AIO			Connect to external capacitor
DVDD_1P0V	AIO			Connect to external capacitor
DVDD_RET_1P5V	AIO			Connect to external capacitor
DVDD_ACT_1P5V	AIO			Connect to external capacitor
VDDRF	AIO			Connect to VDCDC
VDDPA	AIO			Connect to VDCDC

VDDLO	AIO			Connect to VDCDC
Power supply				
VDDR	AIO			Battery connection
VDCDC	AO			Output of the DC-DC converter
SWITCH	AIO			Connection for the external DC-DC converter inductor
VSS	AIO			Ground
AVSS	AIO			Analog Ground
DVSS	AIO			Digital Ground

5 System Overview

5.1 Power Modes

Hibernation mode: All IOs hold their status they had before entering hibernation mode. All power domains are off except for PD_TOP, which include IO and PMU. All clock sources are off, including the RC32K. This mode can be waked up by a change of state on any I/O pin, and after wake, CPU will reset and restart from 0x0 address. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on-reset by reading the reset status register.

Sleep mode: All IOs hold their current status. All power domain are retentive, including 32KB SRAM. All clock sources are off except for the RC32K or XO32K. This mode can be wakeup by any IO, RTC, or Link layer timer. And after wake, CPU will continue the instructions from where it went into Sleep.

5.2 ARM Cortex-M0+ CPU

The Cortex-M0+ processor is a 32-bit Reduced Instruction Set Computing (RISC) processor with a von Neumann architecture (single bus interface). It implements the ARMv6-M architecture, which is based on the 16-bit Thumb (ARM7TDMI) instruction set and includes Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than 8-bit and 16-bit microcontrollers.

5.3 Bluetooth Low Energy

5.3.1 BLE Core

The BLE core is a qualified Bluetooth baseband controller compatible with the Bluetooth Smart specification and it is in charge of packet encoding/decoding and frame scheduling. It performs Link Layer Control management supporting the main BLE states, including advertising and connection.

Feature:

1. All device classes support (Broadcaster, Central, Observer, Peripheral)
2. Simultaneous Master and Slave operation
3. Frequency Hopping
4. All packet types (Advertising / Data / Control)
5. Encryption (AES / CCM)
6. Bit stream processing (CRC, Whitening)
7. Operating clock 16MHz
8. Low power modes supporting 32.768 kHz

5.3.1.1 Sleep Timer

In low power mode, the sleep timer is working and the clock is 32.768kHz, which can be from 32KHz RC or 32KHz Crystal.

5.4 Memories

The below memories are part of MXD2660's internal blocks:

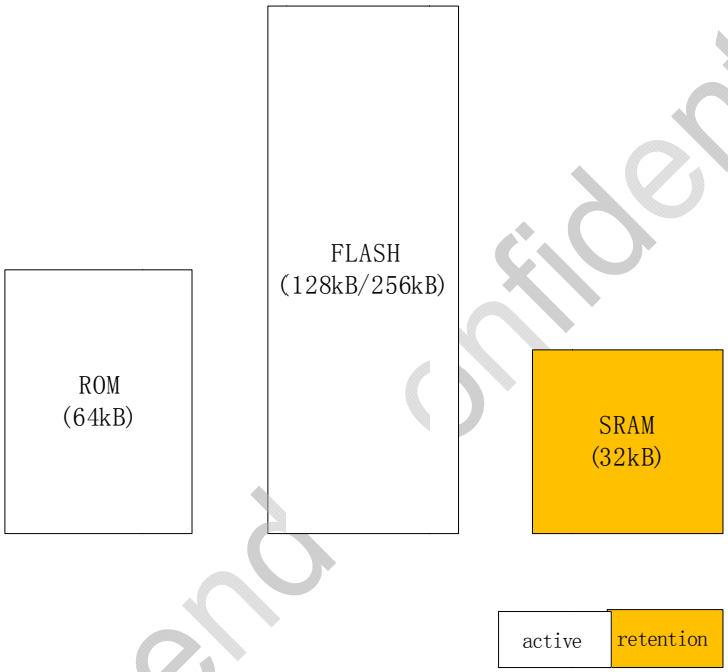


Figure 5-1 MXD2660 memory

1. ROM: This is a 64 KB ROM containing the Bluetooth Smart protocol stack as well as the boot code sequence.
2. Retention SRAM: There is 32KB retention SRAM used to store various data of the Bluetooth Smart protocol as well as the system's global variables and processor stack when the system goes into Sleep mode. Storage of this data ensures secure and quick configuration of the BLE Core after the system wake up.
3. Flash: This is a Flash memory, which is optional 128KB/256KB. Flash memory is used to store the application code and code for all supported Bluetooth Smart profiles.

5.5 Interfaces

5.5.1 UART

The UART is compliant to the industry-standard 16550 and is used for serial communication with a peripheral data set. Data is written from a master (CPU/DMA) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU/DMA) to read back. Both UARTs support hardware flow control signals (RTS, CTS).

Feature:

1. 8 bytes transmit and receive FIFOs
2. Hardware flow control support (CTS/RTS)
3. Functionality based on the 16550 industry standard
4. Programmable character properties, such as number of data bits per character (5-8), optional
5. Parity bit (with odd/even/stick/no select) and number of stop bits (1, 1.5 or 2)
6. Line break generation and detection
7. RX timeout interrupt support
8. Programmable serial data baud rate

5.5.2 SPI

This interface supports a subset of the Serial Peripheral Interface SPITM. The serial interface can transmit and receive 8, 16, 32 bits or as long as data in master/slave mode. Data is written from a master (CPU/DMA) over the APB bus to the SPI.
SPI™ is a trademark of Motorola, Inc.

Feature:

1. 8 bytes transmit and receive FIFOs
2. Slave and Master mode
3. 8 bit, 16 bit, 32 bit or as long as data operation
4. SPI clock line speed up to 8 MHz. Programmable output frequencies in master mode.
5. SPI mode 0, 1, 2, 3 support (clock edge and phase)
6. Programmable SPI_DO idle byte
7. RX timeout interrupt support
8. Programmable TX only/RX only/TRX mode

5.5.3 I2C

The I2C interface is a programmable control bus that provides support for the communications link between Integrated Circuits in a system. It is a simple two-wire bus with a software-defined protocol for system control, which is used in temperature sensors and voltage level translators to EEPROMs, general-purpose I/O, A/D and D/A converters.

Feature:

• Two-wire I2C serial interface consists of a serial data line (SDA) and a serial clock (SCL)
• Two speeds are supported: standard mode (0 to 100 kbit/s) and fast mode (<= 400 kbit/s)
• 8 bytes transmit/receive FIFOs
• Configurable master or slave, transmit/receive operation
• 7 or 10-bit addressing
• configurable slave address and target address
• Interrupt operation

5.5.4 I2S

This interface can be used to receive audio sample streams between MXD2660 and external audio output devices, such as ADCs.

Feature:

- Slave and Master mode
- I2S, LJF, and DSP(PCM a&b) format
- 16 bit, 20 bit, 24 bit operation
- MCLK output (16M, 8M, 4M, 2M)
- fs (8K, 16K 32K)

5.5.5 General Purpose ADC

The MXD2660 is equipped with a low power general purpose SARADC.

Feature:

- Eight single-ended channels
- One channel for battery monitoring, and seven channels for IO voltage monitoring
- Conversion time and dynamic range can be changed

5.5.6 7816

This smart card interface is compatible with the ISO 7816-3 and EMV 4.2 related standards. As a master device, it can transmit data controlled by CPU/DMA to destination card, and also it can receive data stored in SRAM.

Feature:

1. Supports the asynchronous protocols T = 0 in accordance with ISO 7816-3
2. Flexible output clock 1m,2m,4m
3. Error management at character level for T=0 that parity error counter in reception mode and in transmission mode with auto-repetition.
4. 32-bit counting by ETU clock for time-out counter.
5. Power-down mode for reducing current consumption when no activity.

5.5.7 Keyboard

The Keyboard controller can be used for debouncing the incoming GPIO signals when implementing a keyboard scanning engine. It generates an interrupt to the CPU (KBRD_IRQ). In parallel, six extra interrupt lines can be triggered by a state change on 31 selectable GPIOs (GPIOx_IRQ).

Feature:

1. Monitors any of the 31 available GPIOs
2. Implements debouncing time from 0 up to 63 ms
3. Supports six separate interrupt generation lines from GPIO toggling

5.5.8 DMA

The DMA controller provides a way to offload data transfer tasks from the CPU, allowing for more efficient use of the processor and the available bus bandwidth. The DMA controller can perform transfers between memory and peripherals. The controller has dedicated channels for each supported on-chip module, and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

Feature:

1. Support memory to memory, memory to peripheral and peripheral to memory transmission
2. Support UART, SPI, I2C, 7816, I2S interface
3. 5 independent DMA channels
4. Configurable 2 level priority
5. Independent source and destination transfer size(8bit, 16bit, 32bit)
6. Support circular mode
7. Programmable number of data to be transferred: up to 65535
8. Source and destination address increment or no increment

5.5.9 Input/output ports

The MXD2660 has software-configurable I/O pin assignment. gpio, uart, spi, i2c, pwm, 7816, i2s, ir all these interfaces can be configured to any one of the 31 pins.

Feature:

1. 31 configurable pins
2. Fully programmable pin assignment
3. Configurable pull-up, pull-down
4. Configurable schmitt trigger or cmos input

5.6 Timers

5.6.1 General Purpose Timers

The Timer block contains 2 kinds of timer modules that are software controlled, programmable and can be used for various tasks.

Timer 0

• 32-bit up counter with 4 bit pre-scale general purpose timer with 16Mhz Working clock frequency
• Generates compare and overflow interrupt.

Timer 1-6: Every timer can generate one Pulse Width Modulated Signals (PWM) output, with 16bit programmable output frequency and programmable duty cycle

• 16-bit general purpose timer 4 bit pre-scale Counter up with 16Mhz working clock frequency
• Ability to generate 6 Pulse Width Modulated signals (PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5)
• PWM supports smooth parameter change
• PWM supports programmable duty cycle and frequency (16Hz~8MHz)

IR: Timer1 and Timer2 can be used to generate IR signal output

5.6.2 Real Time Counter

The Real Time Counter can be programmed to wake up the chip from power down mode after a preprogrammed time.

Feature:

• 40 bit Real Time Counter with 12 bit pre-scale with 32.768KHz working clock frequency
• Implements tick, 4-channel compare and overflow events
• Generates wake-up to PMU

• Generates interrupt to CPU

5.6.3 Watchdog Timer

The Watchdog timer is an 32-bit timer with 32.768KHz working clock frequency that can be used to detect an unexpected execution sequence caused by a software run-away and can generate a full system reset or a Non-Maskable Interrupt (NMI).

Feature:

• 32 bits Counter up with 0.03052ms step for a maximum 131082s time-out .

• Non-Maskable Interrupt (NMI) or WDOG reset.

• NMI interrupt can be selected masked 16*0.03052ms ahead before WDOG reset.

5.7 Clock/Reset

clock :

There are 3 high frequency clock sources: RC16M(16mhz), XO16M(16mhz) and PLL(x2 or x3) which are used for CPU, memory, peripherals and BLE. And there are also 2 32khz clock sources: RC32K and XO32K, which are used in RTC and PMU for SLEEP mode.

reset:

There is a RESET PAD which is low active. It contains a 30k pullup resistor.

6 Specifications

6.1 Recommended Operating Conditions

Ta=25℃, VIN=3.3V, unless otherwise specified.

Parameter	Ratings			Unit
	Min.	Typ.	Max.	
Power Supply Voltage (VDDR)	1.6	3.0	3.6	V
Junction Temperature	-40	--	125	℃

Table 6-1 Recommended Operating Conditions

6.2 DC Characteristics

Ta=25℃, VIN=3.0V, unless otherwise specified.

Parameter	Ratings			Unit
	Min.	Typ.	Max.	
VIH (Logic-1 input voltage)	2.0			V
IIH (Logic-1 input current)			+1	uA
VIL (Logic-0 input voltage)			0.8	V
IIL (Logic-0 input current)	-1			uA
VOH (Logic-1 output voltage, IOL = -8/-4mA)	2.4			V
VOL (Logic-0 output voltage, IOH = -8/-4mA)			0.4	V
Rx Mode (Typical application with buck converter and receiver active)		5.0		mA
TX mode, 0 dBm output power (Typical application with buck converter and transmitter active)		5.8		mA
CPU active (running from flash)		200		uA/MHz
CPU idle		65		uA/MHz
Hibernation mode (SRAM no retention, IO retention and IO wakeup)		0.7		uA
Sleep mode (SRAM 32kB retention, BLE linked, flash sleep included)		1.2		uA
FLASH Read (active mode, read operation,16MHz)		2.5	3.5	mA
FLASH Write (active mode, write operation,16MHz)			3.5	mA
FLASH Erase (active mode, sector erase operation, 16MHz)			2	mA
Flash Sleep		0.05		uA

Table 6-2 DC Characteristics

6.3 Transceiver Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Sensitivity		Pmin		-95		dBm
Sensitivity(dirty on)				-94		dBm
Maximum input power		Pmax		0		dBm
In-band blocking	Co-channel interference	CI0		9		dB
	Interferer at f_{offs}= +1MHz	CI1		+2		dB
	Interferer at f_{offs}= -1MHz	CI1		+1		dB
	Interferer at f_{offs}= +2MHz	CI2		-26		dB
	Interferer at f_{offs}= -2MHz	CI2		-23		dB
	Interferer at f_{offs}= +3MHz	CI3		-33		dB
	Interferer at f_{offs}= -3MHz	CI3		-31		dB
	Interferer at image channel (Fimage)	CI4		-23		dB
	Interferer at image channel(Fimage+1MHz)	CI5		+1		dB
	Interferer at image channel (Fimage-1MHz)	CI5		-31		dB
Out-of-band blocking	f= 30 – 2000MHz			-30		dBm
	f= 2000 – 2399 MHz			-35		dBm
	f= 2484 – 3000 MHz			-35		dBm
	f= 3000 – 12750 MHz			-30		dBm
Intermodulation Performance for Wanted Signal at -64dBm and 1 Mbps BLE, 3rd, 4th and 5th offset channel				-50		dBm
Upper limit of monotonous range		Pissi(max)		-20		dBm

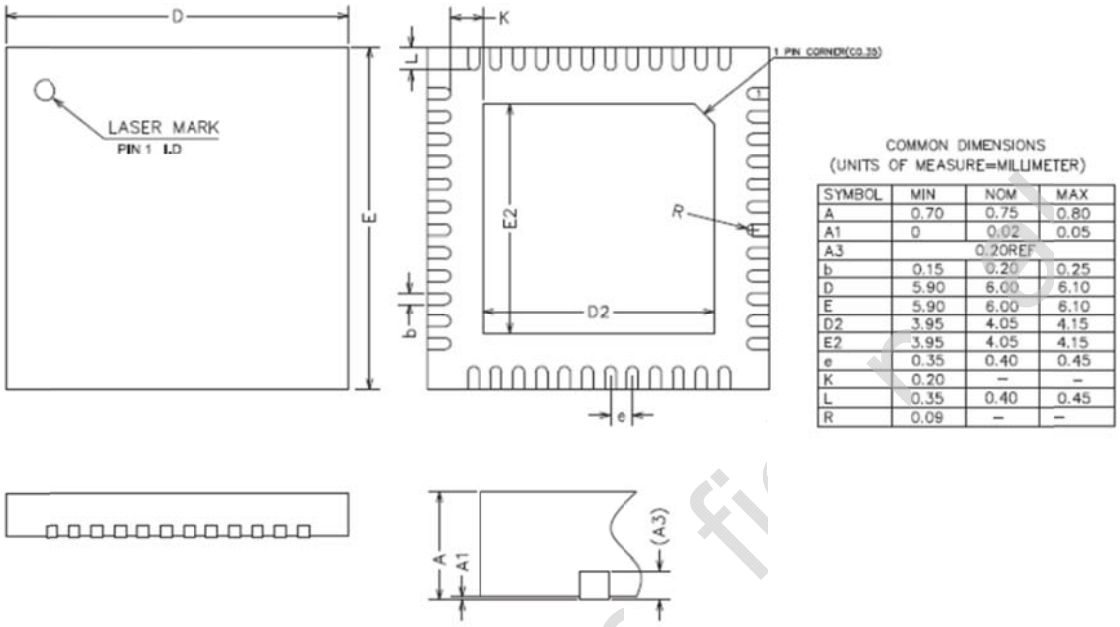
Table 6-3 RX Characteristic

Parameters		Symbol	Min	Typ	Max	Unit
Output power		Ptx	-20		+7	dBm
TX RF Output Steps				3		dB
Average Frequency deviation for 10101010 pattern		ΔF2AVG		230		KHz
Average Frequency deviation for 11110000 pattern		ΔF1AVG		250		KHz
Eye opening = ΔF2AVG/ΔF1AVG		EO		0.9		
Frequency Accuracy			-15		15	KHz
Maximum Frequency Drift			-15		15	KHz
Initial Frequency drift			-15		15	KHz
Drift rate		FDR	-12		12	KHz/50μs
Spurious Emissions	F < 1 GHz			-68		dBm
	F > 1 GHz including harmonics			-48		dBm
In-band Emissions	< f ± 2MHz (f=2400~2483.5MHz,Ptx=0dBm)			-45		dBm
	> f ± 3MHz			-55		dBm

	(f=2400~2483.5MHz,Ptx=0dBm)					

Table 6-4 TX Characteristic

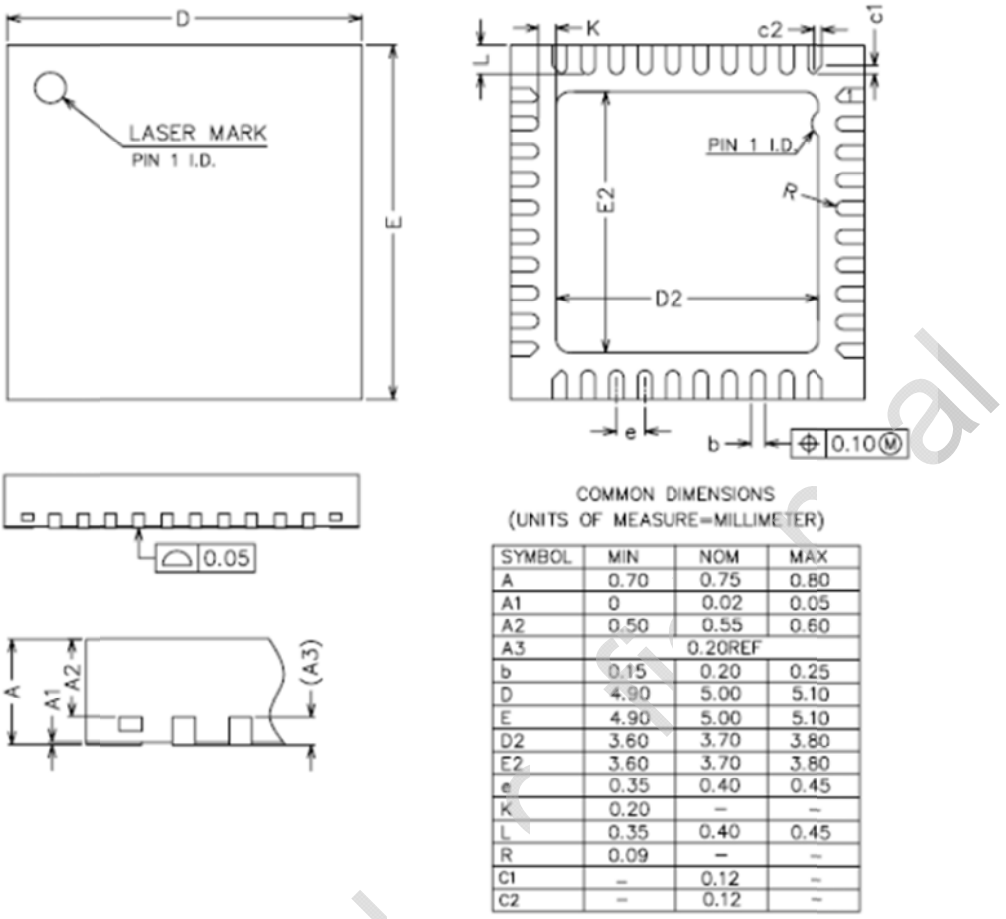
7 Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

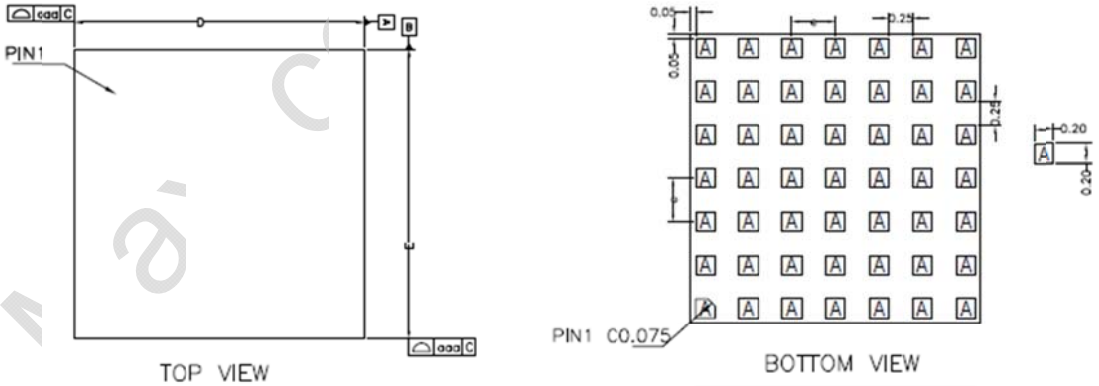
Figure 7-1 MXD2660B QFN48 Package Outline Drawing



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
C1	–	0.12	–
C2	–	0.12	–

Figure 7-2 MXD2660A QFN40 Package Outline Drawing



MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	0.64	0.72	0.80
A2	0.09	0.12	0.15
A3	0.55	0.60	0.65
D	2.95	3.00	3.05
E	2.95	3.00	3.05
e	BSC 0.45		
aaa	0.10		
ccc	0.05		

Figure 7-3 MXD2660C LGA49 Package Outline Drawing

MXD2660 Datasheet

Room 202, No. 50 Bo Xia Road,
Zhangjiang, Shanghai, China (201203)

TEL: +86-21-61006488
FAX: +86-21-61009682
E-MAIL: info@maxscend.com
WEB: www.maxscend.com