USB Power Delivery 3.0 Controller with Integrated Current Sense Supports Qualcomm Quick Charge 4+

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1 Description

The iW657P is a USB Power Delivery (USB PD) interface controller which handles the communication between a Power Adapter and Mobile Device (MD). The controller enables the mobile device to alter the V_{BUS} voltage from the default 5V and/or maximum current limitation (e.g. 3A) for higher power output or better efficiency. The iW657P supports USB PD 3.0, including Programmable Power Supply (PPS) support, while being backwards compatible with USB PD 2.0. The device also supports Qualcomm® Quick Charge™ 4+ technology. The iW657P enables the use of advanced USB Type-C™ connector technology with CC1/CC2 pins for MD attach/detach detection and V_{CONN} support for Electronically Marked Cable (EMC) rated current reading. The iW657P also integrates a high current charge-pump circuit to drive an external NFET V_{BUS} disconnect switch.

The iW657P resides on the secondary side of an AC/DC power supply and negotiates voltage and current settings with the primary-side controller, depending on the requests from the MD. The iW657P uses Dialog's proprietary secondary-to-primary digital communication technology and when paired with one of Dialog's primary-side ***RapidCharge***™ controllers, such as the iW1791 or iW1799, the iW657P eliminates the need for a discrete decoder on the primary side by using one optocoupler to transmit all necessary information for rapid charging to the primary side. This includes output voltage requests, output current limits, output voltage undershoot, output over-voltage, and fault and reset signals. The iW657P incorporates Dialog's proven and reliable DLNK technology to communicate from the secondary to the primary and also has a built-in optocoupler LED driver to minimize the bill of material cost.

The power supply designed with the iW657P is fully protected. Using over-voltage protection on the D+/D-/CC1/CC2 pins, the iW657P helps to address soft short issues in cables and connectors caused by poor or loose connections between the cable connector and the socket, contamination in the USB connector, or a worn out cable. Additionally, proprietary short circuit protection on the V_{BUS} NFET ensures safe operation in the event of a short on the output, while the SD pin can be used with an external NTC resistor for protection from over-temeperature faults. The iW657P also integrates a secondary-side current sensing circuit that provides additional over-current protection for the power adapter.

2 Features

- USB-IF PD certified: USB PD 3.0 + Programmable Power Supply (PPS)
  - » Maximum power limit in PPS to minimize power adapter size
  - » Integrated CC transmitter/receiver supports BMC communication
  - » Backwards-compatible with USB PD 2.0
- Supports Qualcomm Quick Charge 4+ Technology
- Supports up to 7 Power Data Objects (PDOs)
- Supports wide output voltage range from 3.3 to 21V
- Compatible with USB Type-C specification Rev 1.2 for MD attach/detach detection and V_{CONN} support for smart cables
- Integrated charge pump supports single NFET V_{BUS} switch
- 9-bit ADC provides accurate current (optional) and voltage sensing
- Proprietary V_{BUS} NFET protection to protect V_{BUS} switch from damage due to an output short circuit
- Proprietary secondary-to-primary digital communication eliminates discrete decoders on the primary side and simplifies system designs
- D+/D-/CC1/CC2 over-voltage protection (OVP) address soft short issues in the output cables and connectors
- Optional secondary-side current sensing circuit provides additional protection for over-load fault
- Uses external NTC for power adapter temperature sensing
- Programmable active fast discharge from a high voltage V_{BUS} level to 5V at MD unplug or upon request with built-in switch or external switch
- Intelligent circuits helps achieve < 20mW system no-load power at 5V steady-state operation.
- 14-pin 4x3mm TDFN package

3 Applications

- Rapid-charging AC/DC adapters for smart phones, tablets and other portable devices

Qualcomm® Quick Charge™ is a product of Qualcomm Technologies, Inc.

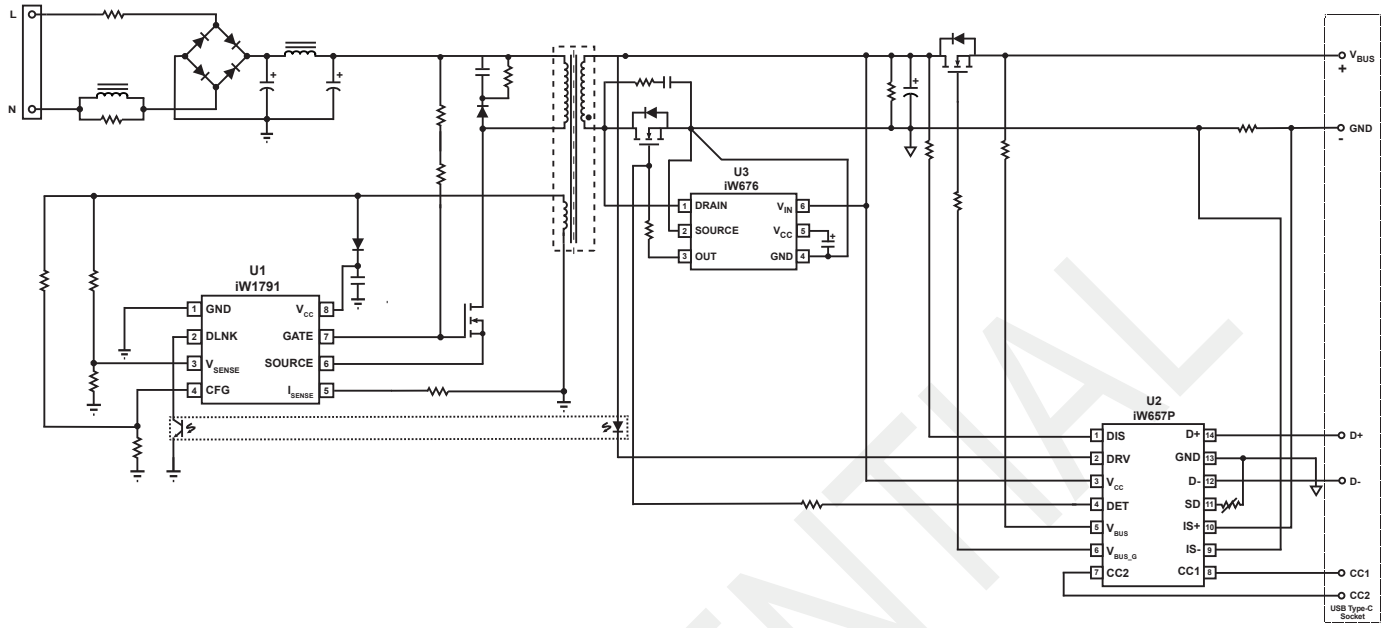


Figure 3.1 : iW657P Typical Application Circuit with Secondary-Side Current Sensing (with iW1791 as the Primary-Side Controller and the iW676 as the Synchronous Rectifier Controller)

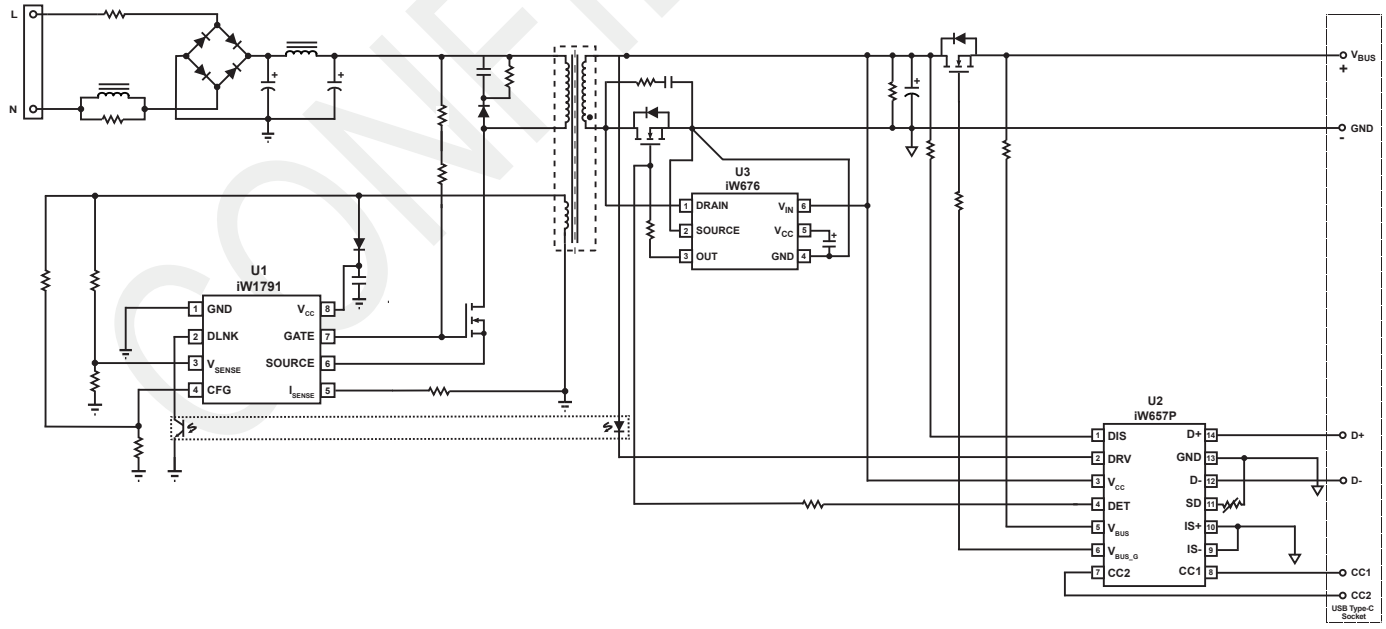


Figure 3.2 : iW657P Typical Application Circuit without Secondary-Side Current Sensing (with iW1791 as the Primary-Side Controller and the iW676 as the Synchronous Rectifier Controller)

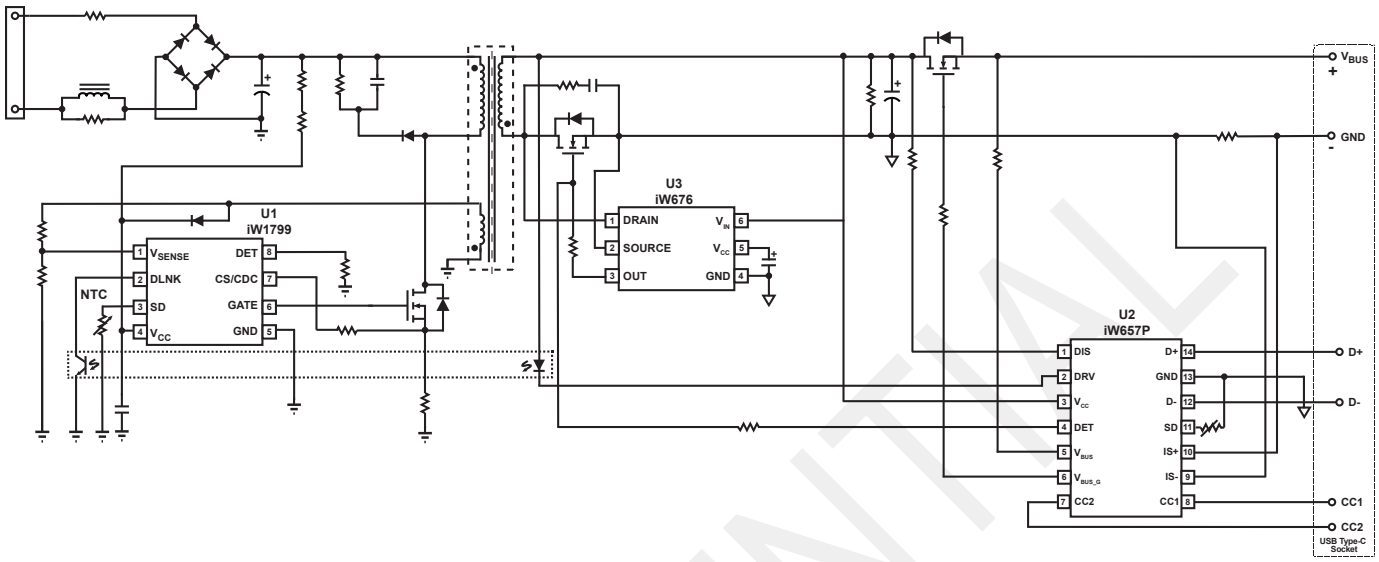


Figure 3.3 : iW657P Typical Application Circuit with Secondary-Side Current Sensing (with iW1799 as the Primary-Side Controller and the iW676 as the Synchronous Rectifier Controller)

4 Pinout Description

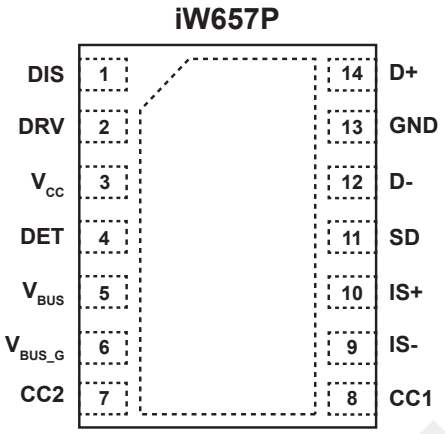


Figure 4.1 : 14-Lead TDFN 4x3mm Package
(Top View, Transparent)

Pin Number DFN-14	Pin Name	Type	Pin Description
1	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
2	DRV	Analog Output	External circuit drive. Can be used to drive optocoupler LED with automatic current limiting for transmitting signals to primary side.
3	V_{CC}	Power Supply	IC power supply.
4	DET	Analog Input	AC unplug detect.
5	V_{BUS}	Analog Input/ Output	Monitor V_{BUS} voltage after N-FET switch.
6	V_{BUS_G}	Analog Input/ Output	Connect to external N-FET gate pin for gate-source voltage control.
7	CC2	Analog Input/ Output	Configuration Channel 2.
8	CC1	Analog Input/ Output	Configuration Channel 1.
9	IS-	Analog Input	Output current sensing terminal - (for current sensing resistor).
10	IS+	Analog Input	Output current sensing terminal + (for current sensing resistor).
11	SD	Analog Input/ Output	Connect to an external NTC resistor to measure the power adapter temperature.
12	D-	Analog Input/ Output	USB D- signal.
13	GND	Ground	Ground.
14	D+	Analog Input/ Output	USB D+ signal.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded.

Parameter	Symbol	Value	Units
V_{CC} voltage	V_{CC}	-0.3 to 30	V
DIS voltage	V_{DIS}	-0.3 to 30	V
DRV voltage	V_{DRV}	-0.3 to 30	V
V_{SD} voltage	V_{SD}	-0.3 to 7	V
D- voltage	V_{D-}	-0.3 to 7	V
D+ voltage	V_{D+}	-0.3 to 7	V
CC1 voltage	V_{CC1}	-0.3 to 30	V
CC2 voltage	V_{CC2}	-0.3 to 30	V
V_{BUS} voltage (I_{VBUS} < 10mA)	V_{BUS}	-0.7 to 30	V
V_{BUS_G} voltage	V_{BUS_G}	-0.7 to 35	V
DET voltage	V_{DET}	-0.7 to 30	V
Peak current at DIS pin (V_{DIS}= 12V)	I_{DIS}	600	mA
IS+ voltage	V_{IS+}	-0.3 to 7	V
IS- voltage	V_{IS-}	-0.3 to 7	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
ESD rating per JEDEC JESD22-A114 (D+, D-, CC1, CC2)		±8,000	V
ESD rating per JEDEC JESD22-A114 (all other pins)		±2,000	V

Notes:

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Electrical Characteristics

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} SECTION						
Standby current	I_{CC}	V_{CC} = 5V, Bus switch off	300	350	450	µA
Operating voltage (Note 1)	V_{CC}		2.6		25	V
Startup threshold (Note 1)	$V_{CC(ST)}$			3.3		V
Undervoltage lockout threshold (Note 1)	V_{CC_UVLO}			2.6		V
Fast discharge threshold (Note 1)	V_{CC_DIS}		+7.3	+10	+12.7	%
Under-voltage threshold	$V_{CC(UV)}$	V_{CC} ≥ 4V	-6.2	-5	-3.8	%
		V_{CC} < 4V		-6		%
Over-voltage threshold	$V_{CC(OV)}$	V_{CC} ≤ 20V	+19	+22	+26	%
		20V < V_{CC} ≤ 21V	23.8	24.4	25.2	V
DIS SECTION						
Fast discharge current	I_{DIS_FAST}	On state			500	mA
Slow discharge current	I_{DIS_SLOW}	V_{CC} = 3.0V - 4.5V		70		mA
		V_{CC} = 4.5V - 7V		52.5		mA
		V_{CC} = 7V - 16V	22.9	35	42.3	mA
		V_{CC} > 16V	12.5	17.5	22.1	mA
DRV SECTION						
Sink current	I_{DRV}	On state	2	2.5	3	mA
V_{BUS} SECTION						
V_{BUS} discharge resistor	R_{VBUS_DIS}		7	10	13	kΩ
V_{BUS} leakge impedance (Note 1)	R_{VBUS_LKG}	V_{BUS} switch off	72.4			kΩ
V_{BUS} attach/detach detection threshold	V_{SAFE_0V}		0.4	0.6	0.8	V
V_{BUS} output short detection threshold (after turn-on)	V_{OSP}			360		mV
V_{BUS_G} SECTION						
V_{BUS_G} to V_{BUS} regulation range	V_{GS}	V_{CC} ≥ 5V	6.2	6.9	7.6	V
V_{BUS_G} to V_{BUS} resistor	R_{GS}		1200	2000	2800	kΩ
V_{BUS_G} drive current	I_G		200			µA
OTP SECTION						
Minimum SD pin sourcing current	I_{SD_MIN}		4.4	5	5.9	µA
Maximum SD pin sourcing current	I_{SD_MAX}		94	100	109	µA

6 Electrical Characteristics (Cont.)

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SD pin NTC temperature - turn-off for V_{BUS} switch, shutdown TA	T_{SD_OTP}	24 - 151°C Configured by Manufacturer (Note 3)		120		°C
SD pin NTC temperature - turn-on for V_{BUS} switch	T_{SD_ST}	T_{SD_OTP} - 10°C		110		°C
IC junction temperature threshold to turn on V_{BUS} switch	T_{J_ST}			130		°C
IC junction temperature threshold to turn off V_{BUS} switch and shutdown TA	T_{J_OTP}			140		°C
D+/D- SECTION						
Data detect voltage	V_{DAT_REF}		0.3	0.35	0.4	V
V_{OUT} selection reference	V_{SEL_REF}		1.8	2	2.2	V
Data line leakage on D+	$R_{DAT\_LKG\ D+}$			1000		kΩ
D+ to D- resistance	R_{DCP_DAT}	D+ = D- = 0.6V			40	Ω
D- pull-down resistance	R_{DM_DWM}		14.25	18	24.8	kΩ
D+ OVP threshold	V_{DP_OVP}		4.15	4.5	4.73	V
D- OVP threshold	V_{DM_OVP}		4.15	4.5	4.73	V
CC1/CC2 SECTION						
CC1 sourcing current (Note 2)	I_{CC1}	Default current limit 2A	165	180	195	µA
		Default current limit 3A	300	330	360	
CC2 sourcing current (Note 2)	I_{CC2}	Default current limit 2A	165	180	195	µA
		Default current limit 3A	300	330	360	
MD pull-down resistor R_D detect threshold	V_{TH_RD}		2.6	2.9	3.2	V
Cable pull-down resistor R_A detect threshold	V_{TH_RA}		0.45	0.5	0.55	V
CC1 pull-up resistor (detach state)	R_{CC1_DETACH}			56		kΩ
CC1 OVP threshold	V_{CC1_OVP}		6.5	6.8	7.25	V
CC2 OVP threshold	V_{CC2_OVP}		6.5	6.8	7.25	V
BMC signal logic high voltage	$V_{CC\_TX\_HIGH}$		1.050	1.125	1.200	V
BMC signal logic low voltage	$V_{CC\_TX\_LOW}$		-75		75	mV
BMC receiver comparator threshold(rising/ falling)	$V_{TH\_CC\_RX}$	Rising	0.64	0.725	0.86	V
		Falling	0.505	0.575	0.675	
BMC signal bit rate	f_{BMC}		270	300	330	kbps
BMC transmitter output impedance	Z_{DRIVER}		33		75	Ω

6 Electrical Characteristics (Cont.)

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CONN} SECTION						
V_{CONN} voltage			3		5.5	V
V_{CONN} current	I_{VCONN}	V_{CONN} = 3V	33			mA
V_{CONN} discharge resistor	R_{DIS_VCONN}			2.6		kΩ
DET SECTION						
DET comparator threshold	V_{TH_DET}		0.68	0.8	0.91	V
Primary side off timer	T_{DET_OFF}		36	40	44	ms
PD/QC MODE TIMMING						
Time from attach MD to V_{BUS} reach 5V (Note 1)	T_{BUS_ON}		0		275	ms
Time from detach MD to V_{BUS} below V_{SAFE_0V} (Note 1)	T_{BUS_OFF}		0		650	ms
Voltage change glitch filter time (Note 1)	$T_{GLITCH\_\Delta V}$			40		ms
New voltage request interval (Note 1)	$T_{V\_NEW\_REQUEST}$		200			ms
ADC SECTION						
V_{BUS} sensing range	V_{BUS_RANGE}		3		26	V
V_{BUS} sensing tolerance	V_{BUS_TOL}	V_{BUS} = 3.3-21V (Note 1)			2	%
I_{BUS} sensing range	I_{BUS_RANGE}	R_{SENSE} = 5mΩ	0		6.5	A
I_{BUS} sensing tolerance	I_{BUS_TOL}	Load current is DC 1-3A (Note 1)	-100		100	mA
Junction temperature range	T_{J_RANGE}		0		165	°C
Junction temperature tolerance	T_{J_TOL}		-10		10	°C
SD NTC tolerance	T_{NTC_TOL}	T_{NTC} ≥ 70°C	-5		5	°C

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 2: Value used depends upon specific product option

Note 3: Parameter can be configured by manufacturer. Please contact Dialog for NTC selection and OTP threshold information.

7 Typical Performance Characteristics

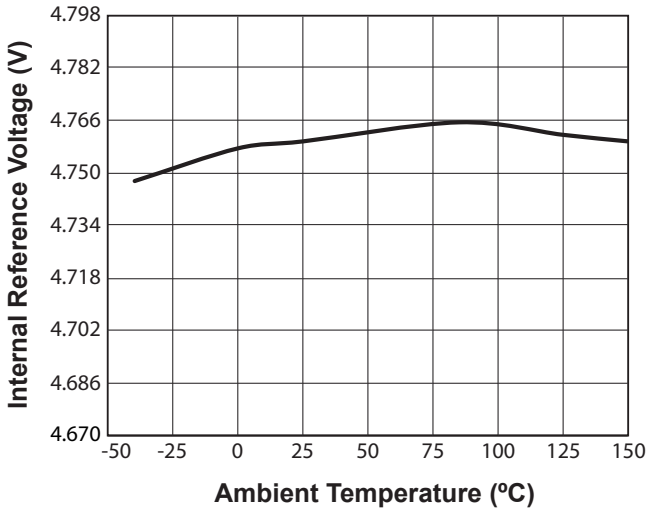


Figure 7.1 : Internal Reference Voltage vs Ambient Temperature

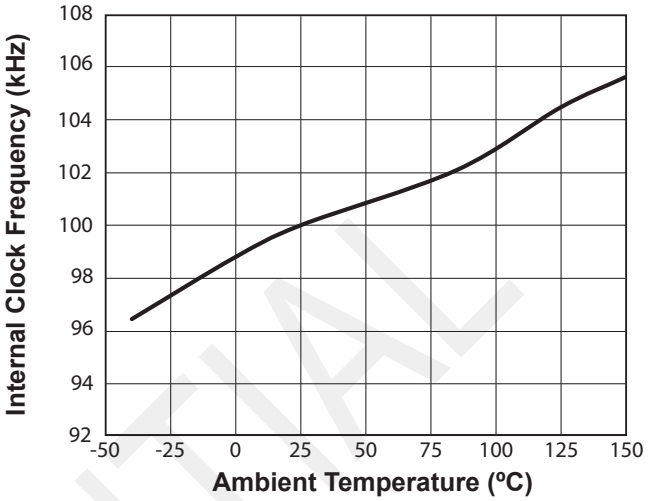


Figure 7.2 : Internal Clock Frequency vs. Ambient Temperature

8 Functional Block Diagram

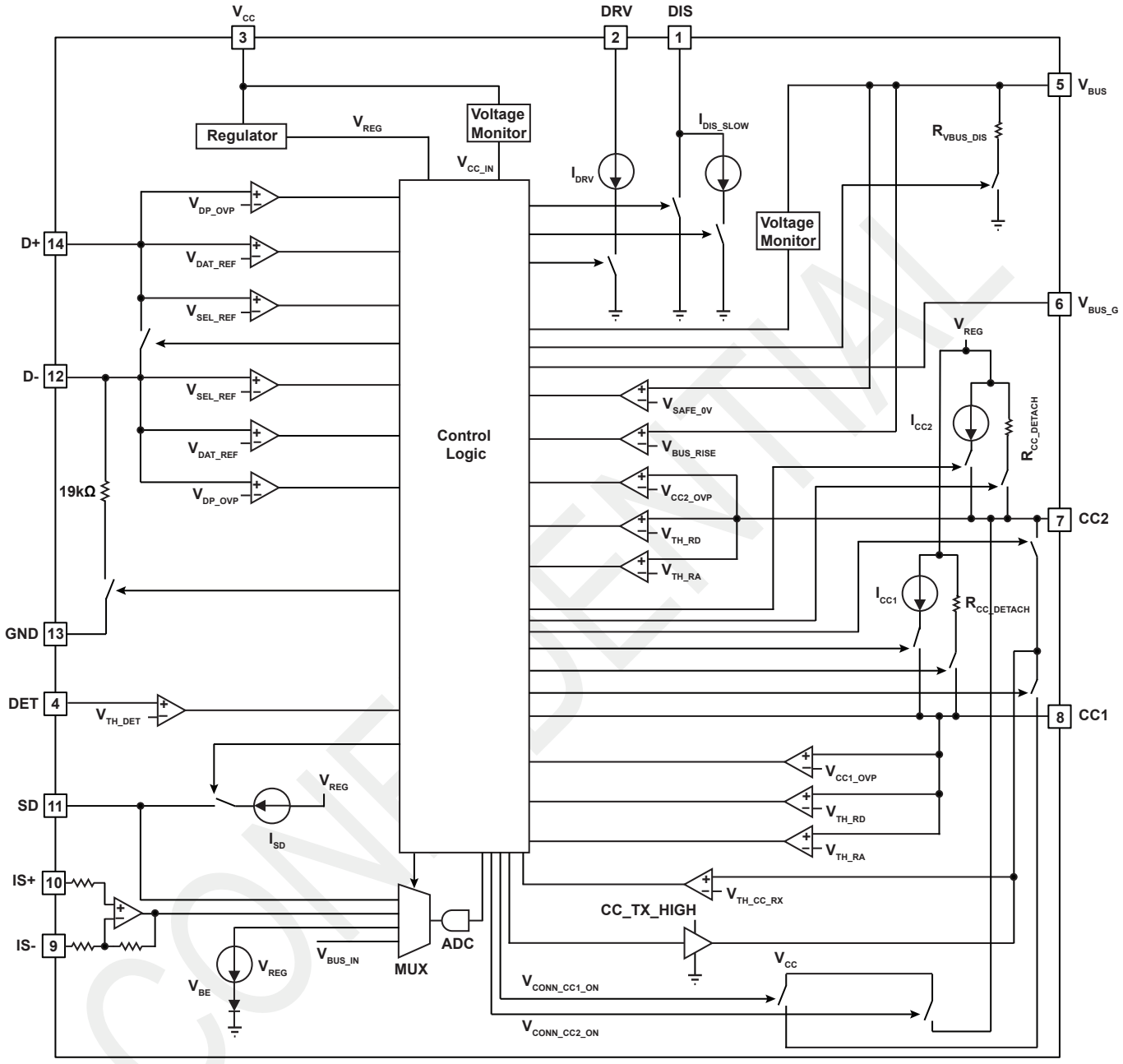


Figure 8.1 : iW657P Functional Block Diagram

9 Theory of Operation

The iW657P is an AC/DC secondary-side controller for USB Type-C™ enabled travel adapters (TA) with USB PD 3.0 and Qualcomm® Quick Charge™ 4+ (USB PD3.0/QC4+) protocol support. This device integrates secondary-to-primary communication interfacing to allow Mobile Devices (MD) equipped with USB PD3.0/QC4+ technology to request the adapter output voltage/current configuration to multiple output levels for fast charging or direct charging. The iW657P supports Programmable Power Supply (PPS) Augmented Power Data Object (APDO) and related messages. With an internal 9-bit ADC, the iW657P can accurately measure V_{BUS}, I_{BUS}, and the TA temperature and provide this information to the MD through PD3.0 messages. The iW657P also supports V_{CONN} and Electronic Marked Cable current reading, which enables iW657P to limit its PDO current not higher than the cable current rating. The iW657P is backward compatible with PD2.0.

The iW657P is also backwards compatible with USB BC1.2 compliant MDs and other MDs to provide 5V output voltage by its default setting. The iW657P can be detected as a dedicated charging port (DCP) if an MD is connected. After the initial handshaking stage, the iW657P interprets the CC1/CC2 signal and D+/D- signals to determine USB PD3.0/QC4+ mode and its associated output voltage/current requests. A valid request is encoded to certain pulse patterns and sent to the primary side through an optocoupler.

Besides the voltage and current information, the iW657P also monitors the adapter output voltage and sends over-voltage or under-voltage information to the primary side through the same optocoupler using Dialog's proprietary secondary-side to primary-side digital communication protocol. The optocoupler is driven by a current source (I_{DRV}) for stable signal transmission independent of output voltage. The iW657P should be paired with one of Dialog's primary-side controller, either the iW1791 or iW1799, for dynamic multi-level voltage and current configuration and control. The primary-side controllers have a built-in circuit to decode the different pulse patterns for voltage configuration, current limit setting, V_{OUT} under-voltage and over-voltage detection, and the primary-side controller responds according to the decoded information. The iW657P also features a programmable fast/slow active discharging function to discharge the output capacitor in a short time after a request for a lower voltage or upon detection of an unplug event of the MD.

9.1 Pin Detail

Pin 1 – DIS

Programmable active discharge. This pin provides fast and slow discharge paths for the external circuit, such as an output capacitor. It can also drive an external P-channel FET. When there is a request for a lower voltage or the USB MD is unplugged at a high voltage, the internal active discharge switches are turned on.

Pin 2 – DRV

External circuit drive. This pin drives the external circuit, such as the optocoupler, to send out all the information for rapid charge. The DRV pin sink current at the ON state is limited to a range such that a low-cost optocoupler can be used.

Pin 3 – V_{CC}

IC power supply. This pin provides the IC supply voltage.

Pin 4 – DET

AC unplug detect.

Pin 5 – V_{BUS}

Monitor V_{BUS} voltage. Used for V_{BUS} switch control and output short circuit protection.

Pin 6 – V_{BUS_G}

Connect to external N-FET gate pin for gate-source voltage control.

Pin 7 – CC2

USB Type-C configuration channel pin 2. Used for MD attach/detach detection and PD communication.

Pin 8 – CC1

USB Type-C configuration channel pin 1. Used for MD attach/detach detection and PD communication.

Pin 9 – IS-

Output current sensing resistor negative terminal input. See figure 3.1.

Pin 10 – IS+

Output current sensing resistor positive terminal input. See figure 3.1.

Pin 11 – SD

Shutdown Pin. Used to measure the travel adapter temperature and implement thermal protection when connected to an external NTC resistor.

Pin 12 – D-

USB D- signal. Used for QC2.0/3.0 signal.

Pin 13 – GND

Ground

Pin 14 – D+

USB D+ signal. Used for QC2.0/3.0 signal and MD reset/unplug detection.

9.2 CC1/CC2 Attach/Detach Detection and V_{BUS} Control

The V_{BUS} switch is off initially upon travel adapter (TA) power up. After the output voltage (and V_{CC} of iW657P) of the TA reaches $V_{CC(ST)}$, CC1 and CC2 are connected to a voltage source, V_{REG} (about 4.5V), through two 56kΩ resistors (R_{CC1_DETACH}). The CC1 and CC2 voltages are compared with V_{TH_RD} to detect if the mobile device (MD) or cable is attached. The MD or cable attach will cause the CC1 and/or CC2 voltage to be lower than V_{TH_RD}. Once the MD and/or cable attach is detected, the iW657P will apply I_{CC1} and I_{CC2} on CC1 and CC2 simultaneously to determine if CC1 and CC2 are connected to R_D (5.1kΩ to GND inside MD) or R_A (1kΩ to GND inside cable) by comparing CC1/CC2 voltage with V_{TH_RD} and V_{TH_RA}. The V_{BUS} switch will turn on after 150ms if the following three conditions are met:

1) V_{BUS} is less than V_{SAFE_0V}

2) V_{CC} is 5V

3) Only one of CC1 and CC2 connects to R_D and the other one connects to R_A or open

After the V_{BUS} switch turns on, the iW657P determines which of the two currents, I_{CC1} or I_{CC2} that was previously applied to CC1 and CC2 respectively, was connected to R_A (or open) and will turn off that current source. The remaining I_{CC1}/ I_{CC2} current will only apply to the CC pin that connects with R_D so that it can detect when the MD detaches. If the MD is detached, the CC1 or CC2 voltage originally connected with R_D will be higher than V_{TH_RD} to indicate the MD is detached. The V_{BUS} switch will thus turn off and V_{BUS} will be discharged through R_{VBUS_DIS} if $V_{BUS}>V_{SAFE\_0V}$. R_{VBUS_DIS} will disconnect after $V_{BUS}<V_{SAFE\_0V}$ or the connect time exceeds 650ms.

At this point, the iW1791/iW1799 and iW657P will change the output voltage (and V_{CC} of the iW657P) to the default 5V level if it is not already 5V. The current limit will be set to the default level per product options. Two 56kΩ resistors (R_{CC_DETACH}) will be reconnected to CC1/CC2 from V_{REG} to start a new attach detection cycle.

9.3 Initialization and Handshaking

An AC/DC power adapter designed with the iW1791/iW1799 and the iW657P starts up initially at its default 5V output voltage setting. When the TA is connected to the MD and V_{BUS} switch is on, the iW657P begins the protocol detection

procedure. The iW657P sends out USB PD Source_Capabilities messages via the CC pin (either CC1 or CC2, whichever pin is connected to R_D) and waits for the MD's response in order to make a PD explicit contract. While waiting for a response, the iW657P starts the BC1.2 detection procedure through the D+/D- pins followed by the QC2.0/QC3.0 detection procedure, also through the D+/D- pins. If the PD protocol is detected first, the QC2.0/QC3.0 protocol is disabled and PD is used until detach. If the QC2.0/QC3.0 protocol is detected first, the iW657P will enter QC2.0/QC3.0 mode and meanwhile continue to send Source_Capabilities and wait for a response from the MD. If PD is not detected after about 7.5 seconds, the iW657P will stop sending Source_Capabilities and stay in QC2.0/QC3.0 mode. If the MD responds and makes a PD explicit contract, the iW657P will exit QC2.0/QC3.0 mode and stay in PD mode until detach. If neither PD nor QC are detected after 7.5 seconds, the TA will disable PD detection and remain in QC detection mode. While the TA is in QC2.0/QC3.0 mode or QC2.0/QC3.0 detection mode, if a PD Hard Reset message is received, the iW657P will disable the V_{BUS} switch for 0.85 seconds and enable the V_{BUS} switch again at the default output voltage of 5V and default current and start the PD and QC2.0/QC3.0 detection procedure again as described previously. Figure 9.1 shows the flowchart for the attach and detection sequence for a travel adapter using the iW657P.

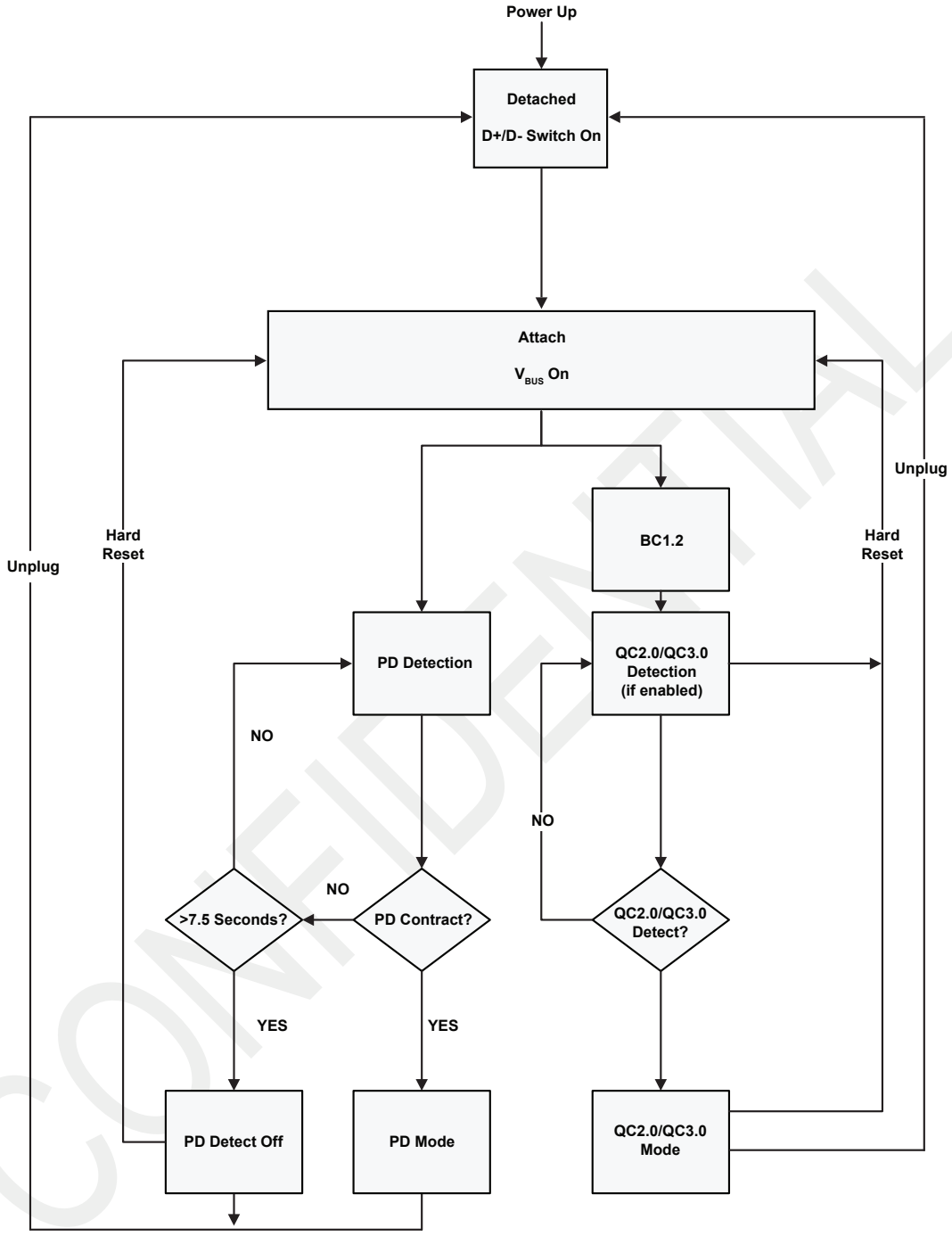


Figure 9.1 : Attach and Detection Flowchart for BC1.2, USB PD 2.0/3.0 and QC2.0/3.0.

9.4 PD Mode Operation

The iW657P integrates a USB PD Biphase Mark Coding (BMC) signal transmitter/receiver and can communicate with the MD directly through the CC1/CC2 pin. It supports both PD2.0 and PD3.0 protocol. The iW657P uses the PD3.0 protocol if the MD is equipped with PD3.0. It will automatically change to use PD2.0 protocol if the MD connected only supports the PD2.0 protocol. The iW657P supports up to 7 Power Data Objects (PDOs). The power negotiation

process starts with the iW657P sending it's Source_Capabilities with all the PDOs it supports. The MD evaluates the received PDOs and requests one of the PDOs. If the request is valid, the iW657P will send a signal to the primary side to change the output voltage and output current limit to the requested value. The iW657P has a built-in encoder to generate the different pulse patterns and to drive the internal switch of the DRV pin so that the voltage information together with the associated current limit setting can be sent to the primary side through an optocoupler. The iW657P will inform the MD when the TA's voltage and current reach the requested level.

The iW657P also supports direct charge (V_{BUS} connects to the MD battery through a switch instead of through a buck converter) operation with the MD through Programmable Power Supply (PPS) Augmented Power Data Objects (APDO). The MD can make a contract with the iW657P at the APDO through standard power negotiation process. When the MD and TA are contracted with APDO, the MD can request any voltage within the APDO voltage range in 20mV steps. The MD can also request any TA output current within the APDO current range in 50mA steps. The internal ADC of the iW657P measures V_{BUS}, I_{BUS}, and TA temperature. This information is saved in the iW657P's internal registers and can be read by the MD through PD PPS_Status and Status messages. The iW657P also integrates a proprietary AC unplug detection function for direct charge. The DET pin connects to the secondary SR MOSFET gate or drain pin, allowing the flyback converter switching to be detected by the iW657P. When AC is unplugged, the flyback and SR controller converter will stop switching. Once the iW657P fails to detect a switching waveform for more than T_{DET_OFF}, the iW657P will turn off the V_{BUS} switch and remove CC1/CC2 pin current so the MD can exit direct charge mode. It can prevent V_{BUS} from going to 5V after AC unplug and plug in again immediately when V_{BUS} is still connected directly to the MD's battery.

Besides standard USB PD messages, the iW657P also supports Vendor Defined Messages (VDM). Please contact Dialog for detailed VDM information.

The primary side current sensing resistor R_S is calculated by

$$R_S = \frac{0.4 \times k_{CC}@I_{DEFAULT} \times N_{PS}}{I_{DEFAULT}} \times \eta_X \qquad (9.1)$$

N_{PS} is flyback converter transformer primary winding to secondary winding turns ratio. η_X is the transformer conversion efficiency and $I_{DEFAULT}$ is the default TA current setting (typically 3A). The $k_{CC}@I_{DEFAULT}$ term is set by the iW657P.

Some of the USB PD features are not supported by iW657P:

- USB Type-C Alternate mode
- USB Type-C Audio Adapter and Debug Accessary mode
- USB PD BFSK communication through V_{BUS}
- USB PD Dynamic Power Capability
- USB PD Peak Current Operation
- USB PD Power Role Swap and Fast role Swap

9.5 V_{CONN} Support and Cable Reading

The USB PD specification supports TA current up to 5A. However, standard USB Type-C™ cables have a maximum current rating of 3A. If the TA has a PDO/APDO current higher than 3A, it needs to ensure that the cable used has a current rating higher than 3A. USB PD requires use of either a captive cable or an Electronically Marked Cable for > 3A applications. The iW657P provides an optional V_{CONN} and cable reading feature to work with EMC. When this feature is enabled, after cable plug in is detected and the TA turns on the output voltage to 5V, the iW657P will connect the V_{CONN} terminal (the CC1 or CC2 terminal that is not used as PD communication channel) to V_{CC}, which is set to 5V. The V_{CONN} voltage source provides the external power supply to the EMC internal circuit. After the V_{CONN} voltage turns on for 60ms, the iW657P will send a PD Discover_Identity message to the EMC to read the EMC current rating.

The iW657P will turn off the internal V_{CONN} switch and start sending out Source_Capabilities after the cable reading. If no response from the cable is received or the cable current rating is 3A, the iW657P will limit its PDO current to 3A maximum. The iW657P will turn on V_{CONN} and cable reading again after plug-in and Hard Reset.

9.6 QC Mode Operation

After initialization and handshaking with the MD, if there is a D+/D- combination change and the D+/D- voltage combination is a valid QC2.0/3.0 request and passes the 40ms deglitch filter, the iW657P enters QC2.0/3.0 mode.

The iW657P interprets the D+/D- combination according to the QC2.0/3.0 specification. The interpretation of the D+/D-combination and voltage requests are listed in Table 9.1.

Please note that a voltage at D+ or D- is detected as:

a) 0V, if it is lower than V_{DAT_REF};

b) 0.6V, if it is between V_{DAT_REF} and V_{SEL_REF};

c) 3.3V, if it is higher than V_{SEL_REF}.

D+	D-	V_{OUT}
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	Enters continuous mode
0.6V	0V	5V
All other combinations		Stays unchanged

Table 9.1: D+/D- Signals and Adapter V_{OUT} (aka V_{BUS}, V_{CC})

The iW657P has a built-in encoder to generate different pulse patterns and to drive the internal switch of the DRV pin so that the voltage information together with the associated current limit setting can be sent to the primary side through an optocoupler.

9.7 Programmable Active Discharge

Discharge of the output capacitor is necessary for a quick voltage transition from a higher level to a lower level when a lower voltage is requested. An internal switch between the DIS pin and GND pin is turned on to provide a current path from the output voltage through an external resistor to ground. The discharging time is programmable with the external resistor. A resistance of 47Ω or higher is recommended for the external resistor to prevent over-current or over-heating inside the IC.

If the application uses a larger output capacitor or requires faster discharging, an external P-channel FET can be used and the iW657P DIS pin can be used to drive the FET. When the MD is unplugged, the iW657P resets to its initial setting. The active fast discharge starts after a confirmed lower voltage request or after the 40ms de-glitch of the D+ voltage drop; it stops when the active discharge threshold of the target voltage is reached or a 200ms timer (including de-glitch time) expires to avoid excess load current and high power dissipation inside the IC. After the active fast discharge stops, a slow discharge path continues to discharge the output capacitor until the 200ms timer expires.

9.8 V_{BUS} Monitoring

In addition to encoding and transmitting the output voltage and current request, the iW657P monitors V_{BUS} for both under-voltage and over-voltage. The V_{BUS} under-voltage, or voltage undershoot, is usually caused by a sudden load current increase. The iW657P also monitors the V_{BUS} over-voltage, especially the over-voltage caused by a potential output voltage setting mismatch between the iW1791/iW1799 and the iW657P.

When a load transient event from light load to heavy load occurs, the output voltage droops. If the output voltage droops to the voltage undershoot threshold, the iW657P turns on the LED of the optocoupler by controlling the DRV pin sink current, and the DLNK pin of the iW1791/iW1799 is pulled down by the transistor of the optocoupler. After the primary-side controller receives this DLNK pin signal, it can intelligently confirm if this signal is caused by an undershoot event and distinguish it from a voltage and current request, and then it promptly increases the switching frequency and t_{ON} to deliver more power to the secondary in order to bring the output voltage back into regulation. The undershoot detection signal of the iW657P is backward compatible with Dialog's secondary-side voltage position monitor, the iW628.

While the iW1791/iW1799 can protect against V_{BUS} over-voltage through the V_{SENSE} signal in most condtions, it is difficult for the iW1791/iW1799 to protect against over-voltage caused by output voltage setting mismatch between the primary-side controller and the iW657P. Therefore, the iW657P, iW1791/iW657P or iW1799/iW657P chipset adds one more layer of OVP. When V_{BUS} rises above the over-voltage threshold of the iW657P's present setting, the iW657P drives the DRV pin in a special switching pattern serving as an OVP signal and turns on both the fast and slow discharge. After the iW1791/iW1799 receives this OVP signal, it shuts down the power supply promptly.

Therefore, the iW657P uses proprietary digital communication to transmit to the primary-side controller all the necessary information for a high-performance rapid-charge AC/DC system design including output voltage requests, output current limits, output voltage undershoot and output over-voltage all via a single optocoupler.

9.9 Internal and External OTP

The iW657P has two sources for over temperature protection (OTP). One is from the IC's internal junction temperature. The other is from an external NTC resistor connected to the SD pin. The SD pin can provide an external OTP function when an NTC resistor is connected between SD and GND. An internal I_{SD} current flows though the NTC resistor and the voltage V_{SD} on the SD pin is measured by the internal ADC. To reduce power loss, the iW657P sends a 650µs current pulse every 20ms. To ensure that V_{SD} is within the ADC effective sensing range (about 1.23V) with wide NTC resistor value variation, the iW657P sends out the highest current (100µA) first and reduces to the next lower current level (40µA, 20µA, 5µA) until V_{SD} is less than 1.23V. The iW657P determines the NTC resistor R_{SD} value by calculating V_{SD}/I_{SD}. The NTC temperature T_{SD} is calculated by:

$$T_{SD} = \frac{1}{\left[\frac{1}{298.15} + \frac{1}{B} \times ln\left(\frac{R_{SD}}{R25}\right)\right]} \qquad (9.2)$$

B is material factor and R25 is the resistance of the NTC device at 25°C temperature. The iW657P monitors the NTC temperature before turn-on of the V_{BUS} switch. The V_{BUS} switch will not turn on if the NTC temperature is higher than T_{SD_ST}. After V_{BUS} turns on, the iW657P will compare the NTC temperature with T_{SD_OTP}. If the NTC temperature is higher than T_{SD_OTP}, the iW657P will turn off the V_{BUS} switch and send a fault signal through DLNK to the primary-side controller to shut down the power converter. The B value, R25 and T_{SD_OTP} are factory programmed. Please contact Dialog for other NTC and T_{SD_OTP} configurations.

The iW657P monitors the IC's junction temperature after cable plug in and compares it with T_{J_ST} before the V_{BUS} switch is enabled and T_{J_OTP} after the V_{BUS} switch is on. The V_{BUS} switch will not turn on if the IC junction temperature is higher than T_{J_ST}. After the V_{BUS} switch turns on, if the IC junction temperature is higher than T_{J_OTP}, the iW657P will turn off the V_{BUS} switch and send a fault signal through DLNK to the primary-side controller to shut down the power converter. The iW657P does not monitor the IC junction temperature if unplugged.

The iW657P will send out a PD Alert message if the NTC temperature increases to within 5°C of the T_{SD_OTP} threshold, or if the IC junction temperature (T_J) increases to within 5°C of the T_{J_OTP} threshold. This allows the MD to reduce its power consumption and avoid the TA from entering over-temperature protection (OTP).

9.10 V_{BUS} Switch Output Short Protection

After the MD is attached to a Type-C connector, the iW657P will turn on the V_{BUS} NFET switch after 150ms. If the V_{BUS} switch turns on into an output short, the output capacitor discharge current may exceed the NFET's maximum current limit and damage the NFET. The iW657P implements a soft-start scheme to ensure the output current rises slowly while the output capacitor discharges. The output short is detected when V_{BUS} discharges below a threshold (V_{CC_LOW}) lower than the normal V_{OUT} minimum voltage at full load. The iW657P will turn-off the V_{BUS} switch immediately to limit the output current. The iW657P will initiate the V_{BUS} switch soft-start and turn-off process every 2s if output short persists.

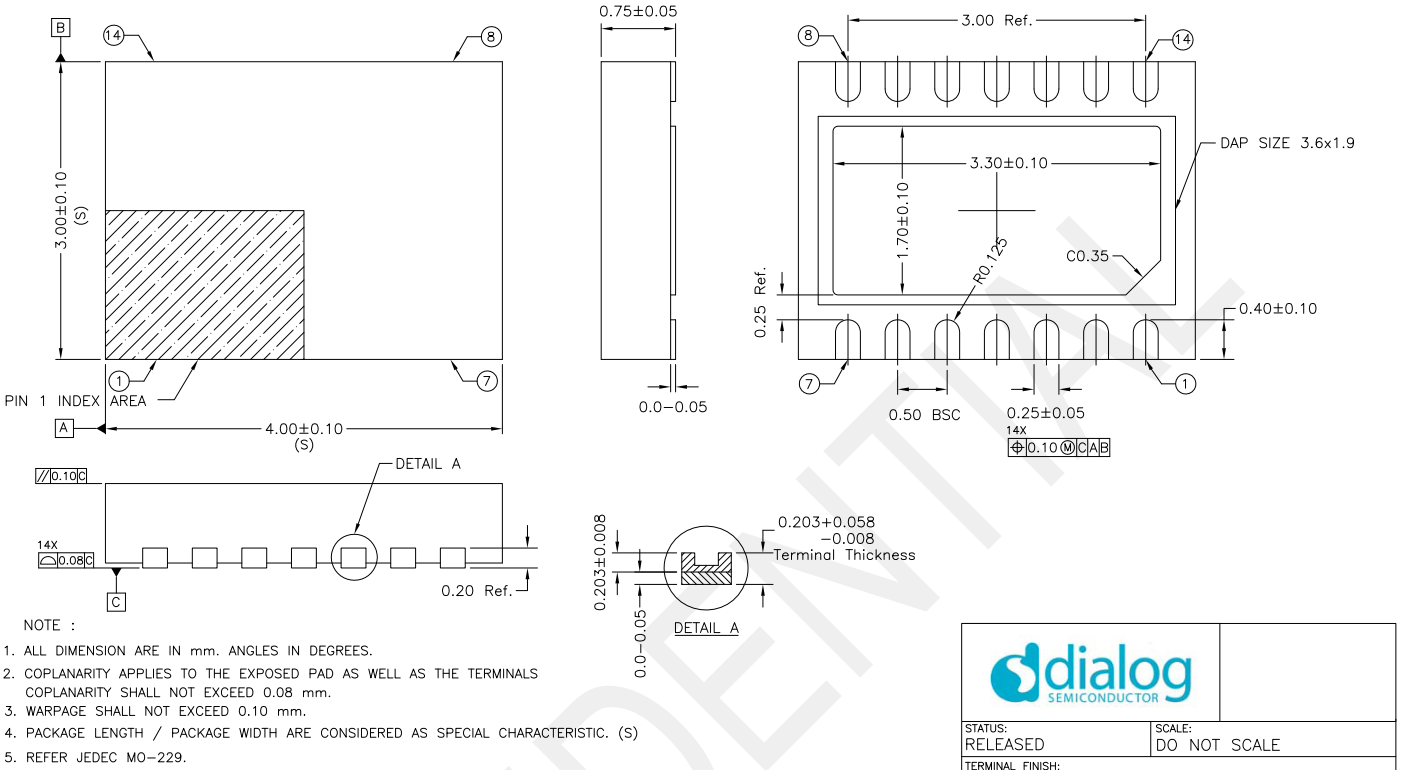
During normal operation when the MD is connected and the V_{BUS} switch is fully on, the voltage drop across V_{CC} and V_{BUS} (V_{BUS} switch $R_{DS(ON)}$ IR drop) is monitored and compared with V_{OSP}. An output short during normal operation will cause V_{CC} - V_{BUS} > V_{OSP} and iW657P will turn-off the V_{BUS} switch immediately. The iW657P will initiate the V_{BUS} switch soft-start and turn-off process every 2s if the output short persists.

9.11 Output Cable Soft Short Detection

The iW657P features D+/D- overvoltage protection (OVP), which addresses soft short issues in the output cables and connectors and provides protection against damages. If the voltage on the D+ or D- pin is above 4.5V, the D+/D- OVP fault is triggered. The CC1 and CC2 voltages are also monitored after IC power up. If the voltage on the CC1 or CC2 pin is above 6.8V, the CC1/CC2 OVP fault is triggered.

When the iW657P detects a D+/D-/CC1/CC2 OVP the V_{BUS} switch and the CC1/CC2 current source are disabled. Then the iW657P will wait for 2 seconds to restart attach detection after no fault is detected.

10 Physical Dimensions



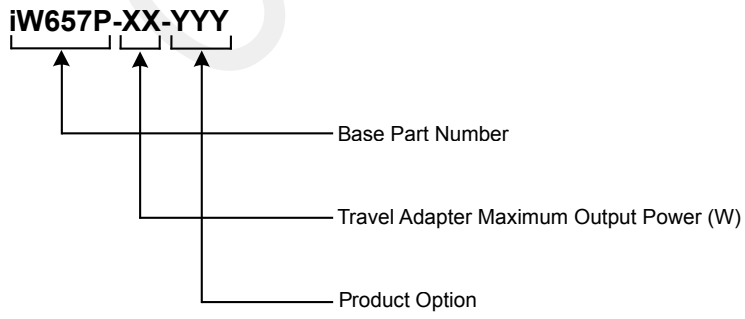
NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO−229.

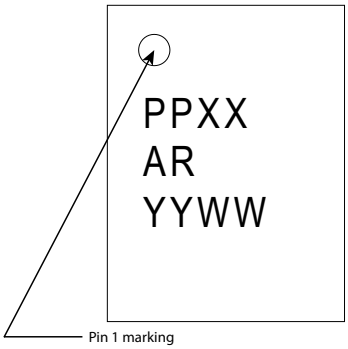
STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: NiPdAu (PPF)	
TITLE: 14 TDFN 4x3mm PACKAGE OUTLINE	
REV: B	REVISION NOTE: TERMINAL FINISH UPDATED — DATE: 26−MAY−2017

Figure 10.1 : 14-Lead TDFN 4x3mm Package

11 Part Number Code Description



12 Top Marking



PP:	Product Option Code: Alphanumeric (unique)
XX:	Lot Identification Code: Numeric or Alphanumeric (unique)
A:	Assembly Location Code
R:	Product Revision
YY:	Year
WW:	Work Week

Note 1: Font size and text alignment may vary by assembly supplier.

Figure 12.1 : Top Marking for iW657P

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