

### Description

The BP0405SCG uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs can be used in a wide variety of applications.



### Features

- N-Channel  
 $V_{DS}=40V, I_D=6A$   
 $R_{DS(ON)} < 26m\Omega @ V_{GS}=10V$
- P-Channel  
 $V_{DS}=-40V, I_D=-5A$   
 $R_{DS(ON)} < 60m\Omega @ V_{GS}=-10V$
- High power and current handling capability

### Applications

- H-bridge
- Inverters

### Typical Application

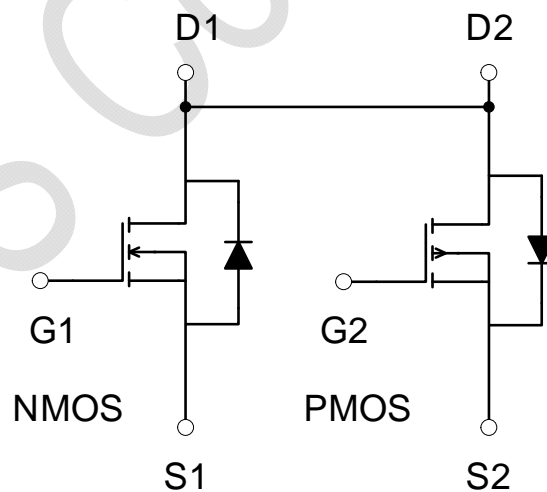


Figure 1. Schematic Diagram

### Ordering Information

Part Number	Package	Package Method	Marking
BP0405SCG	ESOP8	Tape 4,000 pcs/Reel	BP0405 XXXXXXSC XXWWG

### Pin Configuration and Marking Information

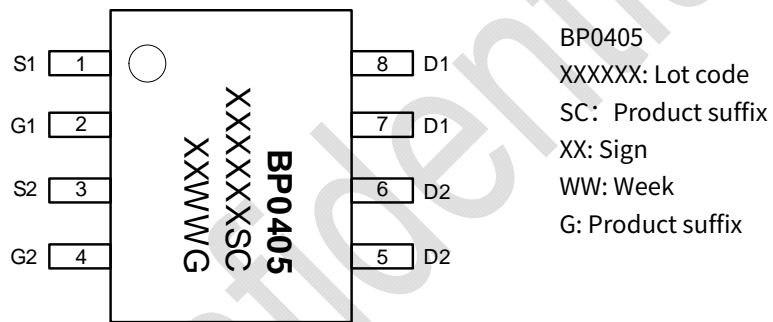


Figure2 : Pin configuration

### Pin Definition

Pin No.	Name	Description
1	S1	NMOS Source
2	G1	NMOS Gate
3	S2	PMOS Source
4	G2	PMOS Gate
5、6	D2	PMOS Drain
7、8	D1	NMOS Drain

**Absolute Maximum Ratings** (Note 1)

Symbol	Parameters		Range		Units
			N-Channel	P-Channel	
V <sub>GS</sub>	Gate-Source Voltage		±20	±20	V
V <sub>DS</sub>	Drain-Source Voltage		40	-40	V
V <sub>GS</sub>	Gate-Source Voltage		±20	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> =25°C	6.5	-5.5	A
		T <sub>C</sub> =70°C	4.5	-3.8	
I <sub>DM</sub>	Pulsed Drain Current (note 2)		35	-22	A
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	2	2	W
T <sub>J</sub> ,T <sub>STG</sub>	Operating Junction and Storage Temperature Range		-55 to 150	-55 to 150	°C
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (note 3)		62.5	62.5	°C/W

**Note 1:** Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Under “recommended operating conditions” the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation range of the device, the electrical characteristics is assured on DC and AC voltage by test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.

**Note 2:** Repetitive Rating: Pulse width limited by maximum junction temperature.

**Note 3:** Surface Mounted on FR4 Board,  $t \leq 10$  sec.

**N-Channel Electrical Characteristics** (Notes 4, 5) (Unless otherwise specified,  $T_A=25\text{ }^\circ\text{C}$ )

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
On Characteristics (Note 6)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.3	1.6	1.9	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=6A$	-	22	26	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=6A$	33	-	-	S
Dynamic Characteristics (Note7)						
$C_{iss}$	Input Capacitance	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0MHz$	-	310	-	pF
$C_{oss}$	Output Capacitance		-	80	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	50	-	pF
Switching Characteristics (Note 7)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20V, R_L=2.5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	4	-	ns
$t_r$	Turn-on Rise Time		-	3	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	15	-	ns
$t_f$	Turn-Off Fall Time		-	2	-	ns
$Q_g$	Total Gate Charge	$V_{DS}=20V, I_D=6A,$ $V_{GS}=10V$	-	8.5	-	nC
$Q_{gs}$	Gate-Source Charge		-	2.2	-	nC
$Q_{gd}$	Gate-Drain Charge		-	2.1	-	nC
Drain-Source Diode Characteristics						
$V_{SD}$	Diode Forward Voltage (Note 6)	$V_{GS}=0V, I_S=6A$	-	0.82	1.2	V

**P-Channel Electrical Characteristics** (Notes 4, 5) (Unless otherwise specified,  $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Off Characteristics						
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
On Characteristics (Note 6)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.5	-1.9	-2.3	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=-10V, I_D=-5A$	-	50	60	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5V, I_D=-5A$	20	-	-	S
Dynamic Characteristics (Note7)						
$C_{iss}$	Input Capacitance	$V_{DS}=-20V, V_{GS}=0V,$ $F=1.0MHz$	-	370	-	pF
$C_{oss}$	Output Capacitance		-	72	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	52	-	pF
Switching Characteristics (Note 7)						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=-20V, R_L=2.5\Omega$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	7.5	-	ns
$t_r$	Turn-on Rise Time		-	5.5	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	19	-	ns
$t_f$	Turn-Off Fall Time		-	7	-	ns
$Q_g$	Total Gate Charge		-	8.5	-	nC
$Q_{gs}$	Gate-Source Charge		-	2.6	-	nC
$Q_{gd}$	Gate-Drain Charge	-	2.1	-	nC	
Drain-Source Diode Characteristics						
$V_{SD}$	Diode Forward Voltage (Note 6)	$V_{GS}=0V, I_S=-5A$	-	-0.9	-1.2	V

**Note 4:** Production testing of the chip is performed at  $25^\circ\text{C}$ .

**Note 5:** The maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.

**Note 6:** Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .

**Note 7:** Guaranteed by design, not subject to production

N-Channel Typical Electrical and Thermal Characteristics Curves

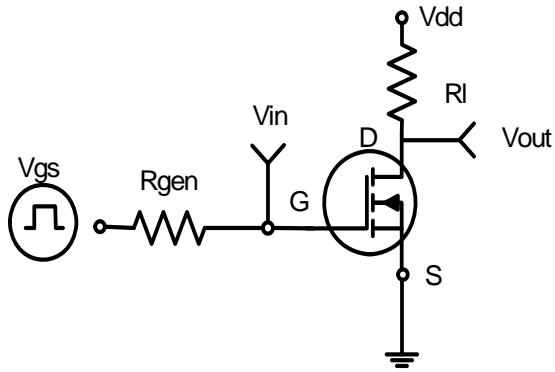


Figure 3. Switching Test Circuit

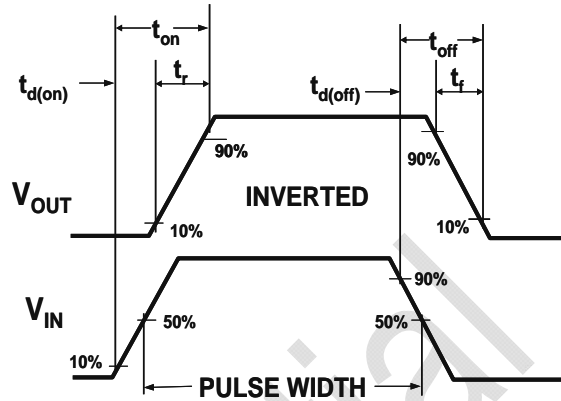


Figure 4. Switching Waveforms

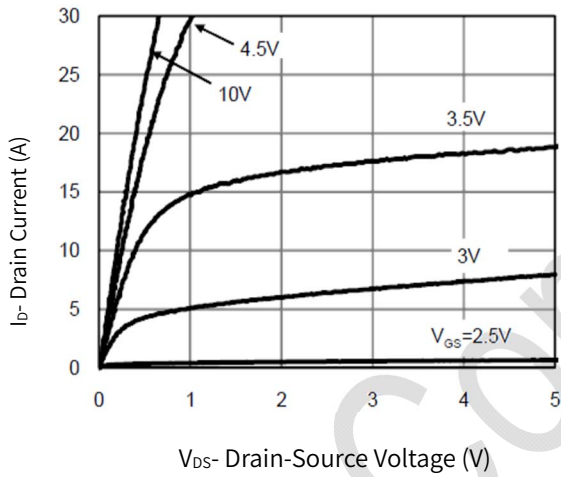


Figure 5. Output Characteristics

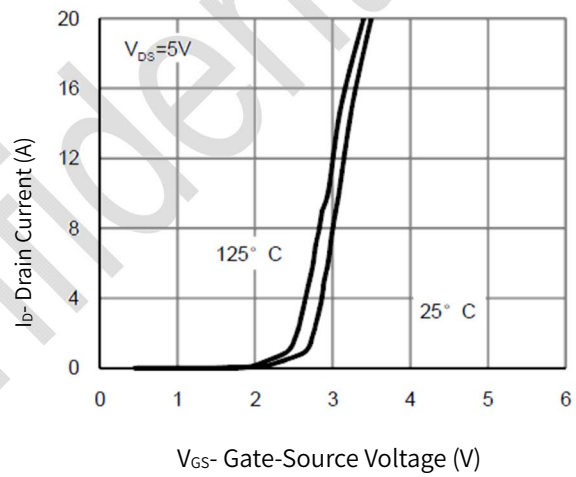


Figure 6. Transfer Characteristics

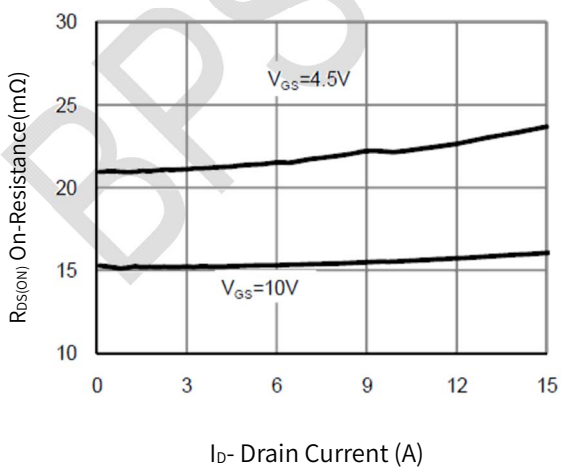


Figure 7. Drain-Source On-Resistance

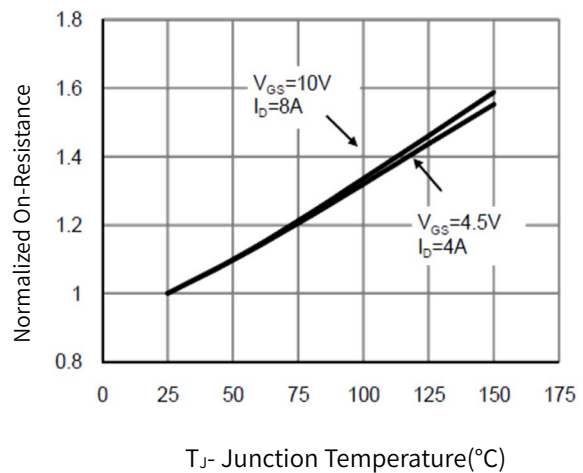


Figure 8. Drain-Source On-Resistance

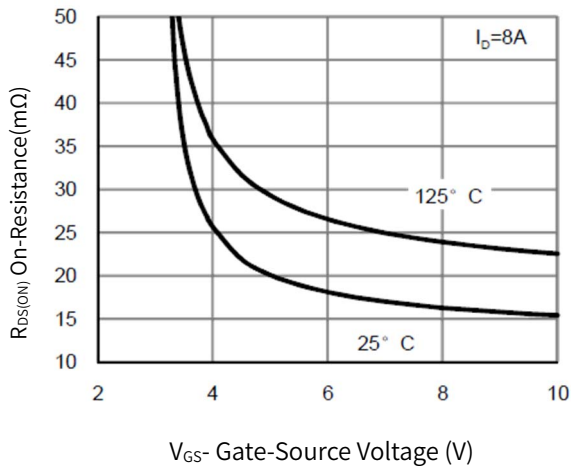


Figure 9.  $R_{DS(ON)}$  VS  $V_{GS}$

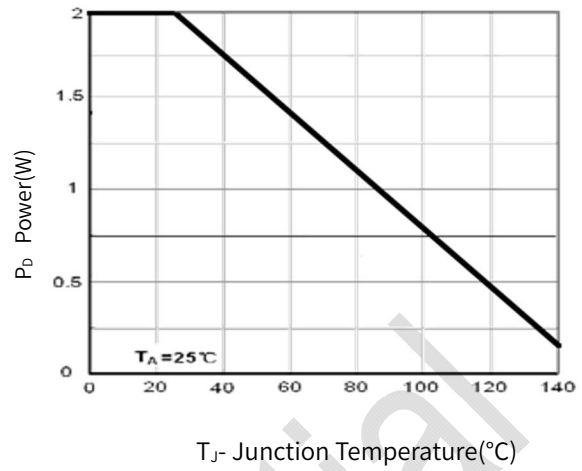


Figure 10. Power Dissipation

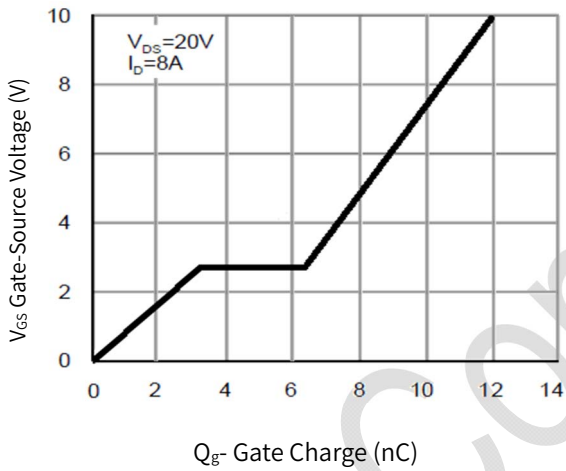


Figure 11 Gate Charge

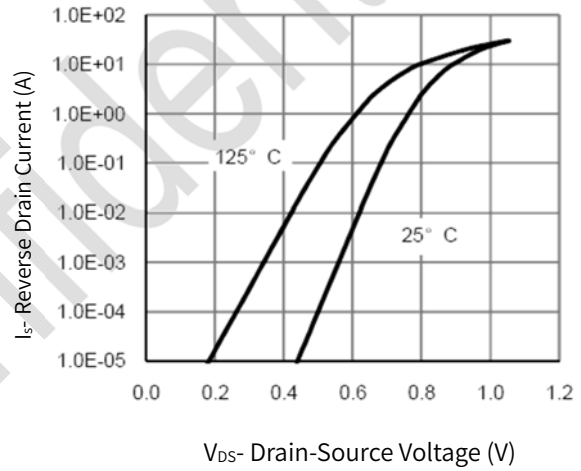


Figure 12. Source- Drain Diode Forward

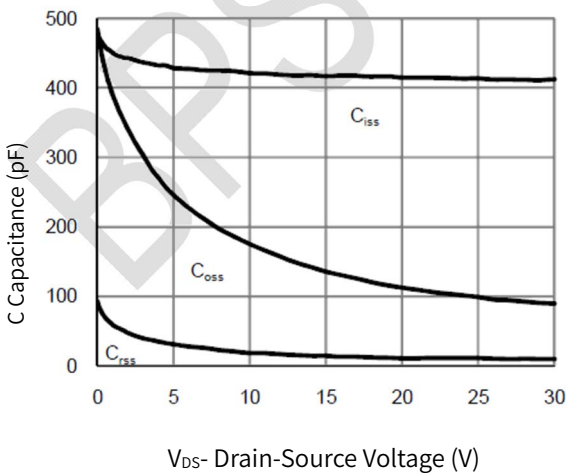


Figure 13. Capacitance vs  $V_{DS}$

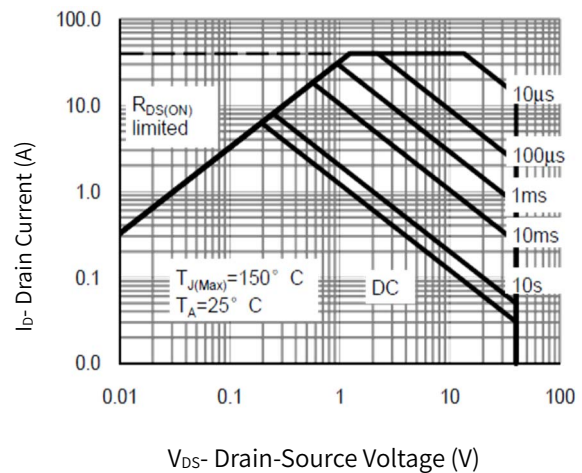


Figure 14. Safe Operation Area

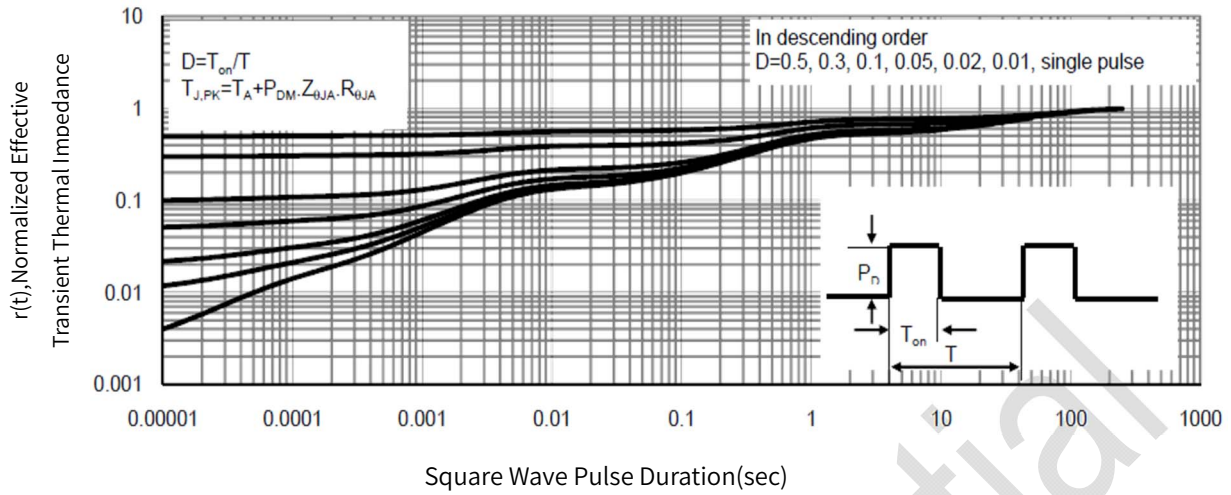


Figure 15. Normalized Maximum Transient Thermal Impedance

### P-Channel Typical Electrical and Thermal Characteristics Curves

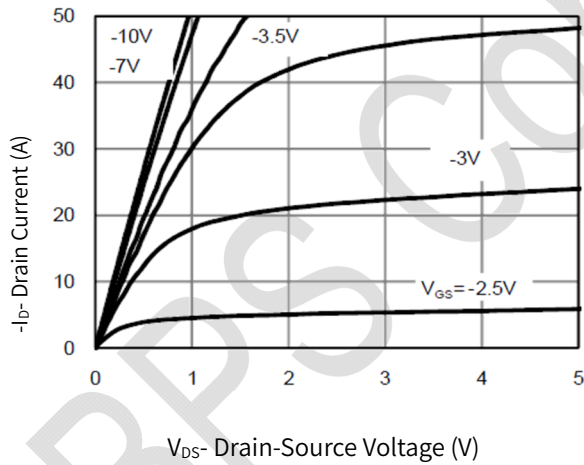


Figure 16. Output Characteristics

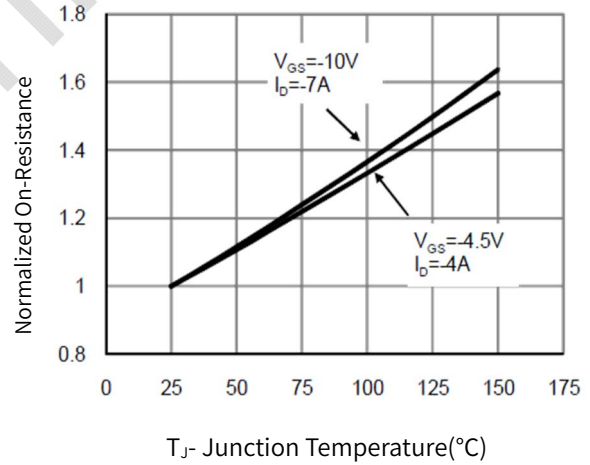


Figure 17.  $R_{DS(ON)}$ -Junction Temperature



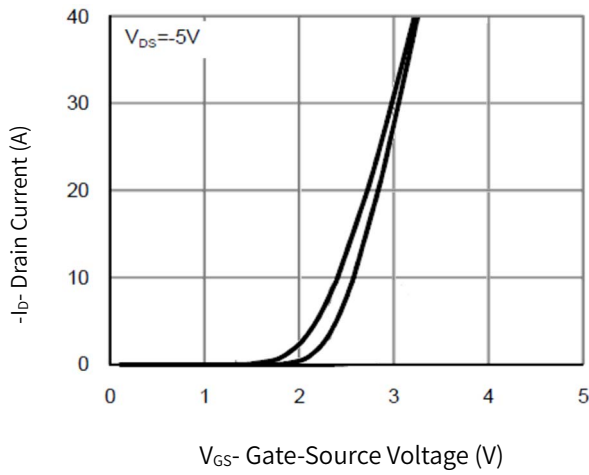


Figure 18. Transfer Characteristics

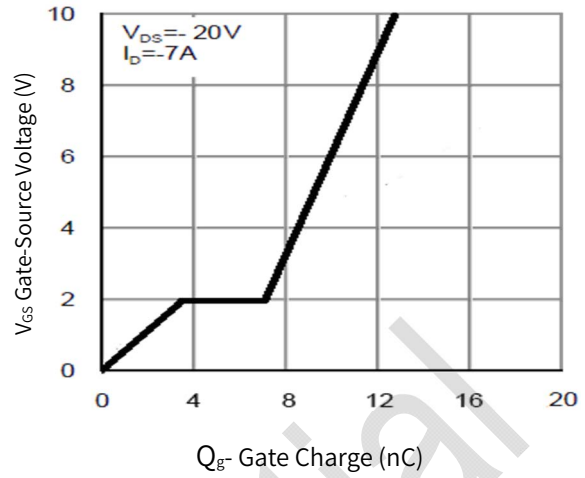


Figure 19. Gate Charge

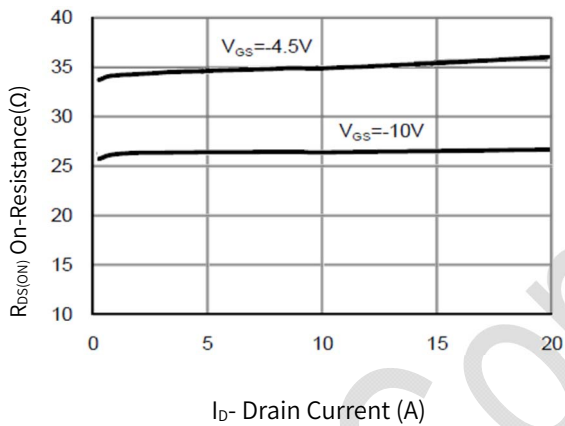


Figure 20.  $R_{DS(ON)}$ - Drain Current

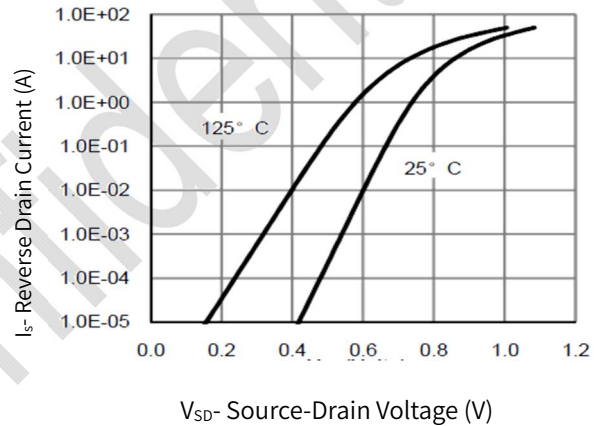


Figure 21. Source-Drain Diode Forward

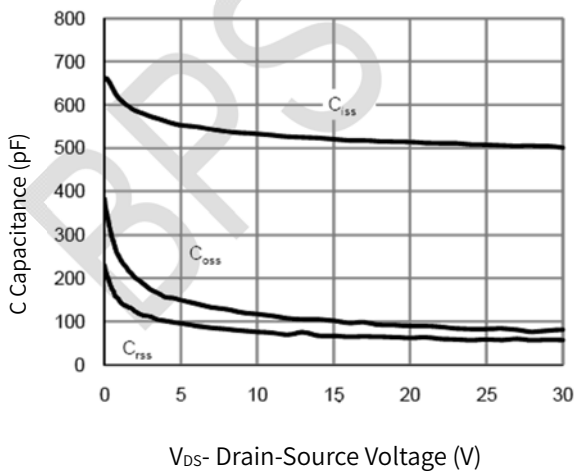


Figure 22. Capacitance vs  $V_{DS}$

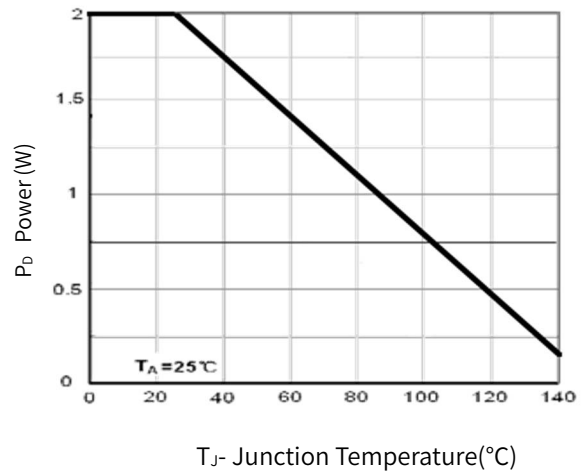


Figure 23. Power Dissipation

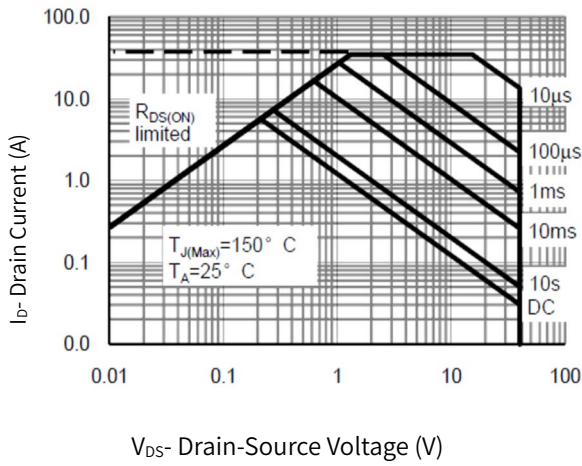


Figure 24. Safe Operation Area

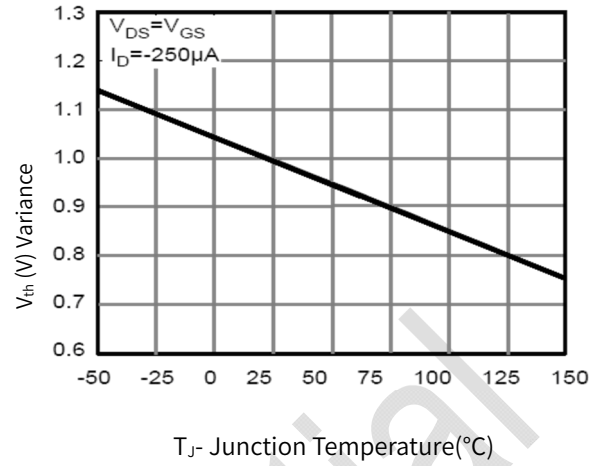


Figure 25.  $V_{GS(th)}$  vs. Junction Temperature

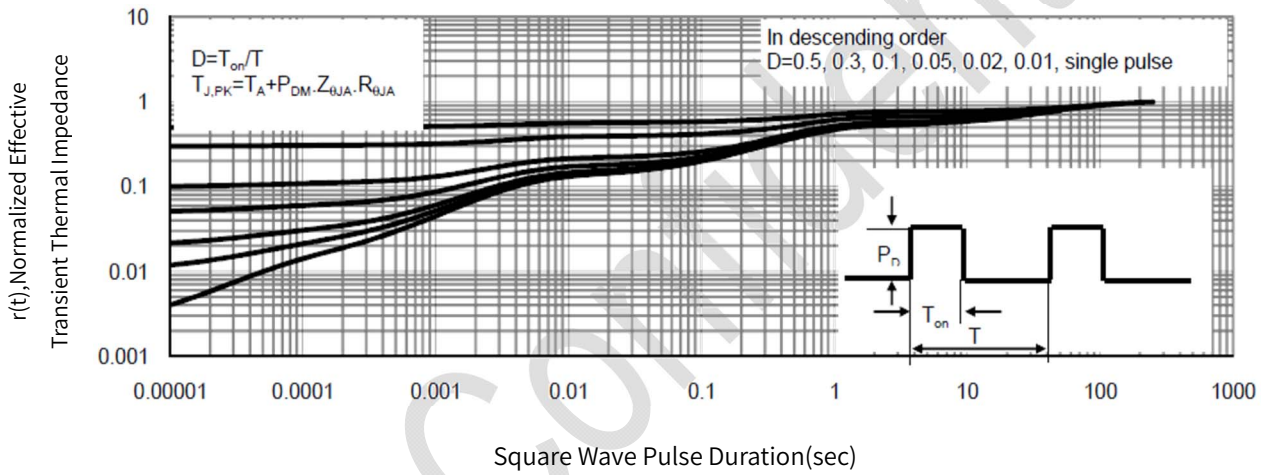
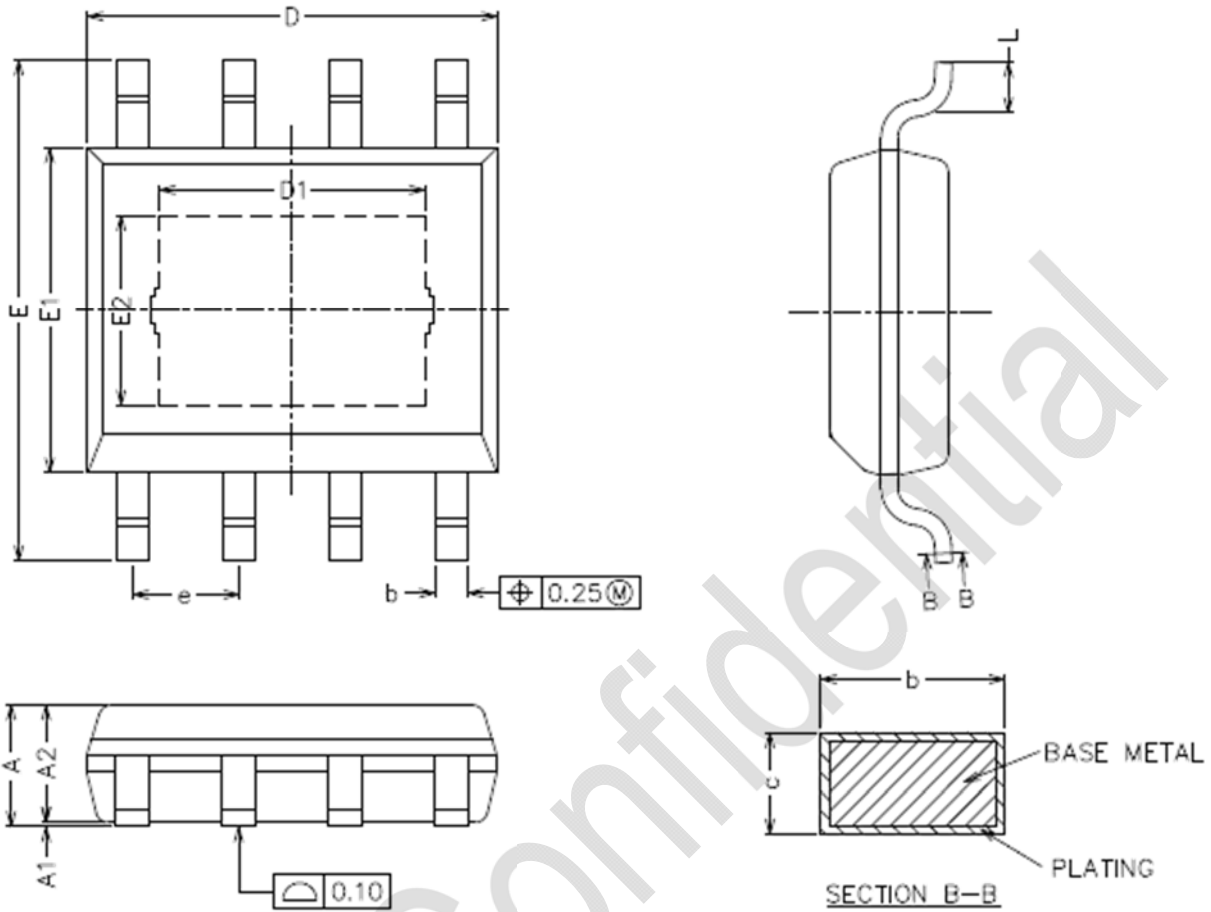


Figure 26. Normalized Maximum Transient Thermal Impedance

**Physical Dimensions**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.00	-	0.15
A2	1.25	1.40	1.65
b	0.30	-	0.50
c	0.10	-	0.25
D	4.70	4.90	5.10
D1	3.02	-	3.50
E	5.80	-	6.40
E1	3.70	3.90	4.10
E2	2.10	-	2.60
L	0.40	0.60	1.25
e	1.17	1.27	1.37

Revision Information

Revision	Date	Notes

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