

SE0503
Surface Mount TVS Avalanche Diode Array

Revision:A

General Description

The surface mount family of arrays are designed to suppress ESD and other transient overvoltage events. These arrays are used to meet the International Electrotechnical Compatibility (IEC transient immunity standards IEC 61000-4-2 for Electrostatic Discharge Requirements). The series are used to help protect sensitive digital or analog input circuits on data, signal, or control lines with voltage levels up to 5VDC.

The monolithic silicon arrays are comprised of specially designed structures for transient voltage suppression (TVS). The size and shape of these structures have be tailored for transient protection. The low capacitance and clamp voltage are ideal for high speed signal line protection.

Applications

- Mobile phone handsets
- Personal Digital Assistants (PDA)
- Portable handheld equipment (Laptop, Palmtop computers)
- Computer port, keyboard (USB1.1)
- Digital still cameras
- Digital video cameras
- MP3 players

Features

- Input Protection for Applications Up to 5VDC
- Fast Response Time < 1ns
- Low Input Capacitance 30pF Typical
- Operating Temperature Range. -40°C to 85°C

Complies with the following standards
IEC61000-4-2

Level 4 15 kV (air discharge)

8 kV(contact discharge)

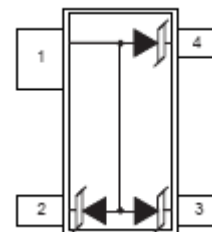
MIL STD 883E - Method 3015-7 Class 3

25 kV HBM (Human Body Model)

Functional diagram



SOT-143

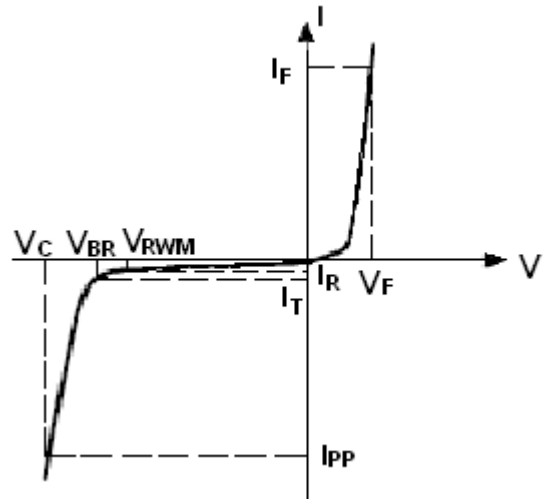


Absolute Maximum Ratings @ 25°C Unless Otherwise Specified

| Symbol | Parameter | Value | Units |
|------------------|--|------------|-------|
| P _{PP} | Peak Pulse Power (t _p = 8/20μs) - See Fig1. | 225 | W |
| T _{STG} | Storage Temperature Range | -65 to 150 | °C |

Electrical Parameter

| Symbol | Parameter |
|-----------|---|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| I_T | Test Current |
| V_{BR} | Breakdown Voltage @ I_T |
| I_F | Forward Current |
| V_F | Forward Voltage @ I_F |



Electrical Characteristics Per Line @ 25°C Unless Otherwise Specified

| Part Numbers | V_{BR} | | | I_T | V_{RM} | I_{RM} | V_F | I_F | C |
|--------------|----------|------|------|-------|----------|----------|-------|-------|--------------|
| | Min. | Typ. | Max. | | | | Max. | | Max. 0v bias |
| | V | V | V | | | | V | | pF |
| SE0503 | 6.0 | 6.6 | 9.8 | 1 | 5.0 | 1 | 1.25 | 200 | 10 |

Note 1: ESD voltage applied between channel pins and ground, one pin at a time; all other channel pins are open; all ground pins are grounded.

Typical Characteristics

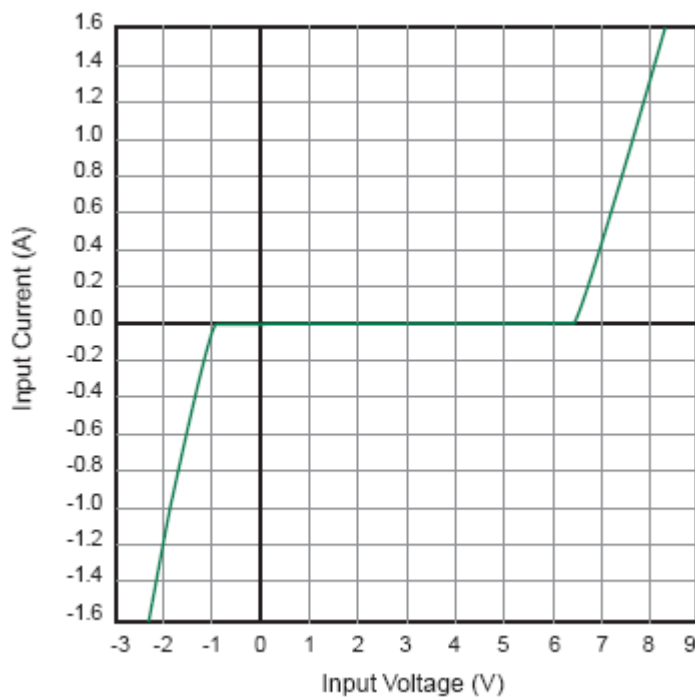


Fig1. Typical Input VI Characteristics

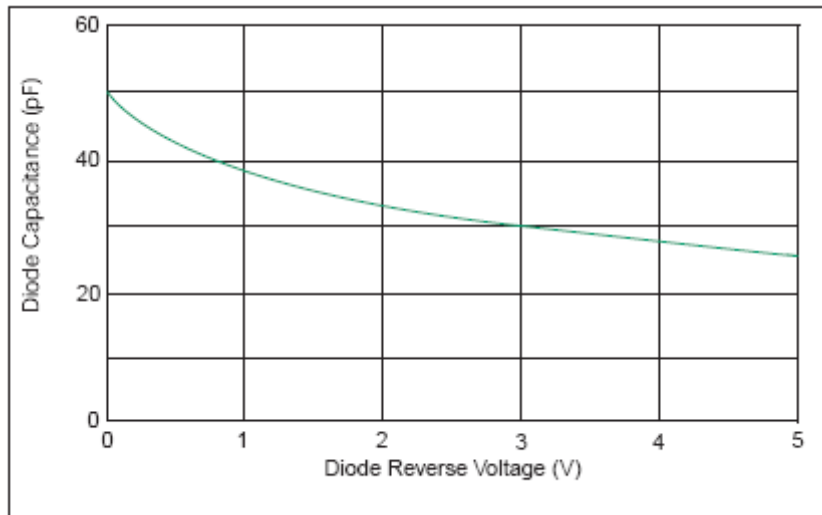
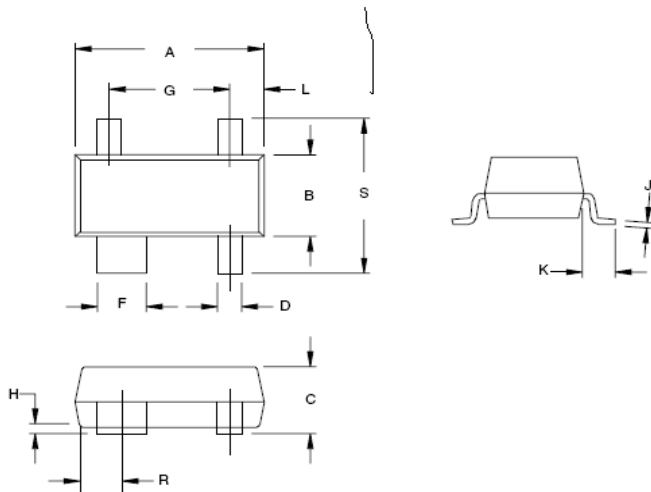


Fig2. Typical Diode Capacitance vs. Reverse Voltage

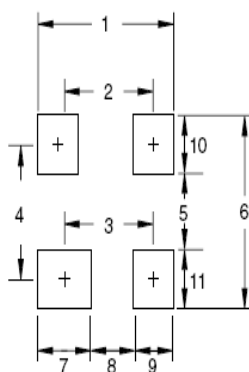
SOT-143 Mechanical Data

PACKAGE OUTLINE



MOUNTING PAD

| TYPICAL | | |
|---------|-------------|--------|
| DIM | Millimeters | Inches |
| 1 | 2.85 | 0.112 |
| 2 | 2.00 | 0.079 |
| 3 | 1.80 | 0.071 |
| 4 | 1.90 | 0.075 |
| 5 | 1.05 | 0.041 |
| 6 | 2.75 | 0.108 |
| 7 | 1.20 | 0.047 |
| 8 | 0.80 | 0.031 |
| 9 | 0.85 | 0.033 |
| 10 | 0.85 | 0.033 |
| 11 | 0.85 | 0.033 |



| PACKAGE DIMENSIONS | | | | |
|--------------------|-------------|------|--------|-------|
| DIM | MILLIMETERS | | INCHES | |
| | MIN | MAX | MIN | MAX |
| A | 2.80 | 3.04 | 0.110 | 0.120 |
| B | 1.20 | 1.39 | 0.047 | 0.055 |
| C | 0.84 | 1.14 | 0.033 | 0.045 |
| D | 0.39 | 0.50 | 0.015 | 0.020 |
| F | 0.79 | 0.93 | 0.031 | 0.037 |
| G | 1.78 | 2.03 | 0.070 | 0.080 |
| H | 0.013 | 0.10 | 0.0005 | 0.004 |
| J | 0.08 | 0.15 | 0.003 | 0.006 |
| K | 0.46 | 0.60 | 0.018 | 0.024 |
| L | 0.445 | 0.60 | 0.0175 | 0.024 |
| R | 0.72 | 0.83 | 0.028 | 0.033 |
| S | 2.11 | 2.48 | 0.083 | 0.098 |

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