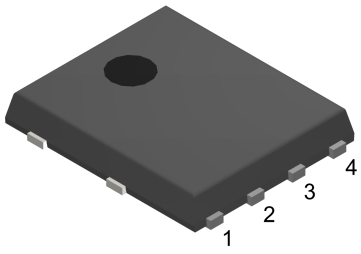
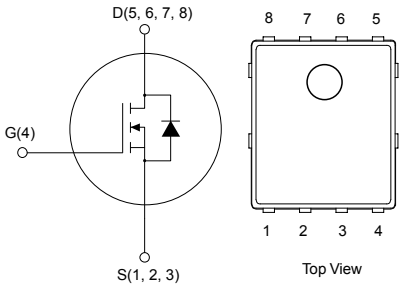
STL150N3LLH6

Datasheet

N-channel 30 V, 0.0016 Ω typ., 33 A, STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT™ 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STL150N3LLH6	30 V	0.002 Ω	33 A	PowerFLAT™ 5x6

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL150N3LLH6

Product summary	
Order code	STL150N3LLH6
Marking	150N3LH6
Package	PowerFLAT™ 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	150	A
	Drain current (continuous) at T_C = 100 °C	93	
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	33	A
	Drain current (continuous) at T_{pcb} = 100 °C	20.8	A
P_{TOT} (1)	Total power dissipation at T_C = 25 °C	80	W
P_{TOT} (2)	Total power dissipation at T_{pcb} = 25 °C	4	W
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV})	200	mJ
I_{AV}	Not-repetitive avalanche current, (pulse width limited by T_{jmax})	20	A
T_{stg} T_j	Storage temperature range Operating junction temperature range	-55 to 150	°C

1. *The value is rated according to $R_{thj\text{-}c}$.*
2. *The value is rated according to $R_{thj\text{-}pcb}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.56	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board, t < 10 s.*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_C = 125 °C (1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 16.5 A		0.0016	0.002	Ω
		V_{GS} = 4.5 V, I_D = 16.5 A		0.0025	0.0034	

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	4040	-	pF
C_{oss}	Output capacitance		-	740	-	
C_{rss}	Reverse transfer capacitance		-	425	-	
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 33 A, V_{GS} = 0 to 4.5 V (see Figure 13. Test circuit for gate charge behavior)	-	40	-	nC
Q_{gs}	Gate-source charge		-	16.3	-	
Q_{gd}	Gate-drain charge		-	15.8	-	
Rg	Gate input resistance	f = 1 MHz, I_D = 0 A	-	1.4	-	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 16.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	17	-	ns
t_r	Rise time		-	18	-	
$t_{d(off)}$	Turn-off delay time		-	75	-	
t_f	Fall time		-	46	-	

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		33	A
I_{SDM}(1)	Source-drain current (pulsed)		-		132	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 33 A	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 33 A, di/dt = 100 A/µs, V_{DD} = 25 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	34		ns
Q_{rr}	Reverse recovery charge		-	35		nC
I_{RRM}	Reverse recovery current		-	2.1		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

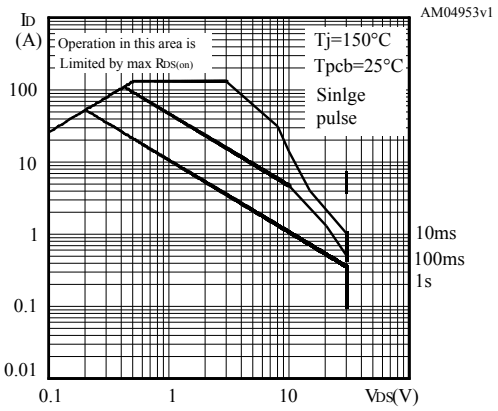


Figure 2. Thermal impedance

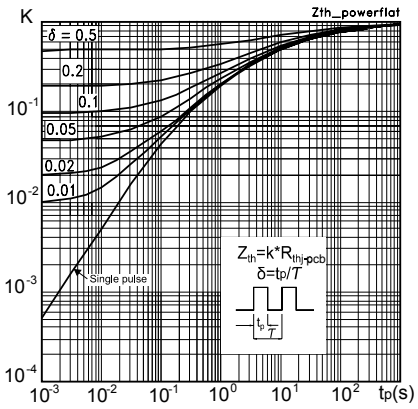


Figure 3. Output characteristics

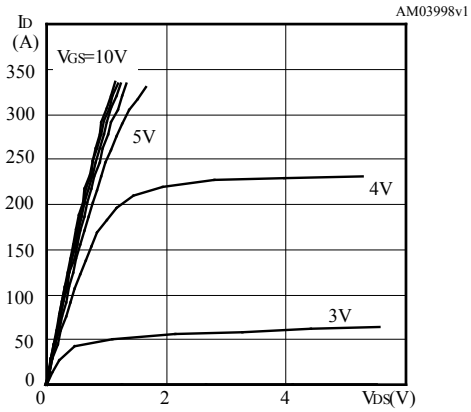


Figure 4. Transfer characteristics

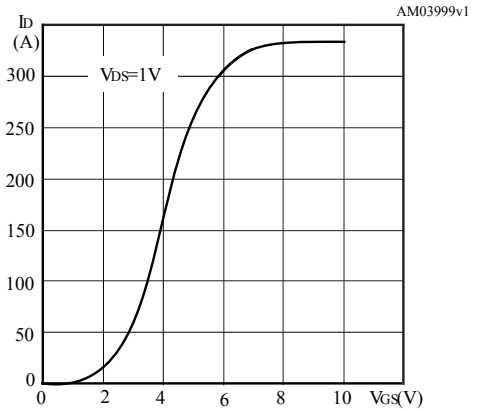


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

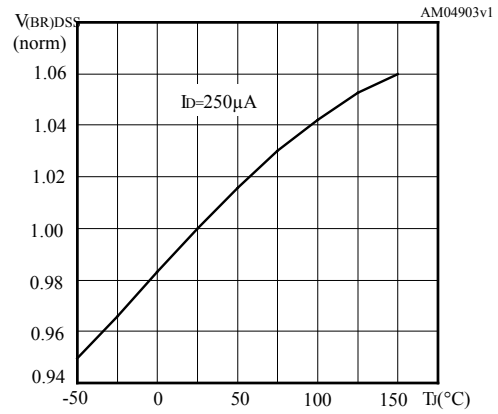


Figure 6. Static drain-source on-resistance

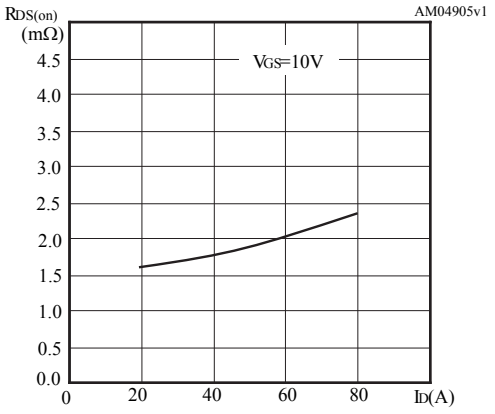


Figure 7. Gate charge vs gate-source voltage

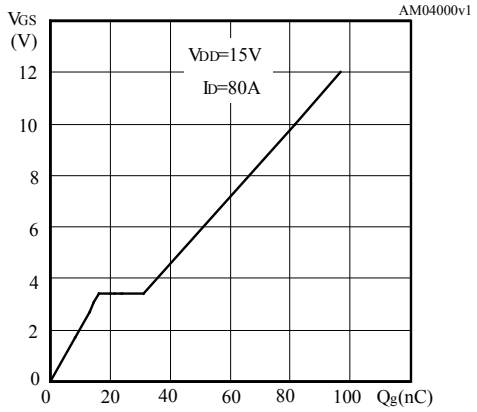


Figure 8. Capacitance variations

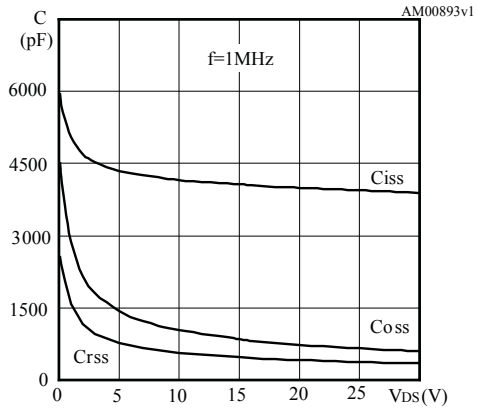


Figure 9. Normalized gate threshold voltage vs temperature

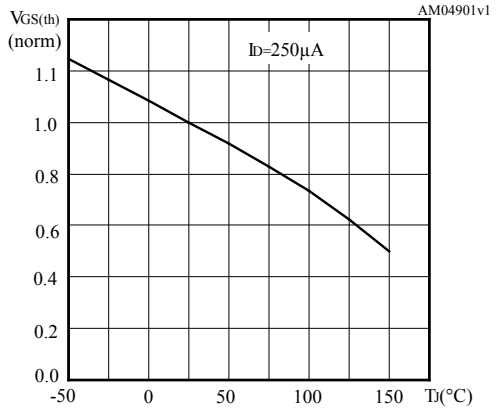


Figure 10. Normalized on-resistance vs temperature

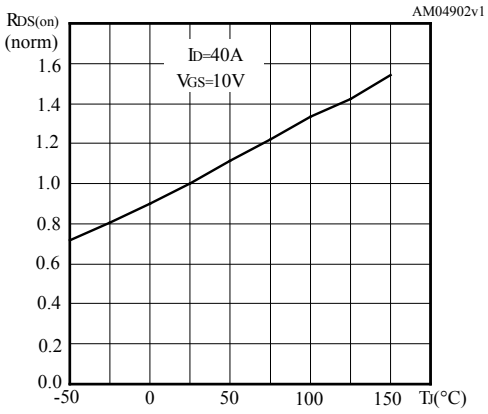
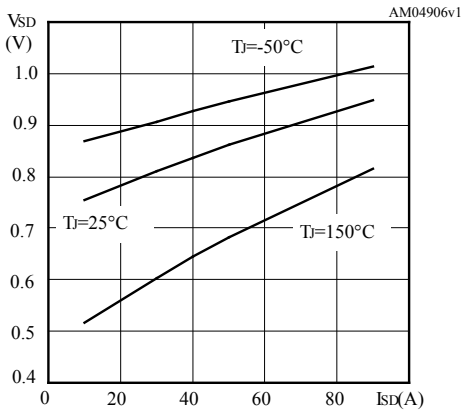


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

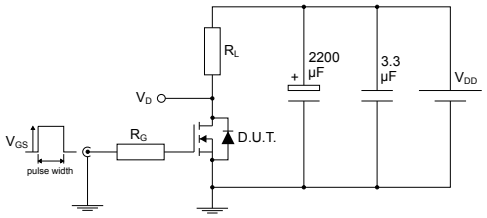


Figure 13. Test circuit for gate charge behavior

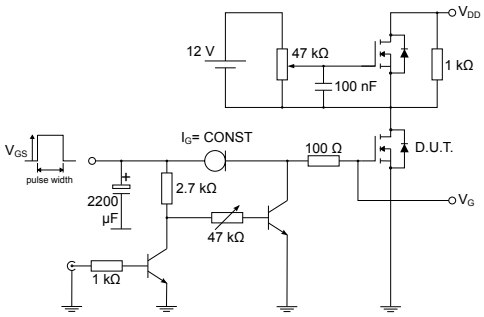


Figure 14. Test circuit for inductive load switching and diode recovery times

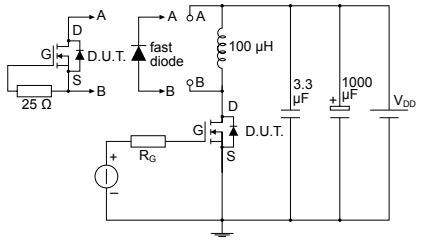


Figure 15. Unclamped inductive load test circuit

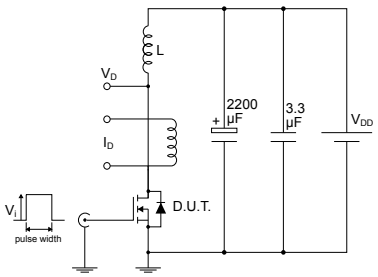


Figure 16. Unclamped inductive waveform

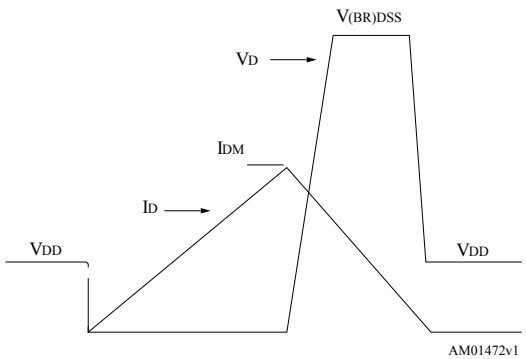
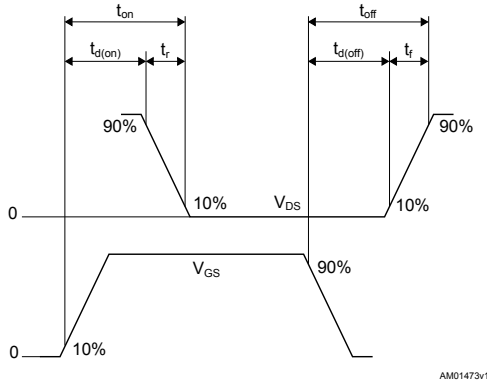


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 18. **PowerFLAT™ 5x6 type C package outline**

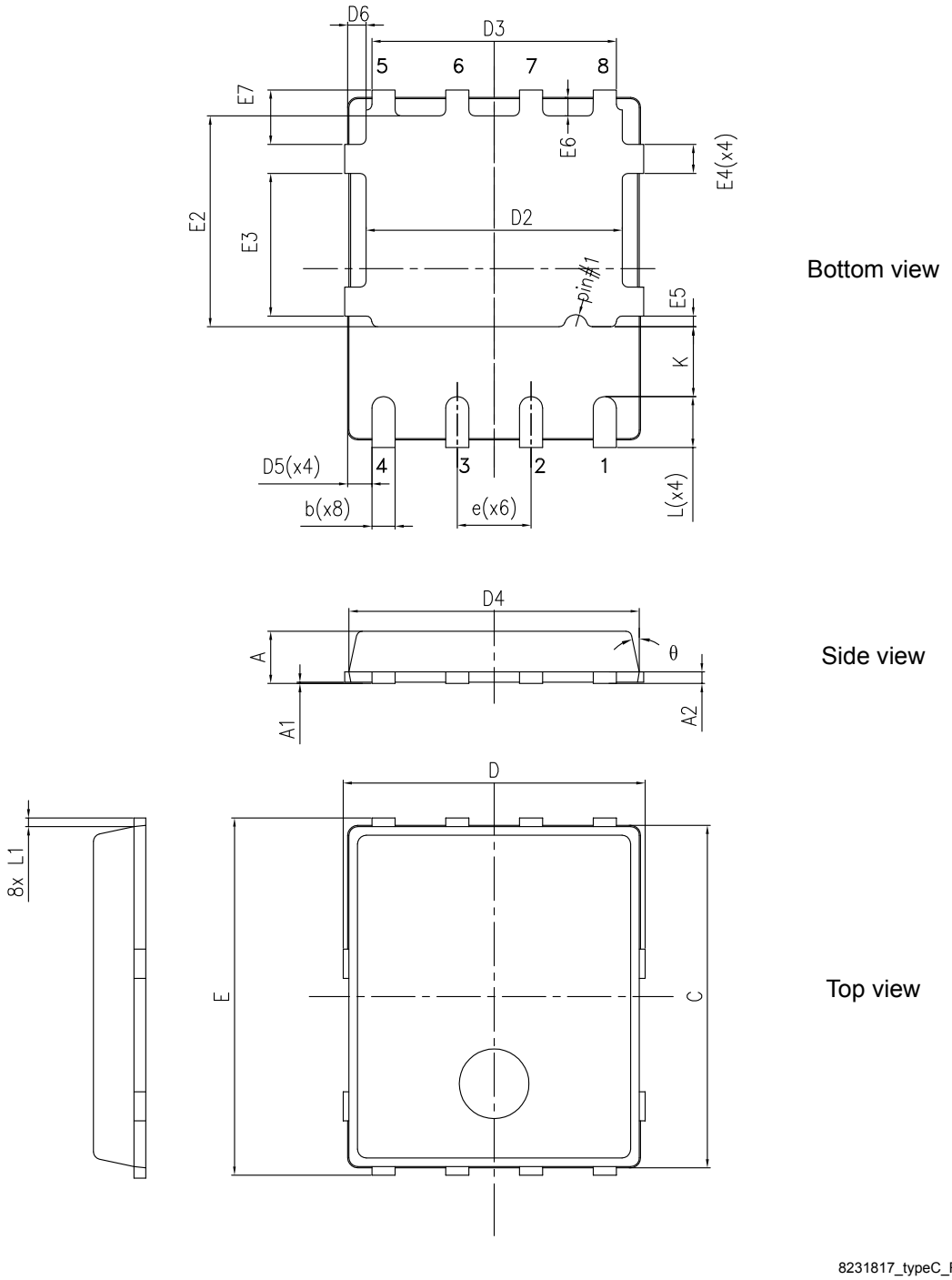
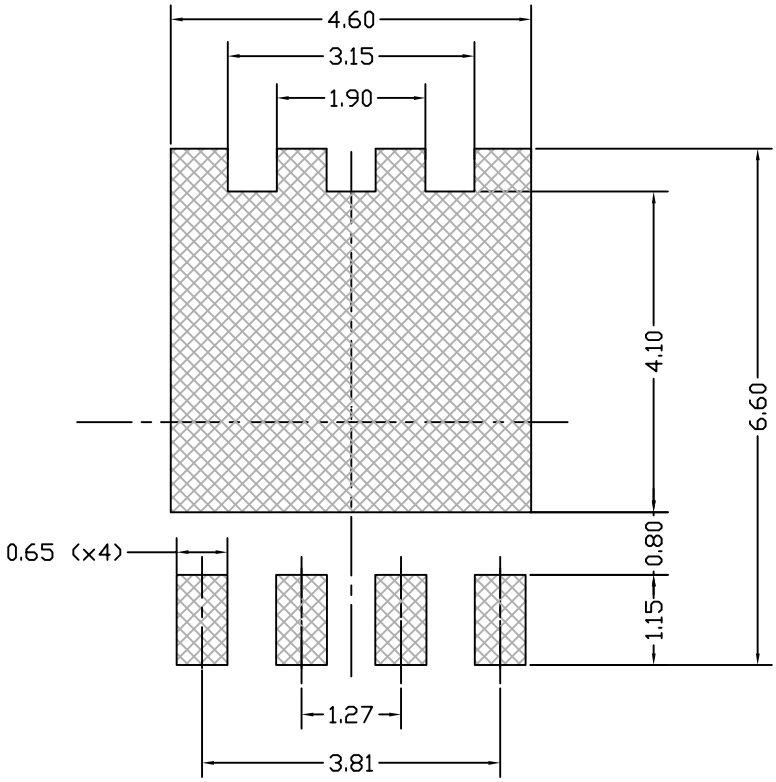


Table 7. **PowerFLAT™ 5x6 type C package mechanical data**

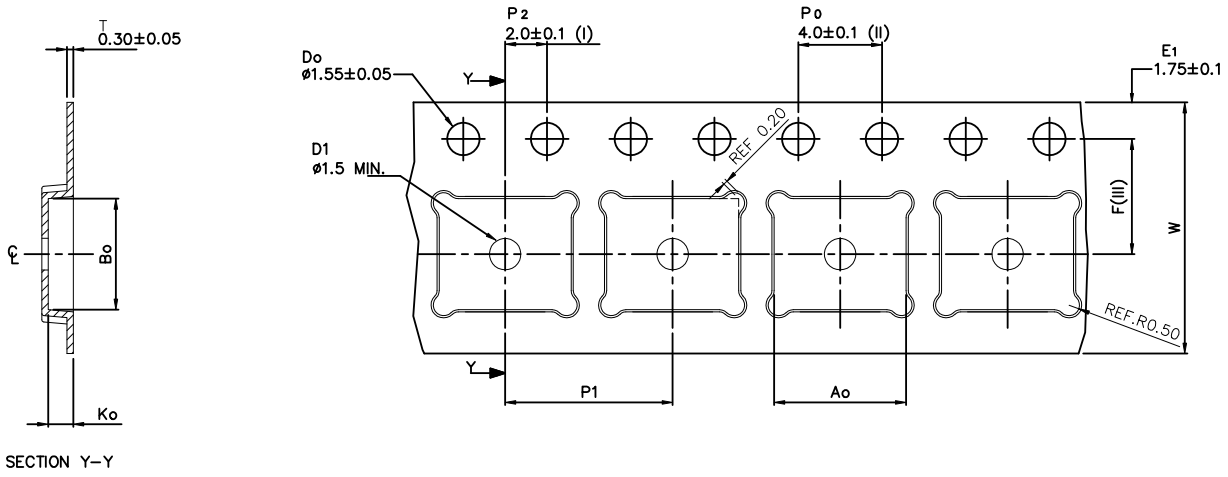
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

Figure 19. **PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)**



4.2 PowerFLAT™ 5x6 packing information

Figure 20. PowerFLAT™ 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

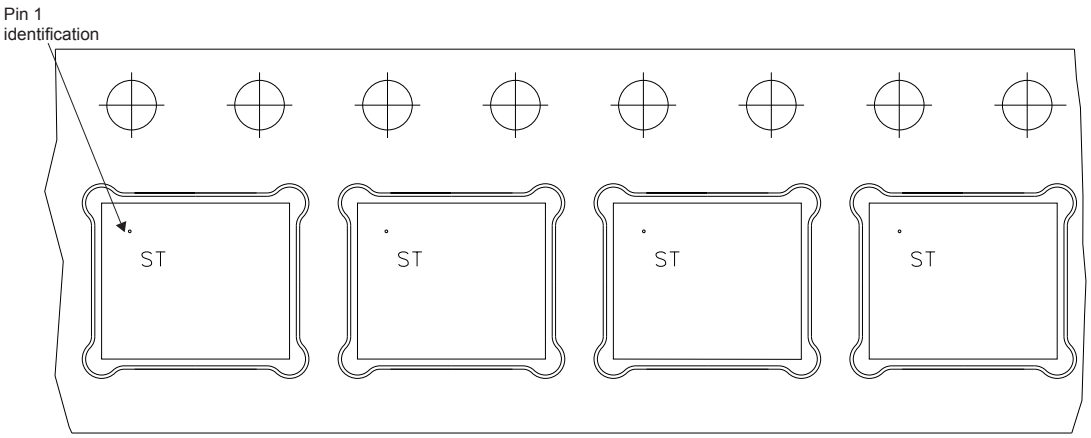
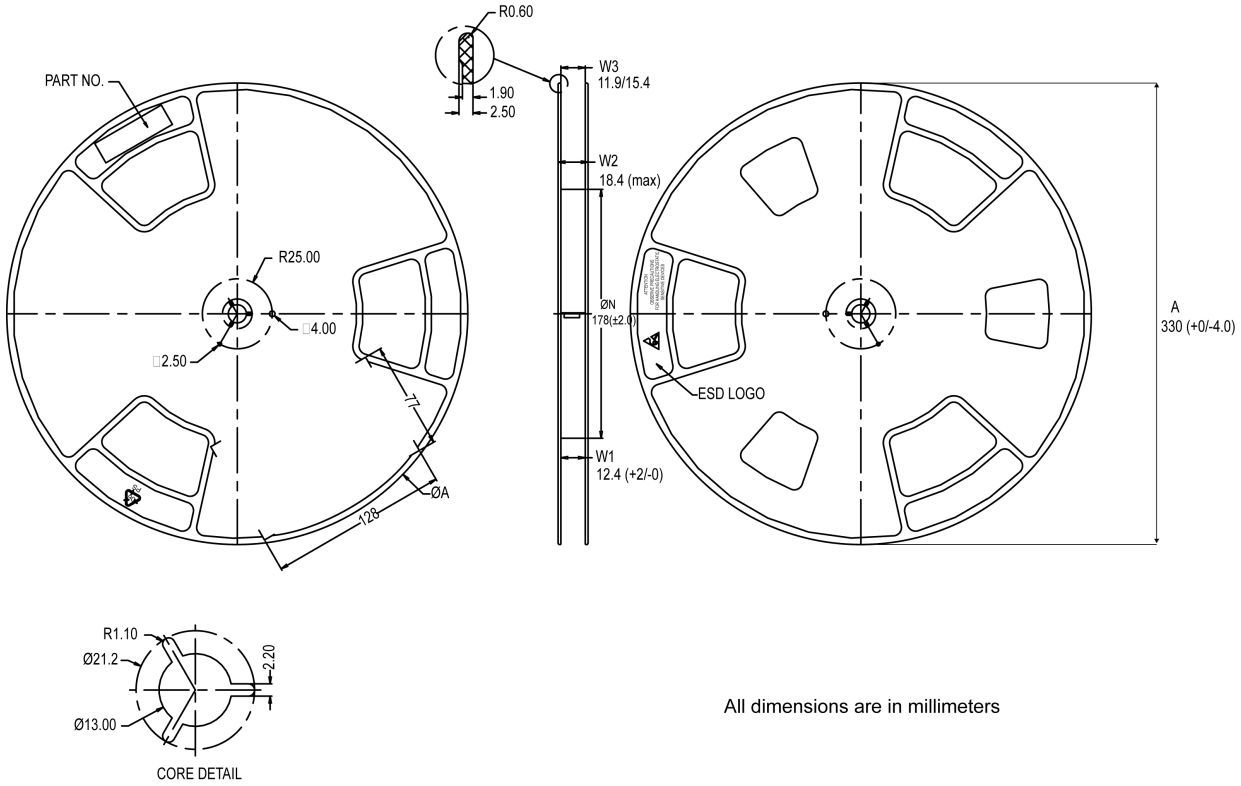


Figure 22. **PowerFLAT™ 5x6 reel**



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 8. **Document revision history**

Date	Version	Changes
21-Jan-2009	1	First release.
08-Sep-2009	2	Document status promoted from preliminary data to datasheet
11-Nov-2010	3	Corrected title in first page $R_{DS(on)}$ max value has been corrected.
03-Apr-2019	4	Modified marking on cover page. Minor text changes.

Contents