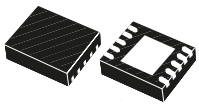
STEF12S

Datasheet

Electronic fuse for 12 V line

TSOT23-8L



DFN10 (3x3 mm)

Features

- 15 V typical output overvoltage clamp
- Absolute maximum voltage of 25 V
- Adjustable current limit
- Thermal protection
- Input undervoltage lockout
- Low inrush current during startup
- Integrated 40 mΩ Power FET
- En/fault pin
- Adjustable slew rate for output voltage
- Gate control pin for reverse current blocking FET (DFN10 package)
- TSOT23-8L and DFN10 (3x3 mm) packages
- Latch (STEF12S) or autoretry (STEF12SA) versions

Application

- Hard Disk and SSD drives
- Hard disk array
- Hot-swap board
- Hot-plug protection

Maturity status link
STEF12S

Description

The STEF12S is an integrated electronic fuse optimized to monitor the 12 V DC power lines.

When connected in series to the main power rail, it is able to precisely detect and react to overcurrent and overvoltage conditions.

When an overload condition occurs, the device limits the output current to a safe value defined by the user. If the anomalous overload condition persists, the device goes into an open state, disconnecting the load from the power supply.

In case of overvoltage on the input, the device regulates the output to a preset safe value.

Undervoltage lockout prevents the load from malfunction, keeping the device off if the rail voltage is too low.

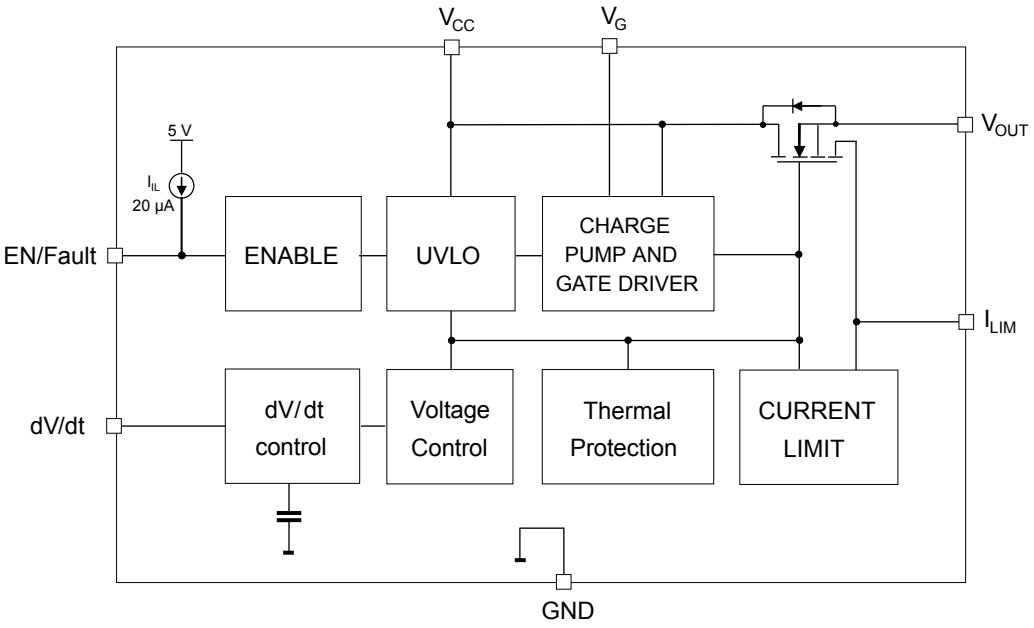
The STEF12S features the adjustable turn-on slew-rate, which is useful to keep the in-rush current under control during startup and hot-swap operations.

On the DFN10 package a dedicated pin provides a gate control for an external optional N-channel Power FET, used to implement the reverse current blocking in case of input voltage loss.

The STEF05S is a companion chip for the 5 V rails, useful to implement a complete power rail control in data-storage applications.

1 Diagram

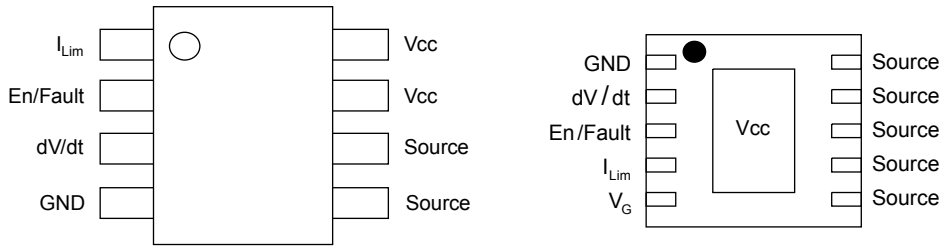
Figure 1. Block diagram



Note: Gate driver pin V_G is available on DFN10 version only.

2 Pin configuration

Figure 2. Pin connection (top view)



TSOT23-8L DFN10 3x3

Table 1. Pin description

Pin #		Symbol	Function
TSOT23-8L	DFN10		
1	4	I_{Lim}[1]	An R_{Lim} resistor between this pin and the Source pin sets the overload and short-circuit current limit levels.
2	3	En/Fault	The En/Fault pin is a tri-state, bi-directional interface. During the normal operation, the pin must be left floating, or it can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin goes into an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during thermal events.
3	2	dV/dt	The internal dV/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 0.85 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
4	1	GND	Ground connection.
5-6	6-10	Source/V_{OUT}	Connected to the source of the internal power MOSFET and to the output terminal of the fuse.
-	5	V_G	Gate driver output for the optional external reverse-blocking power MOS. Leave floating if not used.
7-8	Exposed pad	V_{CC}	Positive input voltage of the eFuse.

1. *Important: missing or shorted R_{Lim} causes current limit circuit malfunction and may lead to device damage.*

3 Typical application

Figure 3. **Typical application circuit**

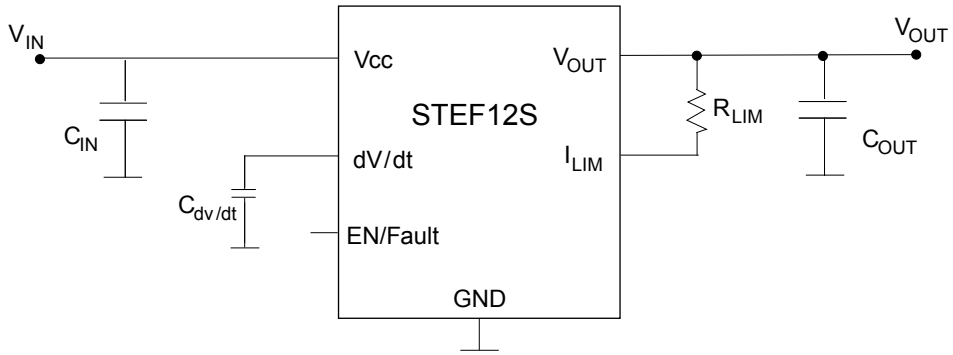
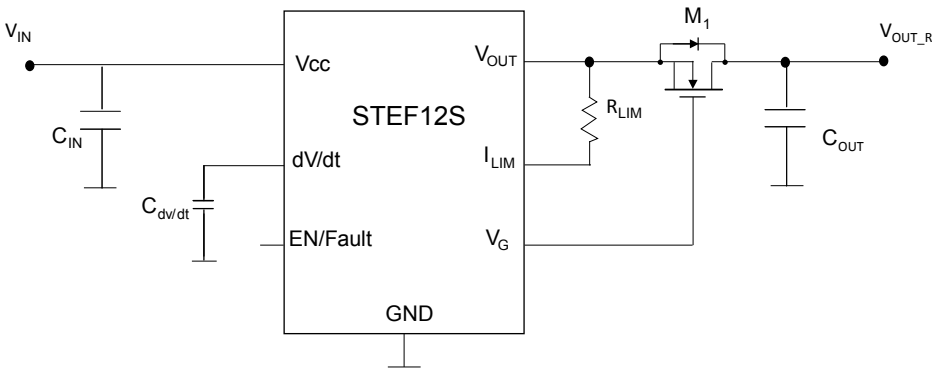


Figure 4. **Application with external reverse current blocking MOSFET**



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Positive power supply voltage	-0.3 to 25	V
V_{OUT}/source	Output voltage	-0.3 to V_{CC} + 0.3	V
V_G	Gate driver pin voltage	-0.3 to V_{OUT} + 5	V
I_{Lim}	Current limit resistor pin voltage	-0.3 to 25	V
En/Fault	En/Fault pin voltage	-0.3 to 7	V
dV/dt	dV/dt pin voltage	-0.3 to 7	V
$T_{J\text{-}OP}$	Operating junction temperature range (1)	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 s	260	°C
HBM	ESD protection - human body model	2	kV
CDM	ESD protection - charged device model (TSOT23-8L package)	500	V
	ESD protection - charged device model (DFN10-3x3 package)	500	V

1. *The thermal limit is set above the maximum thermal ratings. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3. Thermal data (TSOT23-8L)

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	140	°C/W
R_{thJC}	Thermal resistance junction-case (1)	35	°C/W

1. *Based on JESD51-7, 4-layer PCB.*

Table 4. Recommended operating condition

Symbol	Parameter	Value	Unit
V_{CC}	Operating power supply voltage	10 to 13.8	V
I_D	Maximum continuous current T_A = 25°C (1)	3.5	A
C_{IN}	Suggested input capacitor	1	µF
C_{OUT}	Minimum output capacitor	1	µF
R_{Lim}	Current limit resistor range	15.4 to 300	Ω

1. *The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J\text{-}OP}$=125°C, the junction-to-ambient thermal resistance R_{thJA}, and the ambient temperature T_A and can be estimated by: $P_{D(MAX)}$ = (125 °C - T_A) / R_{thJA}. Exceeding the maximum allowable power dissipation produces overheating that may cause thermal shutdown.*

5 Electrical characteristics

V_{CC} = 12 V, $V_{En/Fault}$ = 5 V, C_I = 10 µF, C_O = 10 µF, T_J = 25 °C (unless otherwise specified).

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Under/Overvoltage protection						
V_{Clamp}	Average output clamping voltage	V_{CC} = 17 V	13.8	15	16.2	V
V_{UVLO}	Undervoltage lockout	Turn-on, voltage rising	7.7	8.5	9.3	V
V_{Hyst}	UVLO hysteresis			0.8		V
Power MOSFET						
t_{dly}	Delay time	Enabling of chip to soft start beginning (10 % of V_{OUT}), No $C_{dv/dt}$		250		µs
R_{DSon}	On-resistance (1)	T_J = 25 °C		40	50	mΩ
		T_J = 85 °C (2)		48		
V_{OFF}	Off-state output voltage	V_{CC} = 18 V, V_{GS} = 0, R_L = infinite		1	10	mV
Current Limit						
I_{Short}	Short-circuit current limit	R_{Lim} = 22 Ω, STEF12SGR		2.8		A
I_{Lim}	Overload current limit	R_{Lim} = 22 Ω, STEF12SGR		5.5		A
I_{Short}	Short-circuit current limit	R_{Lim} = 22 Ω, STEF12SPUR		2.4		A
I_{Lim}	Overload current limit	R_{Lim} = 22 Ω, STEF12SPUR		4.6		A
I_{Short}	Short-circuit current limit	R_{Lim} = 39 Ω, STEF12SGR		1.9		A
I_{Lim}	Overload current limit	R_{Lim} = 39 Ω, STEF12SGR		3.8		A
dv/dt circuit						
dv/dt	Output voltage ramp time	From 10% to 90% of V_{OUT}, no Cdv/dt		0.85		ms
En/Fault						
V_{IL}	Low level input voltage	Output disabled			1.8	V
$V_{I(INT)}$	Intermediate level input voltage	Thermal fault, output disabled	1.2	1.3	1.45	V
V_{IH}	High level input voltage	Output enabled	2.5			V
$V_{I(MAX)}$	High state maximum voltage			4.9		V
I_{IL}	Low level input current (sink)	$V_{En/Fault}$ = 0 V		-20	-50	µA
I_I	High level leakage current for external switch	$V_{En/Fault}$ = 5 V			1	µA
	Maximum fan-out for fault signal	Total numbers of chips that can be connected to this pin for simultaneous shutdown			3	Units
Current consumption						
I_{Bias}	Bias current	Device operational		0.37		mA
		Thermal shutdown (2)		0.16		
		Off mode, $V_{En/Fault}$ = 0 V		0.12		
External MOSFET gate driver (DFN10 package only)						
I_G	Sourcing current	Device On		30		µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_P	Pull-down current	$V_{En/fault}$ = 0 V		8		mA
V_G	Gate driver voltage	V_G - V_{OUT}		5		V
Thermal protection						
T_{SHDN}	Thermal shutdown			165		°C
	Hysteresis			20		

1. *Pulsed test.*
2. *Guaranteed by design and correlation but not tested in production.*

6 Application information

6.1 Turn-on and soft startup feature

When the input voltage is applied, the En/Fault pin goes up to the high state and the internal control circuitry is enabled.

After an initial delay time of typically 250 µs, the output voltage is ramped up with a slope defined by the internal dv/dt circuitry. If no additional capacitor is connected to dV/dt pin, the ramp-up time (V_{OUT} from 10% to 90%) is around 0.85 ms.

Connecting a capacitor between the $C_{dv/dt}$ pin and GND allows the modification of the output voltage ramp-up time. Given the desired time interval Δt during which the output voltage goes from zero to its maximum value, the capacitance to be added on the $C_{dv/dt}$ pin can be calculated using the following theoretical formula.

$$\Delta t\,(ms) = 0.85 + C_{dv/dt}(pF) \times 0.021$$

Where $C_{dv/dt}$ is expressed in farads and the time in seconds.

Figure 5. Delay time and V_{OUT} ramp-up time

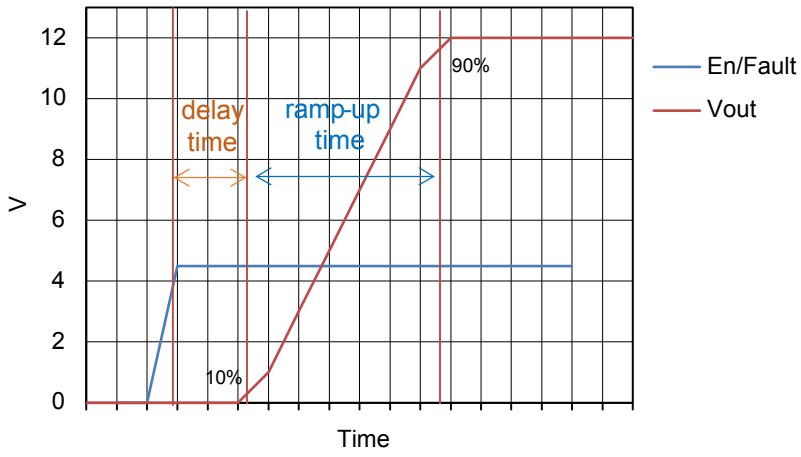


Table 6. Rise time vs. C_{dvdt}

C_{dvdt} (pF)	0	22	33	47	100	180	270	470	1000
Rise time (ms)	0.85	1.3	1.56	1.9	3	4.7	6.6	11	22

6.2 Maximum load at startup

Depending on supply voltage and load, it is possible that during startup the power dissipation is such that the maximum power protection is triggered and the output is shut down before the startup is complete. The EN/Fault signal is set according to Figure 6. En/Fault driver circuit. En/Fault pin behavior during thermal protection events.

In case of strong capacitive loads, the total start-up time may be longer than the programmed start-up time, since it is dependent also on the limitation current, the output load and the output capacitance value. In such a situation, the foldback current limit could activate, so that the startup is longer or interrupted by the intervention of thermal protection. To avoid this occurrence, a longer start-up time should be set by the appropriate selection of the $C_{dv/dt}$ capacitor.

6.3 Normal operating conditions

The STEF12S eFuse behaves like a mechanical fuse, supplying the circuitry on its output with the same voltage shown on its input, with a small voltage fall due to the internal N-channel MOSFET $R_{DS(on)}$.

6.4 Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 15 V, if the input voltage exceeds the V_{CLAMP} threshold. In this condition, the device regulates the output voltage, therefore the power dissipation increases. Thermal shutdown can occur if the overvoltage persists.

6.5 Current limiting

During the operation, if the load current reaches the I_{LIM} threshold, an overload is detected. The current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the I_{SHORT} value. The overload threshold and current limit can be customized by the limiting resistor R_{Lim} Figure 3. Typical application circuit.

As shown in Section 1 Diagram, the device uses an internal N-channel sense FET with a fixed ratio, to monitor the output current and limit it at the level set by the user.

To achieve the requested current limitation, the R_{Lim} value can be selected by using the following table, together with the graph in Figure 10. I_{Lim} and I_{Short} vs. R_{Lim} - (STEF12SGR) and Figure 11. I_{Lim} and I_{Short} vs. R_{Lim} - (STEF12SPUR). Higher resistor values can be used, but due to the current limit trend shown in the before mentioned graphs, the minimum values of I_{LIM} and I_{SHORT} are asymptotically limited.

Table 7. I_{LIM} / I_{SHORT} vs. R_{Lim} STEF12SGR

R_{Lim} (Ω)	15.4	22	24.9	30	39	49.9	100	200	300
I_{LIM} (A)	8	5.5	5.1	4.4	3.8	3.2	2.4	1.7	1.5
I_{SHORT} (A)	5.1	2.8	2.6	2.3	1.9	1.5	0.8	0.4	0.3

Table 8. I_{LIM} / I_{SHORT} vs. R_{Lim} STEF12SPUR

R_{Lim} (Ω)	15.4	22	24.9	30	39	49.9	100	200	300
I_{LIM} (A)	5.9	4.6	4.4	3.8	3.2	2.8	2	1.5	1.3
I_{SHORT} (A)	3.2	2.4	2.2	1.9	1.7	1.5	0.8	0.4	0.3

Note: Missing or shorted R_{Lim} causes current limit circuit malfunction and may lead to the device damage.

6.6 Thermal shutdown

If the device temperature exceeds the thermal shutdown threshold (T_{SHDN}), typically 165 °C, the power MOSFET is turned off and the load disconnected.

On the STEF12S latch version, the EN/Fault pin of the device is automatically set to an intermediate voltage (typically 1.3 V), in order to signal the overtemperature event to the system controller.

The device can be reset from this condition either by cycling the supply voltage or by pulling down the EN pin below the V_{il} threshold and then releasing it.

On the autoretry version (STEF12SA), the EN/Fault pin is set to a low logic level and the autoretry circuit attempts to restart the device with soft-start once the die temperature is reduced to 145 °C typ. (165 °C minus the hysteresis value, 20 °C typ.).

6.7 En/Fault pin

The EN/Fault pin has the dual function of controlling the output of the device and providing information about the device status to the application. A simplified diagram of this circuit is depicted in Figure 6.

When it is used as a standard Enable pin, it can be connected to an external open drain or open-collector device. In this case, when it is pulled to a low logic level, it turns the output of the eFuse off.

High and low logic levels are defined as V_{IH} and V_{IL} in Table 5.

If this pin is left floating, since it has an internal pull-up circuitry, the eFuse is turned on.

Pull-up current is 20 µA clamped to 5 V ($V_{I(MAX)}$).

On the STEF12S (latch version), in case of thermal fault, the pin is pulled to an intermediate state ($V_{I(INT)}$) as shown in Figure 6. En/Fault driver circuit. This signal can be provided to a monitor circuit, informing it that a thermal shutdown has occurred, or it can be directly connected to the EN/Fault pins of other eFuse devices on the same application in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the Enable pin below the V_{il} threshold and then releasing it.

On the STEF12SA autoretry version, once the thermal shutdown is triggered, the EN/Fault pin of the device is set to low state. It goes back to high level once the autoretry occurs.

Figure 6. En/Fault driver circuit

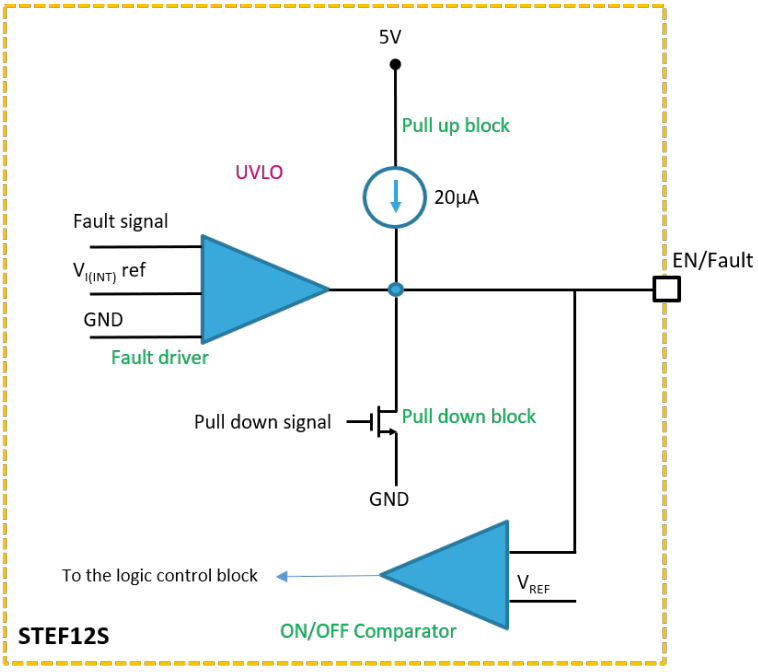
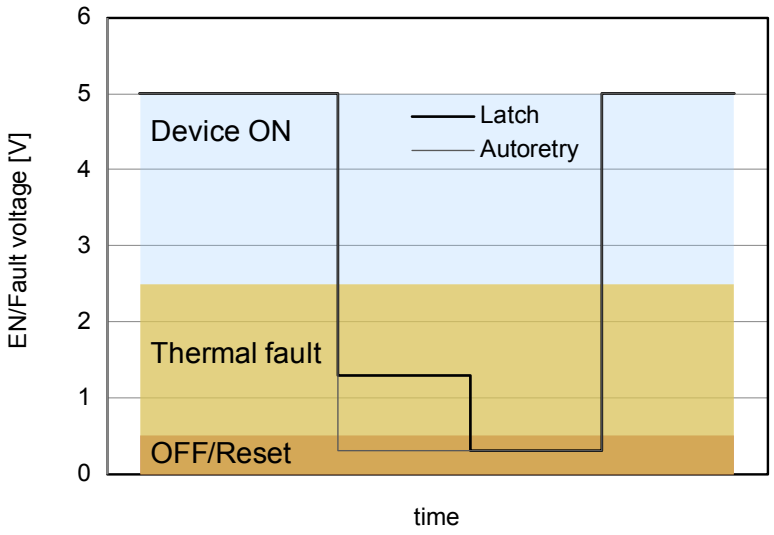


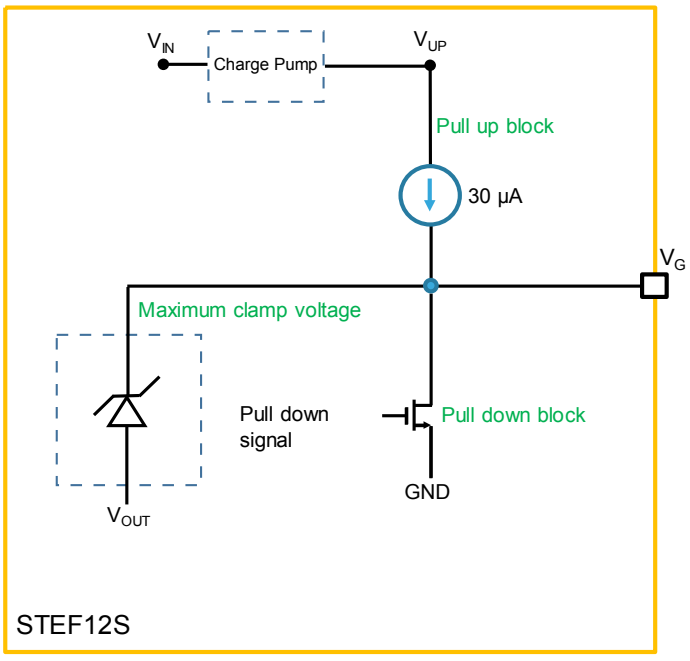
Figure 7. **En/Fault pin status**



6.8 Reverse blocking function

Many applications require reverse current blocking, to allow the completion of pending system activities (such as writing the data on SSD or parking the head in HDD) in case of power loss or during brownout. The STEF12S provides a dedicated gate drive signal on the V_G pin, which can be used to control an external blocking MOSFET, M1 as shown in Figure 4 and Figure 8. As V_{CC} drops during input power removal, the signal on V_g falls, and both the internal pass element and M1 MOSFET are turned off, therefore blocking any current flow from the load to the input of the eFuse. By appropriate selection of C_{OUT} the required load current can be guaranteed to complete the power-down sequence.

Figure 8. **External gate driver circuit (only on DFN10 version)**



6.9 Application suggestions and PCB layout guidelines

Input and output capacitors are mandatory to guarantee the device control loop stability and reduce the transient effects of stray inductances, which may be present on the input and output power paths. In fact, when the STEF12S interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output.

To reduce the effects of such transients, a C_{IN} capacitor of at least 1 µF (including voltage and temperature derating) is recommended between the input pin and GND, and located as close as possible to the device.

For the same reason, a C_{OUT} capacitor of at least 1 µF (including voltage and temperature derating) must be connected to the output port.

When the device is powered by a power line made up of very long wires, the input inductance is higher than few µH, so the input capacitor should be increased in order to guarantee the proper operation of the device.

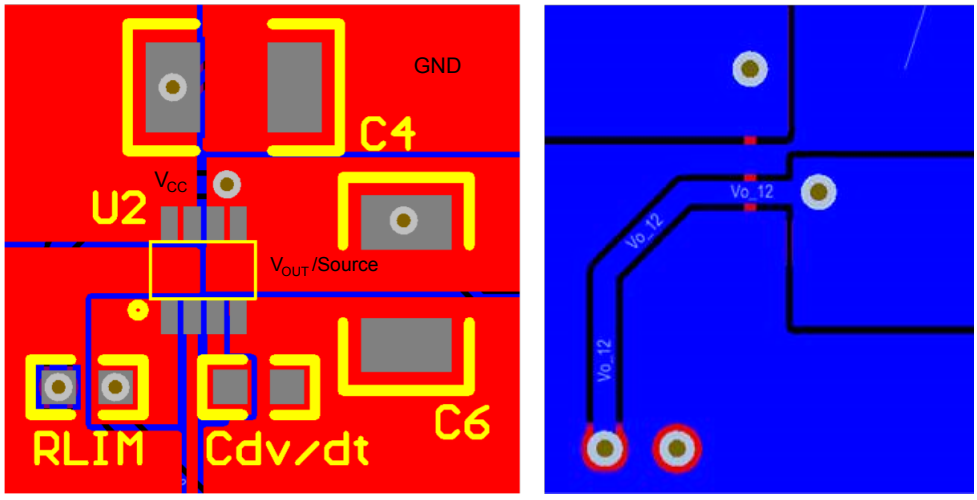
It is suggested to provide for additional protections and methods to address these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes
- Schottky diode on the output to absorb negative spikes. The negative AMR of V_{OUT} pin is - 0.3 V (see Table 2.), nevertheless, negative transient up to - 0.6 V with a maximum duration of 50 µs are tolerated by the device. Schottky diode must be selected to satisfy the above requirements.
- Combination of ceramic and electrolytic capacitors on the input and output.

The PCB layout is critical for a stable and reliable operation. Refer to the typical PCB layout example shown in Figure 9. PCB layout example and to the following guidelines:

- Defining the high current input and output copper traces as short as possible and adequately sized to sustain at least the overload current
- Placing the R_{Lim} resistor close to the ILim pin and connect the other terminal of the component to V_{OUT} with the shortest possible trace. In fact, parasitic effects on the R_{Lim} connection trace can affect the current limit accuracy.
- Placing the $C_{dv/dt}$ capacitor close to the dV/dt pin and connect the other terminal to GND with the shortest possible trace. Use low-leakage components for C_{dvdt}.
- The TSOT23-8L package dissipates the thermal power mainly through the leads, so providing large enough copper areas around the PCB soldering pads is recommended.

Figure 9. PCB layout example



Top layer Bottom layer

7 Typical characteristics

V_{CC} = 12 V, $V_{En/Fault}$ = floating, R_{Lim} = 22 Ω, C_{OUT} = 10 µF, $C_{dV/dt}$ = floating, T_A = 25°C, unless otherwise specified.

Figure 10. I_{Lim} and I_{Short} vs. R_{Lim} - (STEF12SGR)

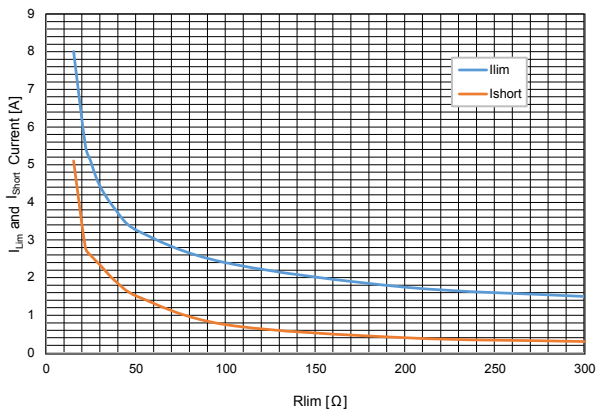


Figure 11. I_{Lim} and I_{Short} vs. R_{Lim} - (STEF12SPUR)

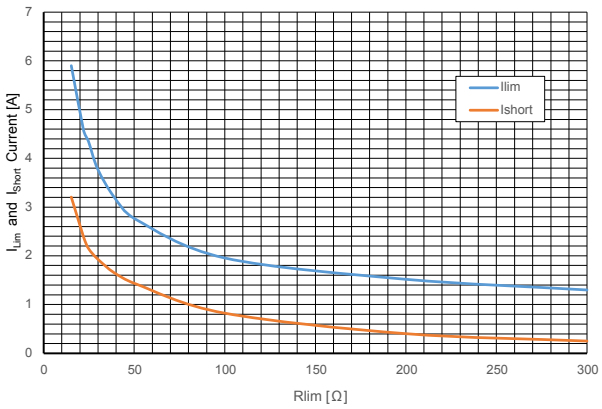


Figure 12. Bias current vs. temperature

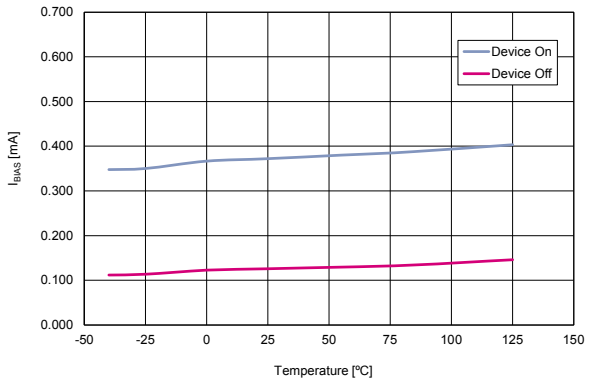


Figure 13. Bias current vs. temperature (thermal shutdown)

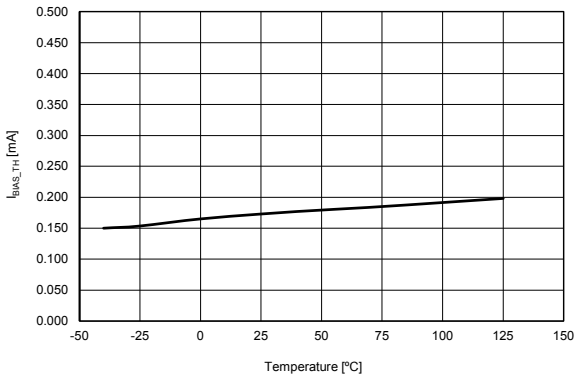


Figure 14. R_{DS_ON} vs. temperature

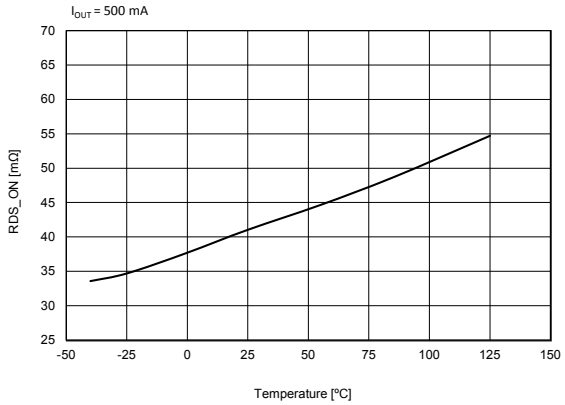


Figure 15. I_{LIM} vs. temperature

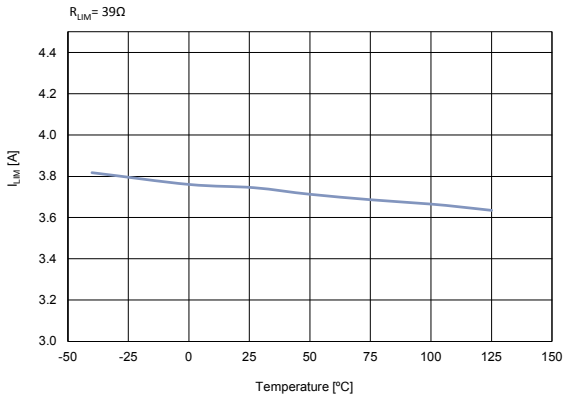


Figure 16. I_{Short} vs. temperature

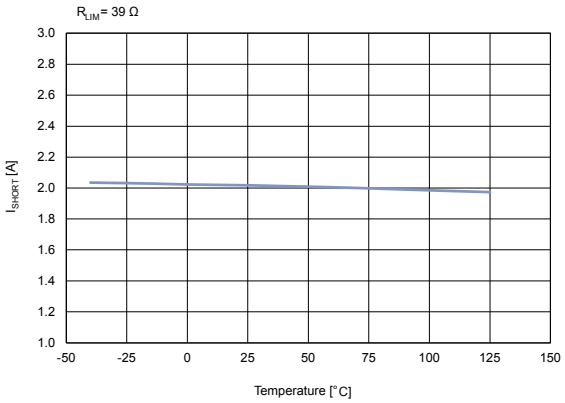


Figure 17. Clamping voltage vs. temperature

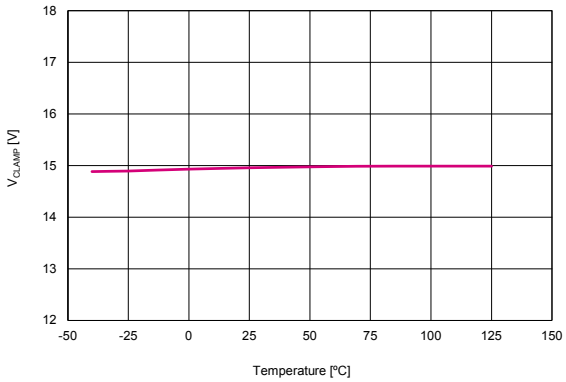


Figure 18. UVLO vs. temperature

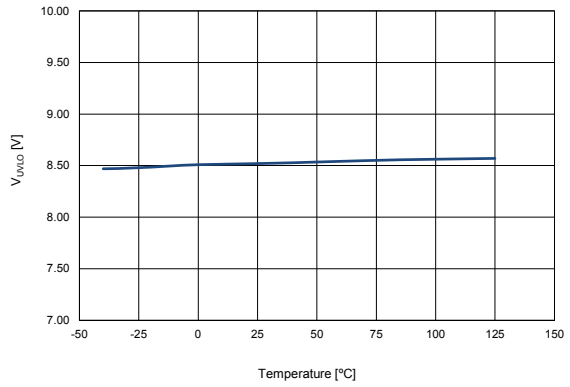


Figure 19. UVLO hysteresis vs. temperature

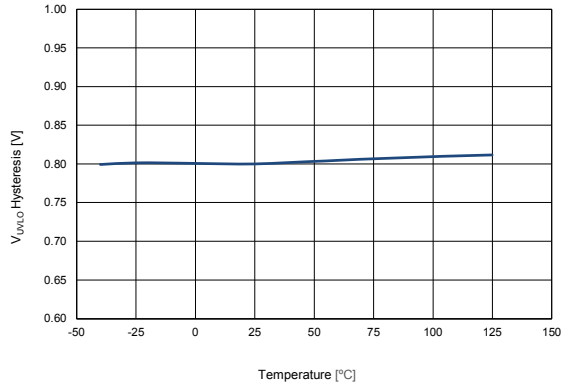


Figure 20. En/Fault pin thresholds vs. temperature

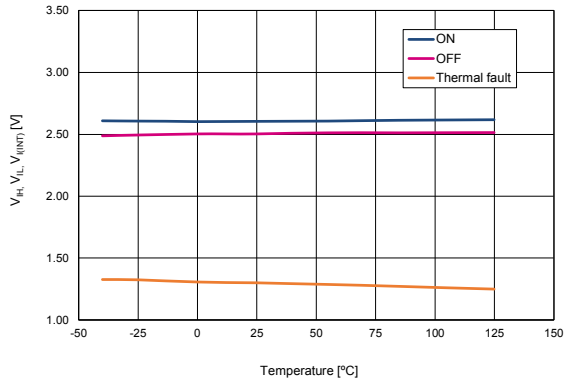


Figure 21. En/Fault pull-up voltage vs. temperature

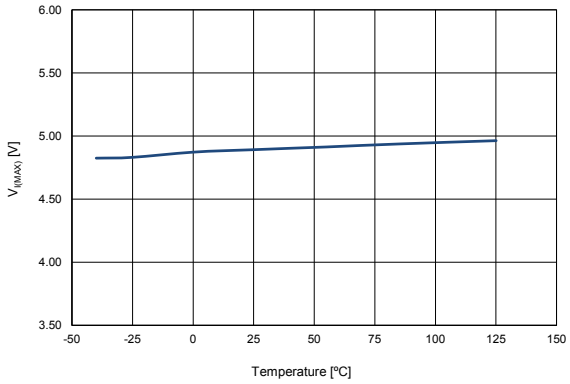


Figure 22. En/Fault pin current vs. temperature (En/Fault to GND)

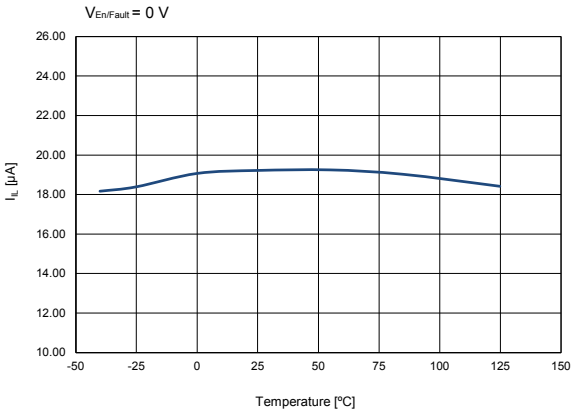


Figure 23. Soft-start time vs. temperature (no C_{dvdt})

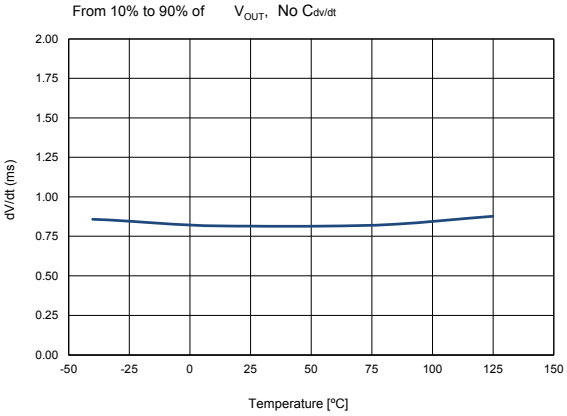
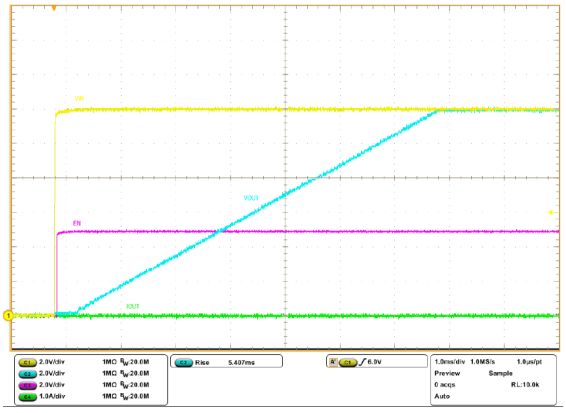


Figure 24. Start-up via input voltage (no load)



V_{IN}=from 0V to 12V, I_{OUT}= 0 mA , $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

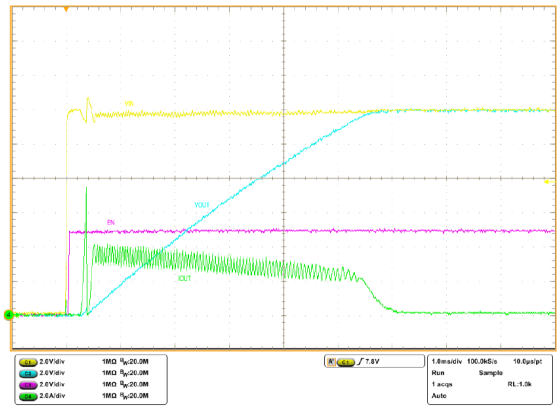
Figure 25. Start-up via En/Fault pin (no load)

$V_{En/Fault}$=from 0V to floating, I_{OUT}= 0 mA , $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 26. Start-up via input voltage (5 Ω load)

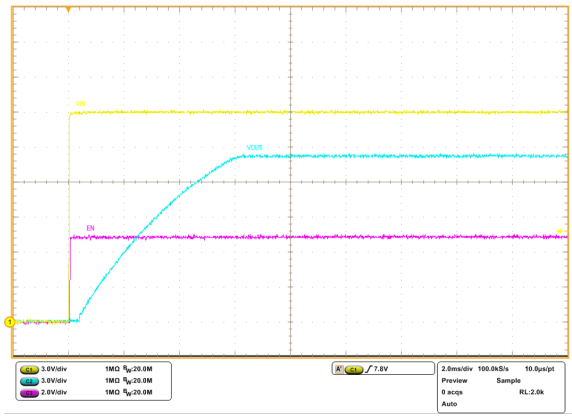
V_{IN}=from 0V to 12V, R_{LOAD}= 5 Ω, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 27. Start-up via input voltage (C_{OUT} = 1500 µF)



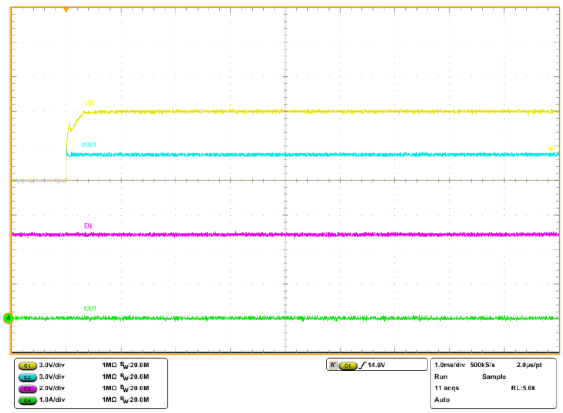
V_{IN}=from 0V to 12V, No load, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 1500 µF, R_{LIM} = 22Ω

Figure 28. Start-up into voltage clamp



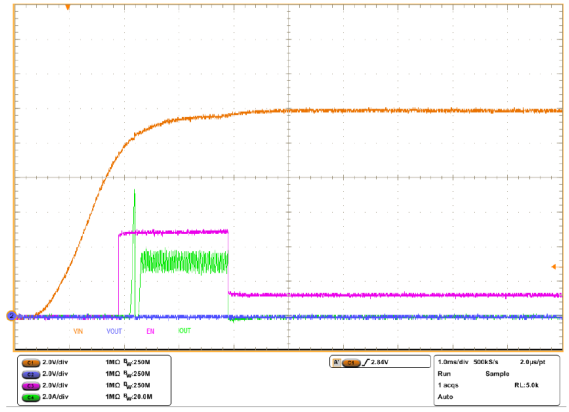
V_{IN}=from 0V to 18V, No load, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 29. Voltage clamp during operation



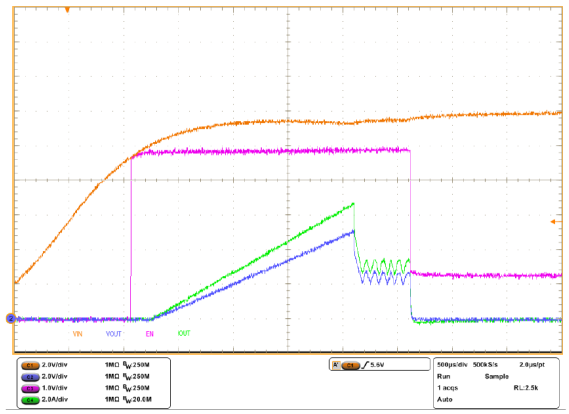
V_{IN}=from 12V to 18V, No load, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 30. Start-up into output short-circuit



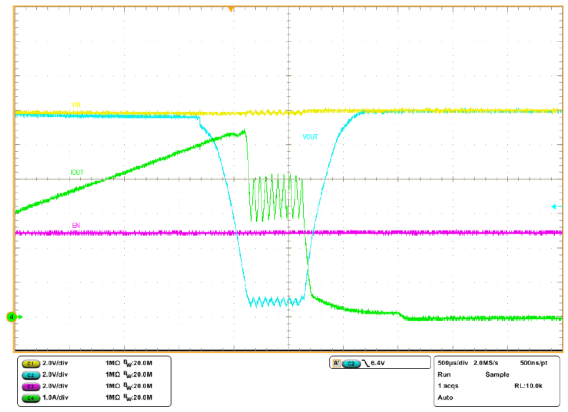
V_{IN}= 12V, V_{OUT} shorted to GND, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 31. Start-up into overload



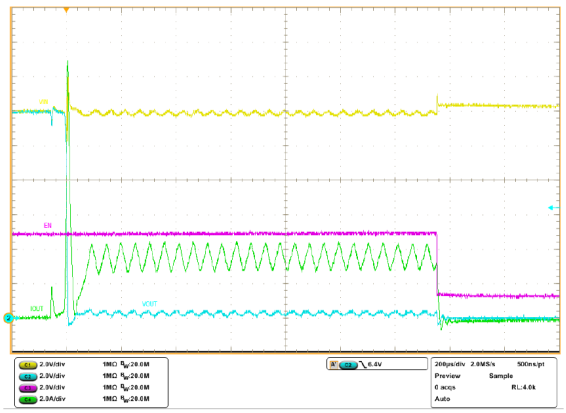
V_{IN}= 12V, R_{LOAD}= 0.75 Ω, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 32. Overcurrent protection during operation



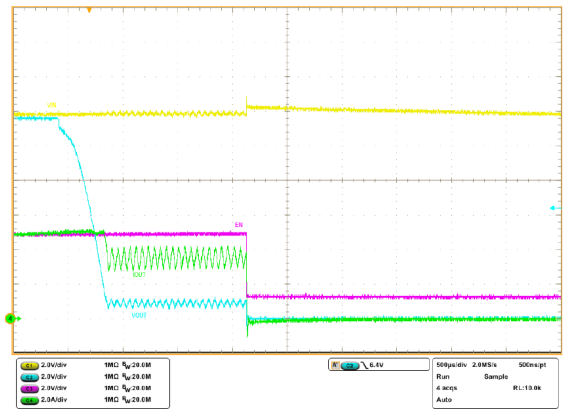
V_{IN}= 12V, I_{OUT} = from 0 to current limit, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 33. Output short-circuit during operation



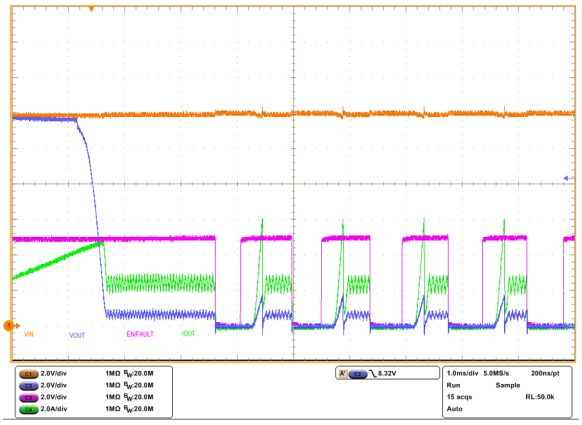
V_{IN}= 12V, V_{OUT} = from 12V to GND, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 34. Thermal shutdown (latched version)



V_{IN}= 12V, $C_{dV/dt}$= 220 pF, C_{IN}= 2.2 µF, C_{OUT}= 10 µF, R_{LIM} = 22Ω

Figure 35. Thermal shutdown (autoretry version)



V_{IN} = 12 V, $C_{dV/dt}$ = 220 pF, C_{IN} = 2.2 µF, C_{OUT} = 10 µF, R_{LIM} = 22 Ω

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 TSOT23-8L package information

Figure 36. TSOT23-8L package outline

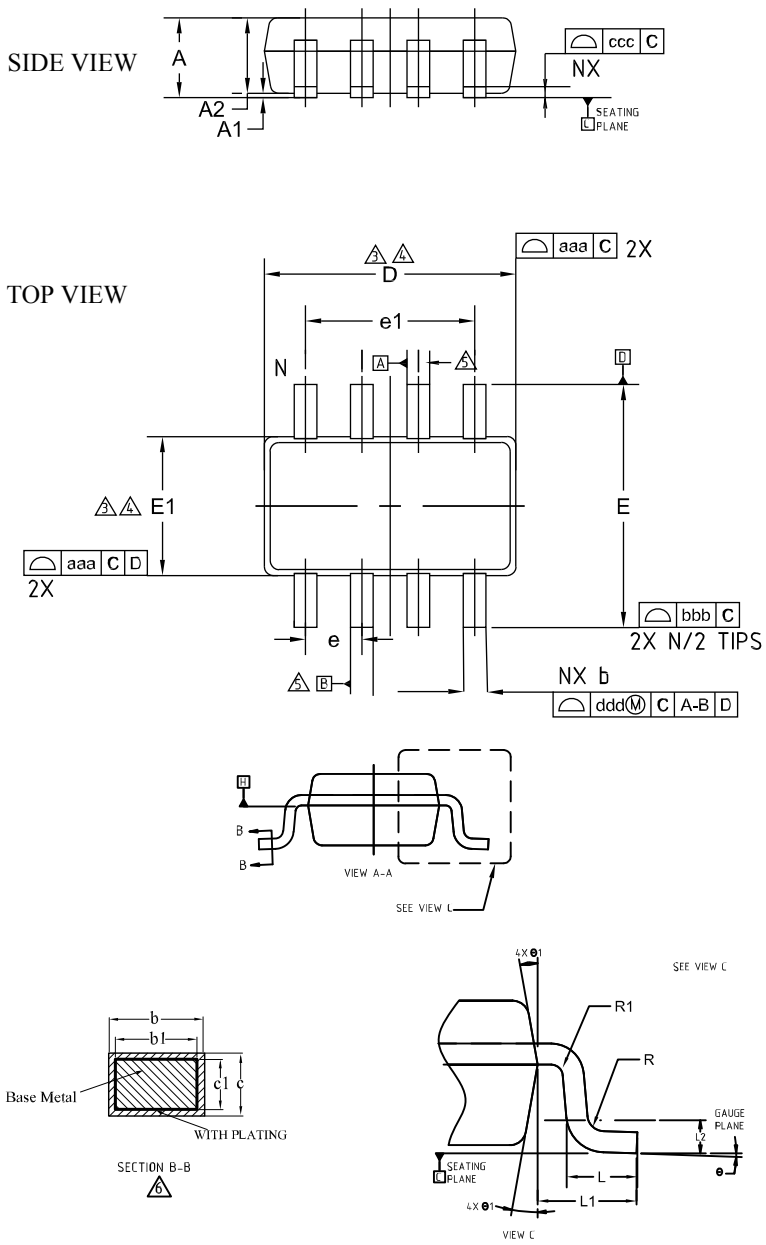
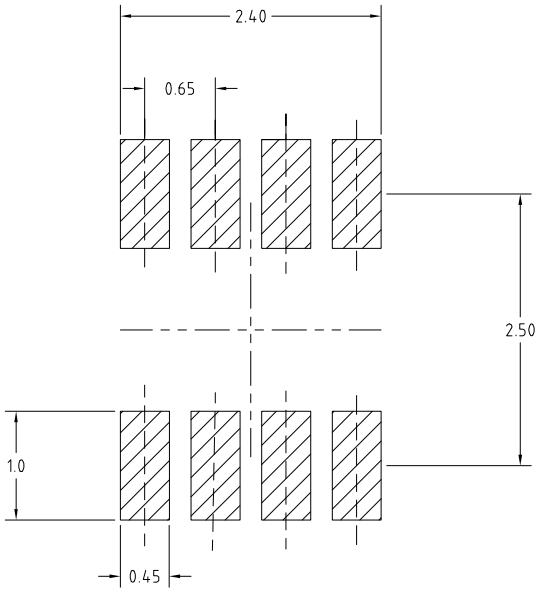


Table 9. **TSOT23-8L mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1
A1	0.01	0.05	0.1
A2	0.84	0.87	0.9
b	0.22	-	0.36
b1	0.22	0.26	0.3
c	0.12	0.15	0.2
c1	0.08	0.13	0.16
D	-	2.90 BSC	-
E	-	2.80 BSC	-
E1	-	1.60 BSC	-
e	-	0.65 BSC	-
e1	-	1.95 BSC	-
L	0.3	0.4	0.5
L1	-	0.60 BSC	-
L2	-	0.25 BSC	-
R	0.1	-	-
R1	0.1	-	0.25
Θ	0	4°	8°
Θ1	4°	10°	12°
Tolerance of form and position			
aaa	0.15		
bbb	0.25		
ccc	0.1		
ddd	0.13		
N	8		
ND	4		

Figure 37. **TSOT23-8L recommended footprint**



8.2 DFN10 (3 x 3 mm) package information

Figure 38. **DFN10 (3 x 3 mm) package outline**

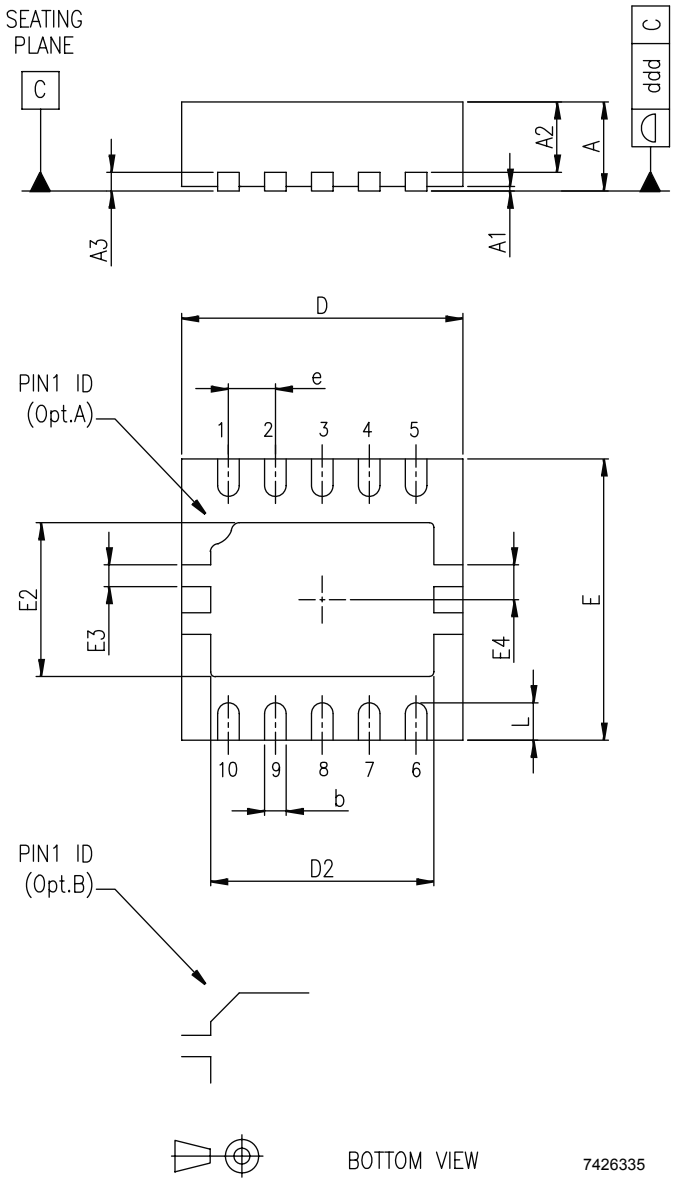
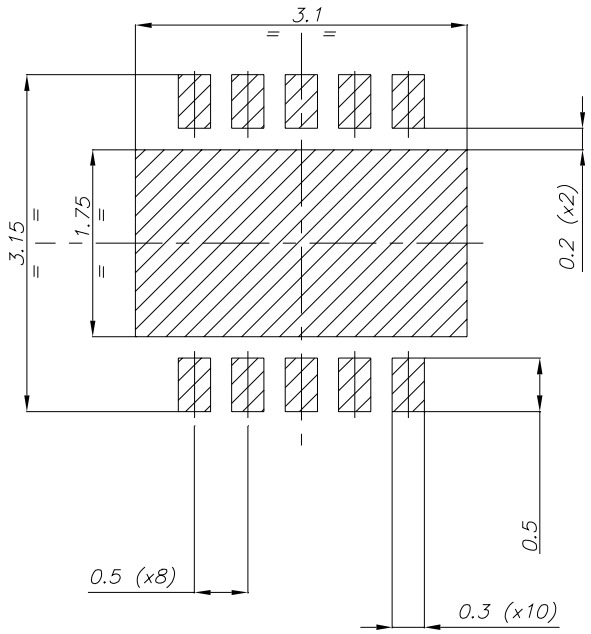


Table 10. DFN10 (3 x 3 mm) mechanical data

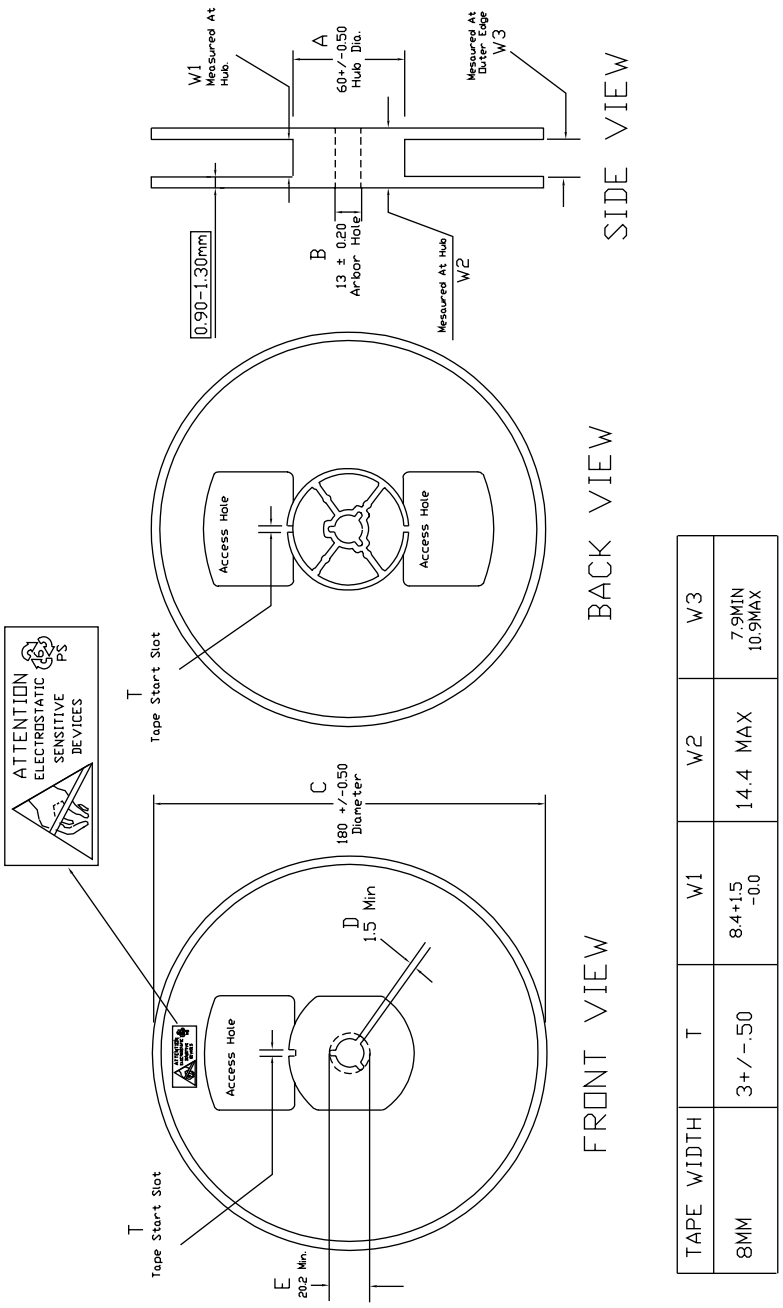
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	
A2		0.70	
A3		0.20	
b	0.18	0.23	0.30
D	2.85	3.00	3.15
D2	2.23	2.38	2.52
E	2.85	3.00	3.15
E2	1.49	1.64	1.75
E3	0.230		
E4	0.365		
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 39. DFN10 (3 x 3 mm) recommended footprint



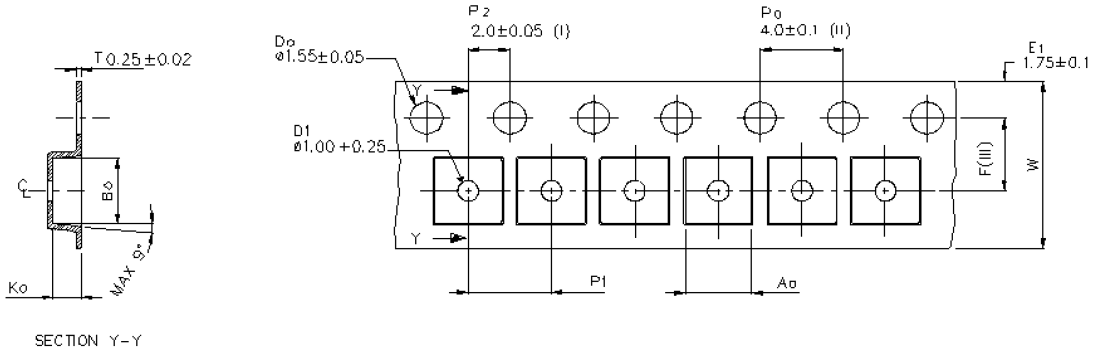
8.3 TSOT23-8L packing information

Figure 40. **TSOT23-8L reel drawing outline**



TAPE WIDTH	T	W1	W2	W3
8MM	3+/-.50	8.4+1.5 -0.0	14.4 MAX	7.9MIN 10.9MAX

Figure 41. **TSOT23-8L carrier tape**

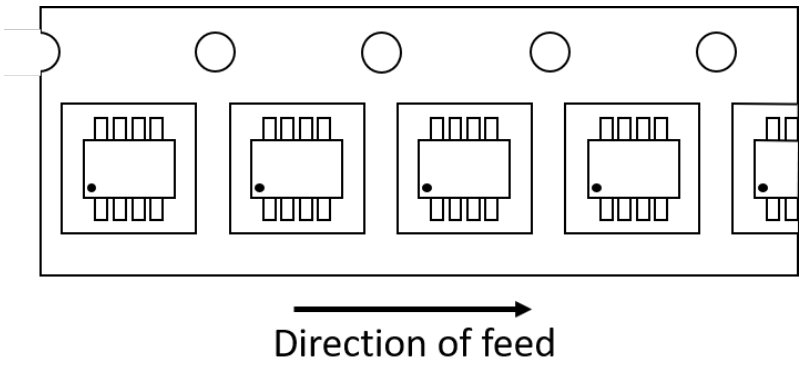


Ao	3.23 +/−0.10
Bo	3.17 +/−0.10
Ko	1.37 +/−0.10
F	3.50 +/−0.05
P1	4.00 +/−0.10
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max. 10^{6} OHM/SR

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 42. **TSOT23-8L device orientation in tape**



8.4 DFN10 (3 x 3 mm) packing information

Figure 43. **DFN10 (3 x 3 mm) reel drawing outline**

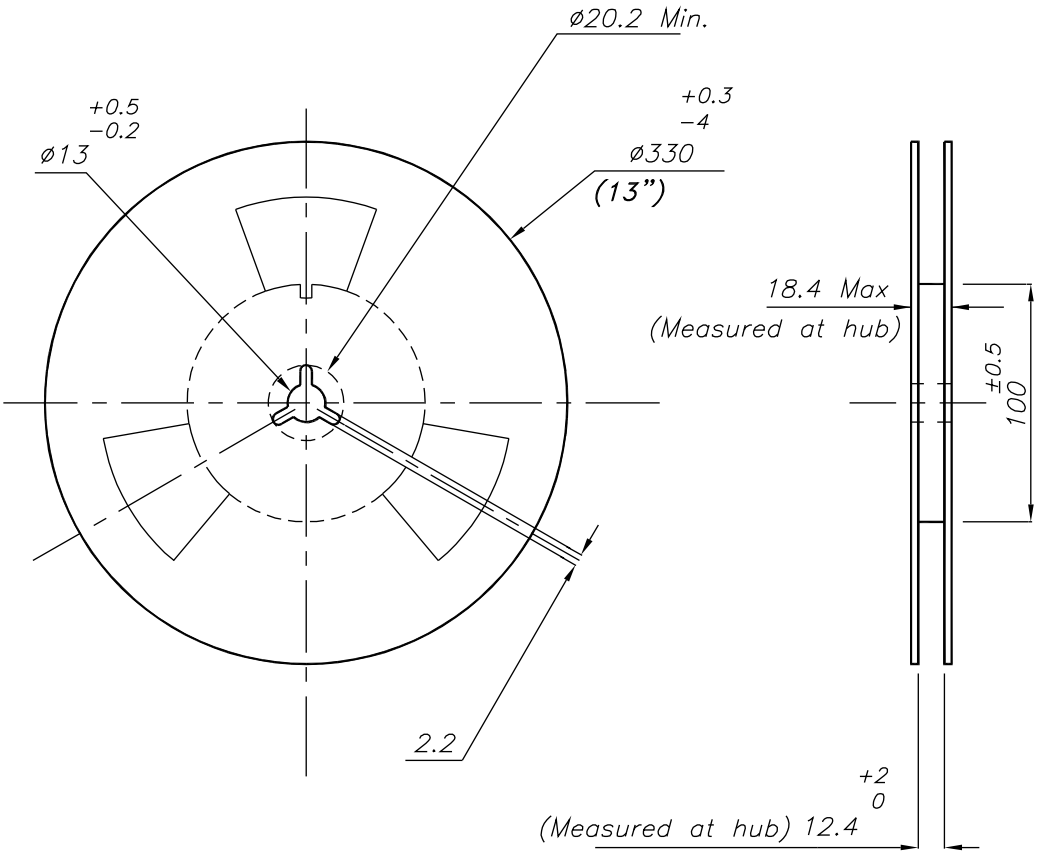
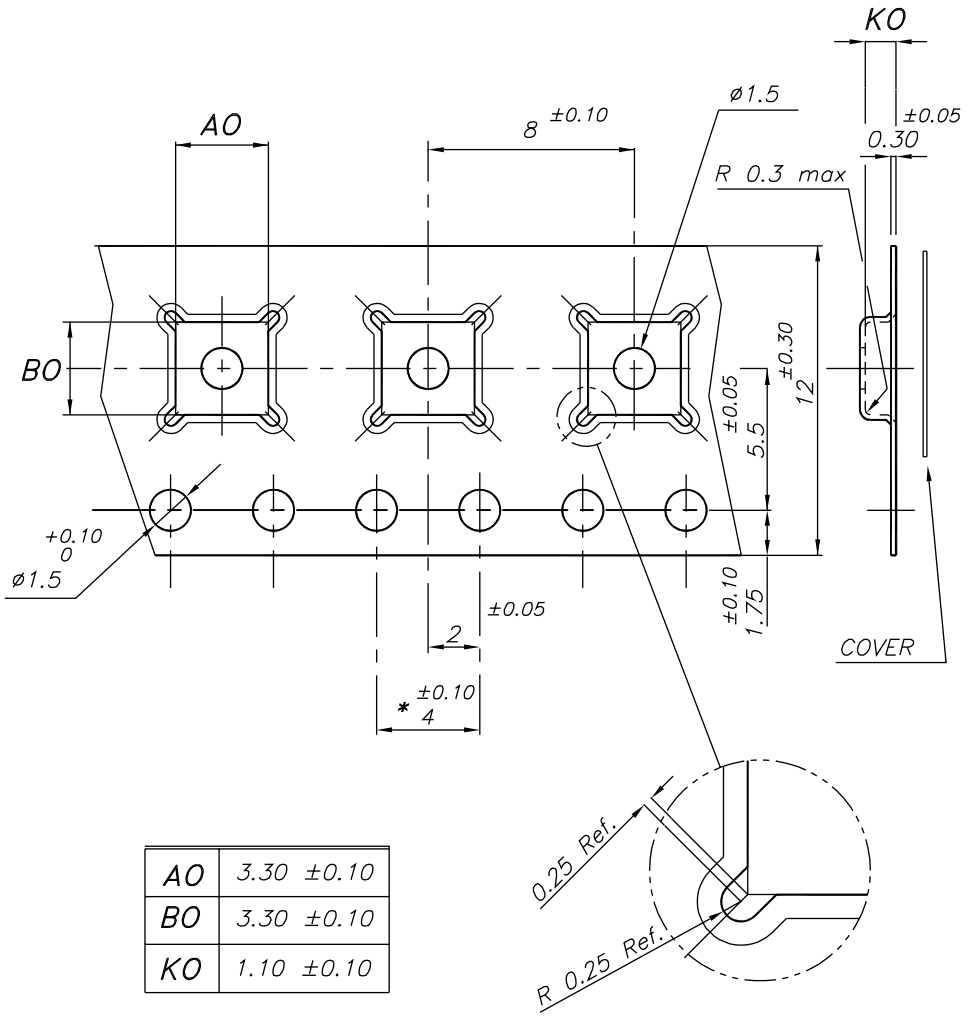
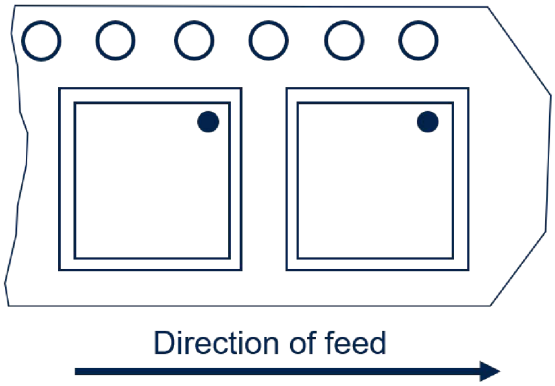


Figure 44. **DFN10 (3 x 3 mm) carrier tape**



AO	3.30 ±0.10
BO	3.30 ±0.10
KO	1.10 ±0.10

Figure 45. **DFN10 (3 x 3 mm) device orientation in tape**



9 Ordering information

Table 11. **Order codes**

Order code	Package	Packaging	Marking	Thermal protection
STEF12SGR	TSOT23-8	Tape and reel	12SL	Latch-off
STEF12SAGR			12HA	Autoretry
STEF12SPUR	DFN10-3x3		12SLP	Latch-off
STEF12SAPUR			12HA	Autoretry

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
17-Dec-2019	1	Initial release.
29-May-2020	2	Updated Figure 1, $V_{I(INT)}$ max. value in Table 5, Section 6.7 En/Fault pin, Section 6.9 Application suggestions and PCB layout guidelines and Figure 33. Added row R_{Lim} parameter in Table 4 and new order code STEF12SAPUR in Table 11.
25-Aug-2020	3	Updated Table 11. Order codes.
06-Oct-2021	4	Added new Section 8.3 TSOT23-8L packing information and Section 8.4 DFN10 (3 x 3 mm) packing information.

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