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# FDMC8015L

## N-Channel Power Trench® MOSFET

40 V, 18 A, 26 mΩ

### Features

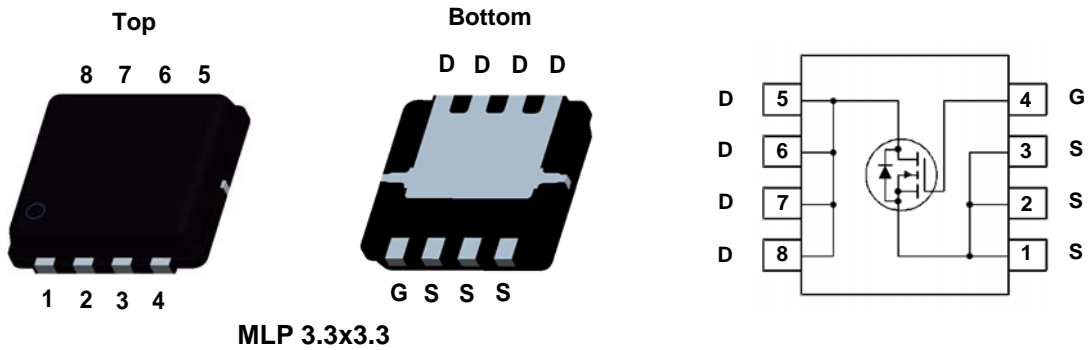
- Max  $r_{DS(on)}$  = 26 mΩ at  $V_{GS} = 10$  V,  $I_D = 7$  A
- Max  $r_{DS(on)}$  = 36 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 6$  A
- Low Profile - 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- Load Switch
- Motor Bridge Switch



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol         | Parameter  | Ratings     | Units            |
|----------------|--|-------------|------------------|
| $V_{DS}$       | Drain to Source Voltage  | 40          | V                |
| $V_{GS}$       | Gate to Source Voltage   | ±20         | V                |
| $I_D$          | Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$ | 18          | A                |
|                | -Continuous (Silicon limited) $T_C = 25^\circ\text{C}$               | 22          |                  |
|                | -Continuous $T_A = 25^\circ\text{C}$ (Note 1a)                       | 7           |                  |
|                | -Pulsed  | 30          |                  |
| $E_{AS}$       | Single Pulse Avalanche Energy (Note 3)                               | 32          | mJ               |
| $P_D$          | Power Dissipation $T_C = 25^\circ\text{C}$                           | 24          | W                |
|                | Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)                 | 2.3         |                  |
| $T_J, T_{STG}$ | Operating and Storage Junction Temperature Range                     | -55 to +150 | $^\circ\text{C}$ |

### Thermal Characteristics

|                 |   |     |                    |
|-----------------|---|-----|--------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case              | 5.1 | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53  |                    |

### Package Marking and Ordering Information

| Device Marking | Device    | Package  | Reel Size | Tape Width | Quantity   |
|----------------|-----------|----------|-----------|------------|------------|
| FDMC8015L      | FDMC8015L | Power 33 | 13"       | 12 mm      | 3000 units |

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

### Off Characteristics

|                                      |   |   |    |    |           |                      |
|--------------------------------------|---|---|----|----|-----------|----------------------|
| $BV_{DSS}$                           | Drain to Source Breakdown Voltage         | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$                    | 40 |    |           | V                    |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ |    | 36 |           | mV/ $^\circ\text{C}$ |
| $I_{DSS}$                            | Zero Gate Voltage Drain Current           | $V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$                            |    |    | 1         | $\mu\text{A}$        |
| $I_{GSS}$                            | Gate to Source Leakage Current            | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$                        |    |    | $\pm 100$ | nA                   |

### On Characteristics

|  |  |   |   |      |    |                      |
|--|--|---|---|------|----|----------------------|
| $V_{GS(th)}$                           | Gate to Source Threshold Voltage                         | $V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$                              | 1 | 1.8  | 3  | V                    |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$       |   | -6   |    | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$                           | Static Drain to Source On Resistance                     | $V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$                                     |   | 19.7 | 26 | m $\Omega$           |
|  |  | $V_{GS} = 4.5\text{ V}$ , $I_D = 6\text{ A}$                                    |   | 24   | 36 |                      |
|  |  | $V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$ |   | 29   | 39 |                      |
| $g_{FS}$                               | Forward Transconductance                                 | $V_{DD} = 5\text{ V}$ , $I_D = 7\text{ A}$                                      |   | 30   |    | S                    |

### Dynamic Characteristics

|            |                              |  |  |     |     |          |
|------------|------------------------------|--|--|-----|-----|----------|
| $C_{iss}$  | Input Capacitance            | $V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ ,<br>$f = 1\text{ MHz}$ |  | 710 | 945 | pF       |
| $C_{oss}$  | Output Capacitance           |  |  | 94  | 125 | pF       |
| $C_{riss}$ | Reverse Transfer Capacitance |  |  | 58  | 90  | pF       |
| $R_g$      | Gate Resistance              |  |  | 1.2 |     | $\Omega$ |

### Switching Characteristics

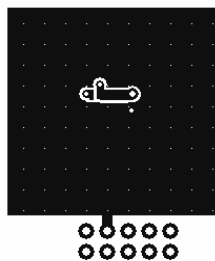
|              |                               |   |  |     |      |    |    |
|--------------|-------------------------------|---|--|-----|------|----|----|
| $t_{d(on)}$  | Turn-On Delay Time            | $V_{DD} = 20\text{ V}$ , $I_D = 7\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$ |  | 6.3 | 13   | ns |    |
| $t_r$        | Rise Time                     |   |  | 1.9 | 10   | ns |    |
| $t_{d(off)}$ | Turn-Off Delay Time           |   |  | 18  | 33   | ns |    |
| $t_f$        | Fall Time                     |   |  | 1.7 | 10   | ns |    |
| $Q_{g(TOT)}$ | Total Gate Charge             |   | $V_{GS} = 0\text{ V to } 10\text{ V}$          |     | 13.6 | 19 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge             | $V_{GS} = 0\text{ V to } 4.5\text{ V}$  | $V_{DD} = 20\text{ V}$ ,<br>$I_D = 7\text{ A}$ |     | 6.6  | 10 | nC |
| $Q_{gs}$     | Total Gate Charge             |   |  |     | 1.9  |    | nC |
| $Q_{gd}$     | Gate to Drain "Miller" Charge |   |  |     | 2.5  |    | nC |

### Drain-Source Diode Characteristics

|          |                                       |   |  |      |     |    |
|----------|---------------------------------------|---|--|------|-----|----|
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}$ , $I_S = 7\text{ A}$ (Note 2)     |  | 0.84 | 1.2 | V  |
|          |                                       | $V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)     |  | 0.76 | 1.1 |    |
| $t_{rr}$ | Reverse Recovery Time                 | $I_F = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ |  | 18   | 33  | ns |
| $Q_{rr}$ | Reverse Recovery Charge               |   |  | 8.6  | 18  | nC |

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53\text{ }^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 1\text{ mH}$ ,  $I_{AS} = 8\text{ A}$ ,  $V_{DD} = 36\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

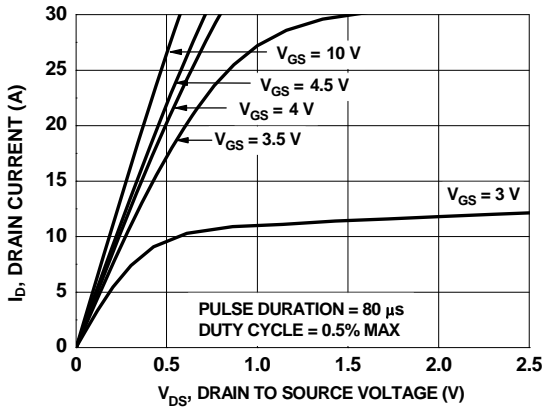


Figure 1. On Region Characteristics

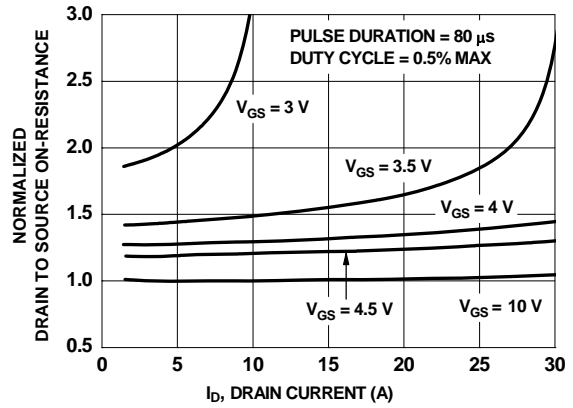


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

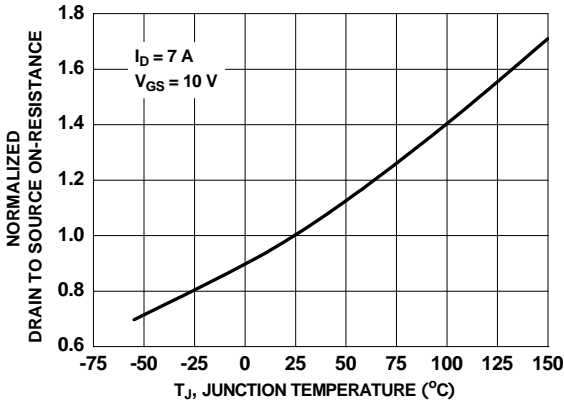


Figure 3. Normalized On Resistance vs Junction Temperature

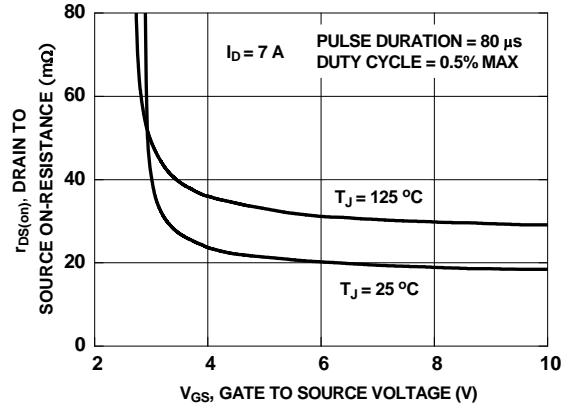


Figure 4. On-Resistance vs Gate to Source Voltage

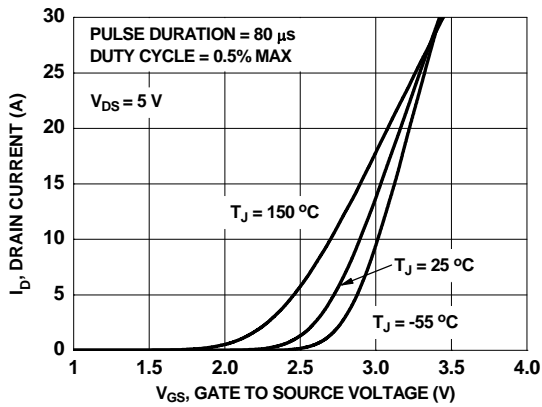


Figure 5. Transfer Characteristics

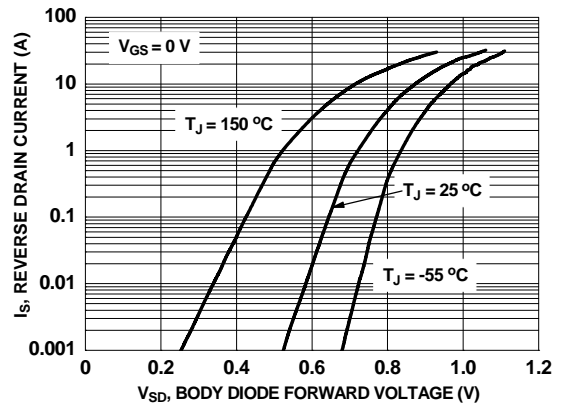
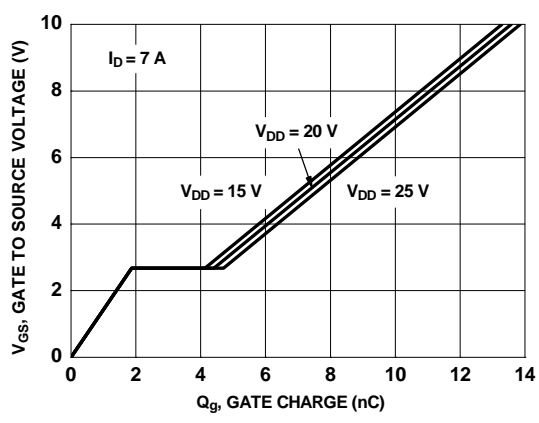
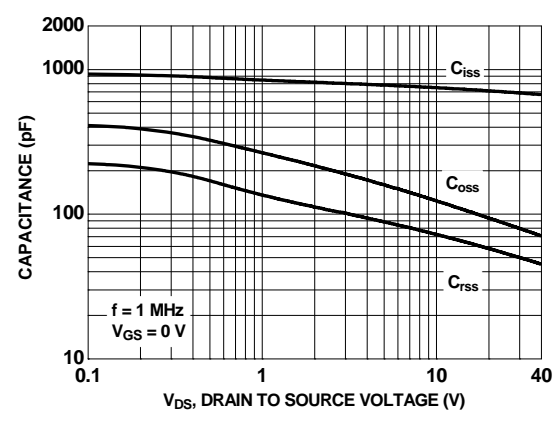


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

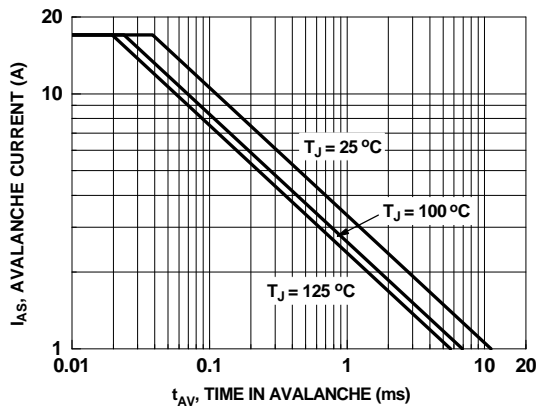
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



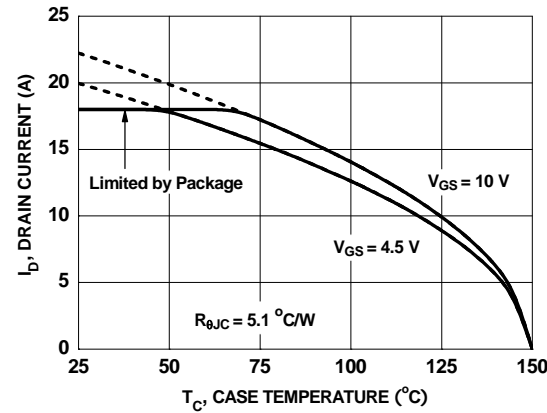
**Figure 7. Gate Charge Characteristics**



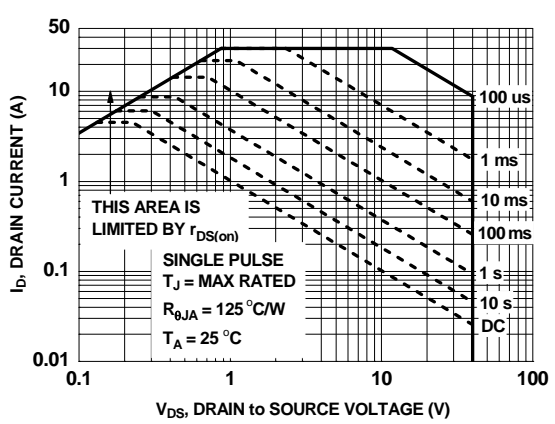
**Figure 8. Capacitance vs Drain to Source Voltage**



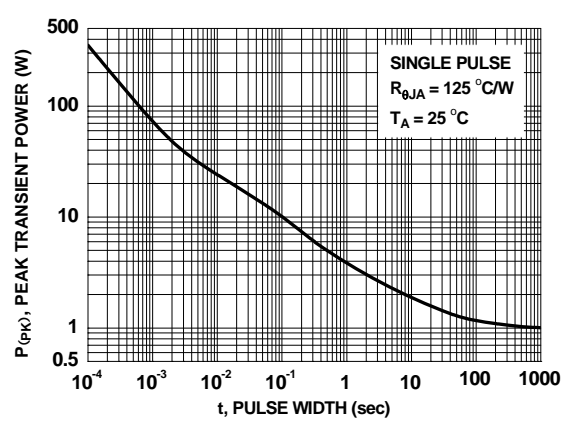
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

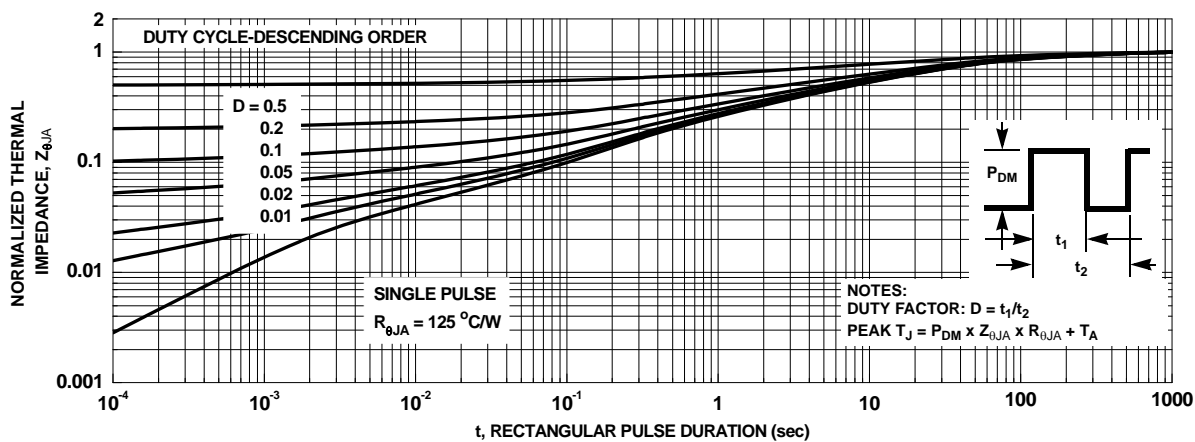


**Figure 11. Forward Bias Safe Operating Area**

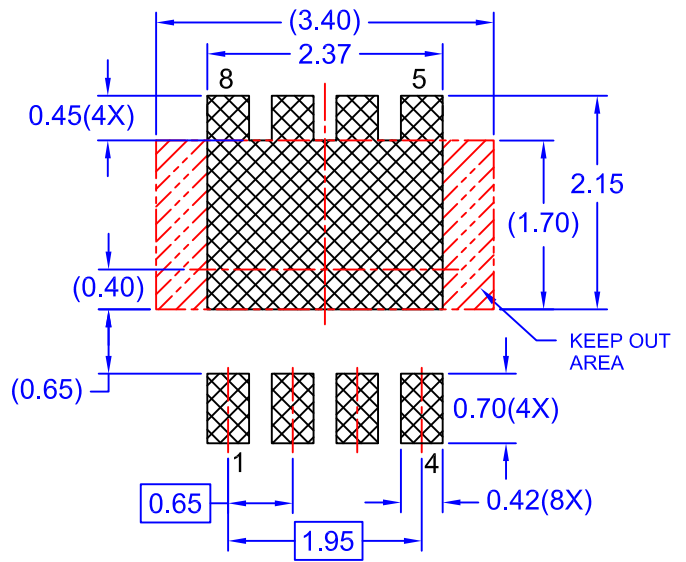
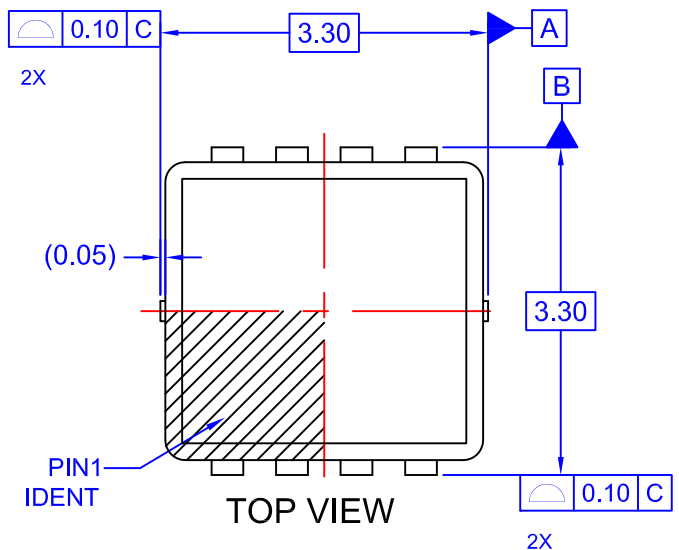


**Figure 12. Single Pulse Maximum Power Dissipation**

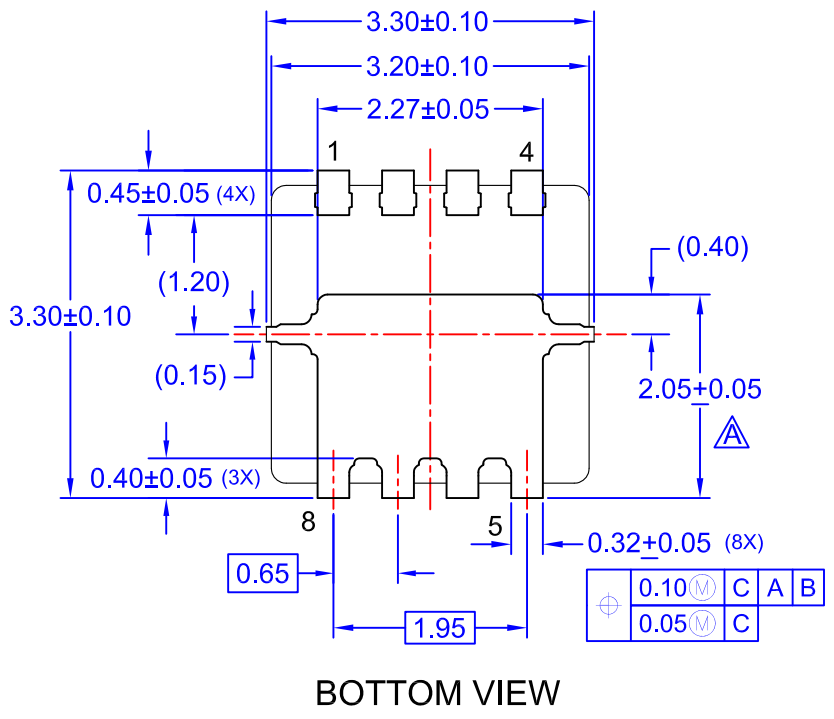
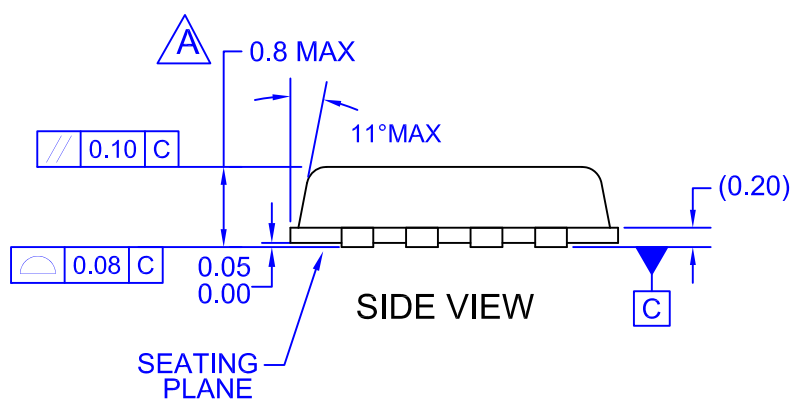
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



**RECOMMENDED LAND PATTERN**



- NOTES:**
- A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
  - D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
  - E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.
  - F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
  - G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
  - H. DRAWING FILENAME: MKT-MLP08Trev4.
  - I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.



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