

MOSFET – Power, Single N-Channel

60 V, 27.5 mΩ, 21 A

NVMFS5C680NL

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFS5C680NLWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State	$T_C = 25^\circ\text{C}$	I_D	21	A
		$T_C = 100^\circ\text{C}$		15	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25^\circ\text{C}$	P_D	24	W
		$T_C = 100^\circ\text{C}$		12	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	8.1	A
		$T_A = 100^\circ\text{C}$		5.7	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.4	W
		$T_A = 100^\circ\text{C}$		1.7	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$		I_{DM}	87	A
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			I_S	20	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 1.5 \text{ A}$)			E_{AS}	44.6	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

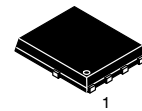
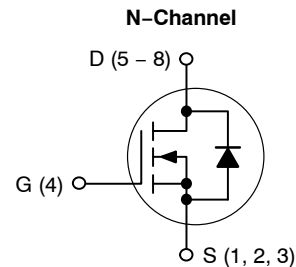
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

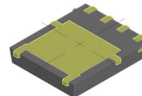
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	$R_{\theta JC}$	6.3	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	44	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	27.5 mΩ @ 10 V	21 A
	43.0 mΩ @ 4.5 V	

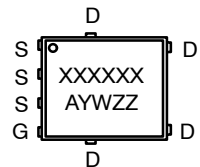


DFN5 (SO-8FL)
CASE 488AA
STYLE 1



DFNW5 (FULL-CUT SO8FL WF)
CASE 507BA

MARKING DIAGRAMS



XXXXXX = 5C680L (NVMFS5C680NL) or
680LWF (NVMFS5C680NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFS5C680NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C		10	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 13 μA	1.2		2.2	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		22.9	27.5	mΩ
		V _{GS} = 4.5 V, I _D = 7.5 A		35.8	43.0	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 10 A		20		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		330		pF
Output Capacitance	C _{oss}			172		
Reverse Transfer Capacitance	C _{rss}			5		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 7.5 A		5.8		nC
Threshold Gate Charge	Q _{G(TH)}			0.8		
Gate-to-Source Charge	Q _{GS}			1.3		
Gate-to-Drain Charge	Q _{GD}			0.6		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 7.5 A		2.7		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	t _{d(on)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 7.5 A, R _G = 1.0 Ω		5		ns
Rise Time	t _r			12.5		
Turn-Off Delay Time	t _{d(off)}			14		
Fall Time	t _f			2.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 7.5 A	T _J = 25°C		0.87	1.2	V
			T _J = 125°C		0.76		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 7.5 A		18		ns	
Charge Time	t _a			8.3			
Discharge Time	t _b			9.7			
Reverse Recovery Charge	Q _{RR}			7.5		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

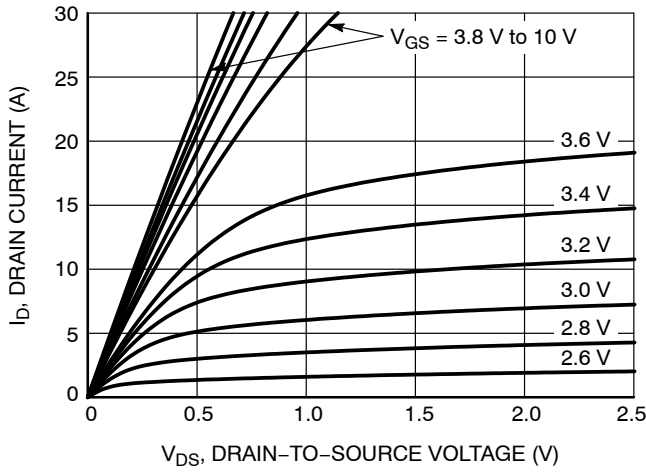


Figure 1. On-Region Characteristics

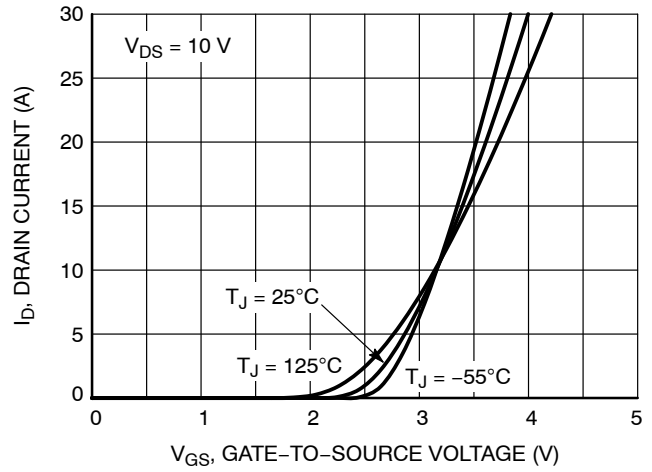


Figure 2. Transfer Characteristics

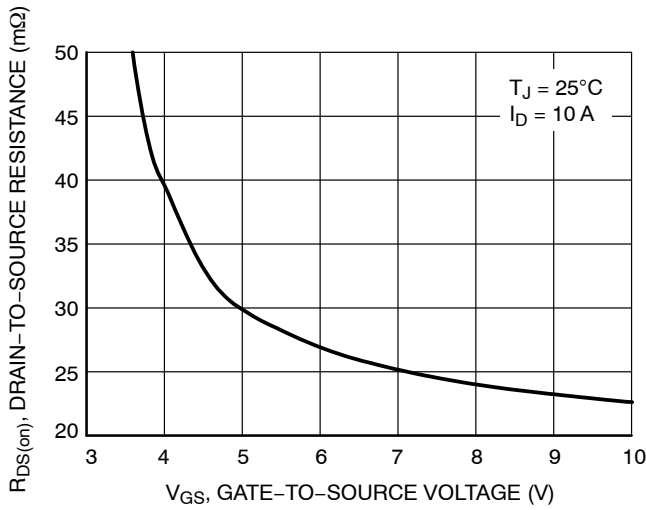


Figure 3. On-Resistance vs. Gate-to-Source Voltage

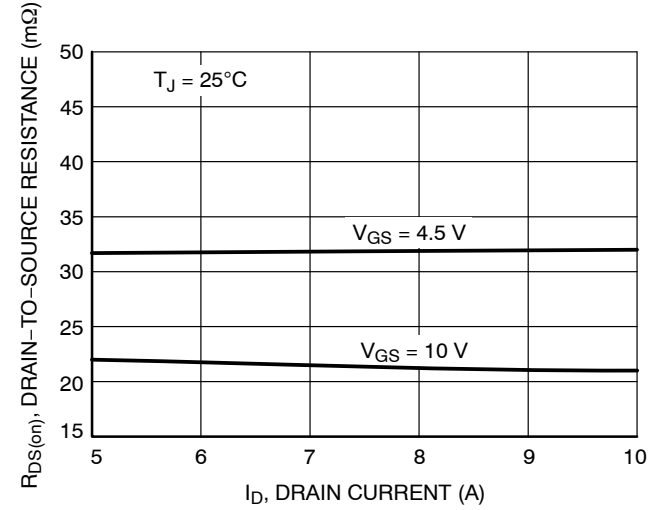


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

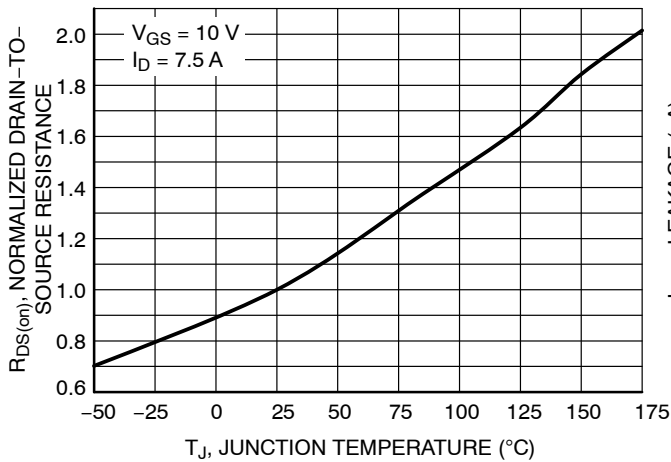


Figure 5. On-Resistance Variation with Temperature

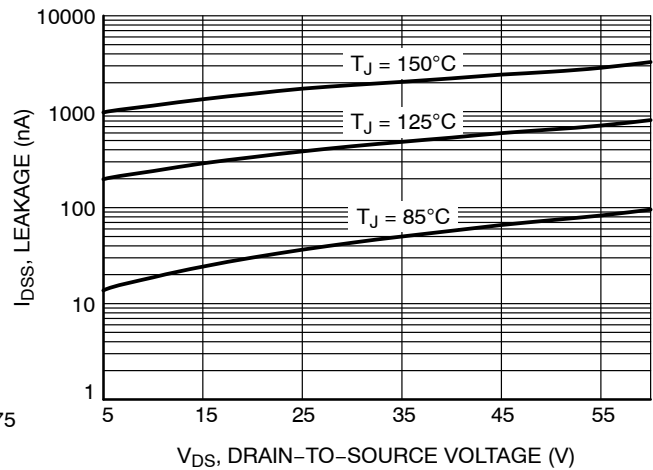


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

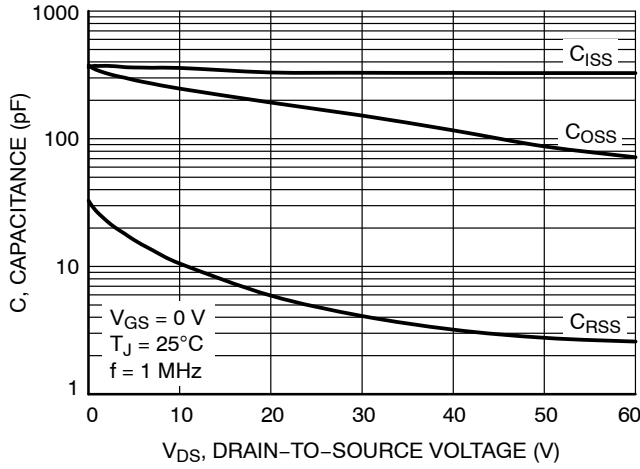


Figure 7. Capacitance Variation

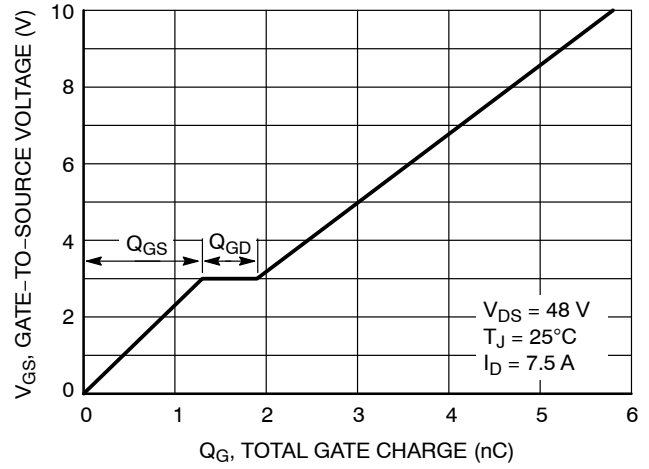


Figure 8. Gate-to-Source vs. Total Charge

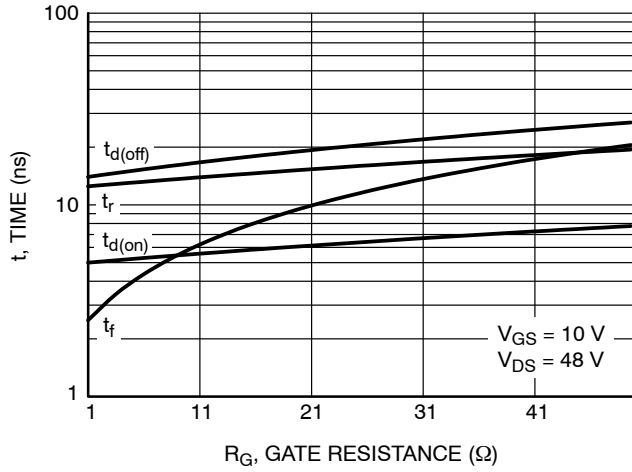


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

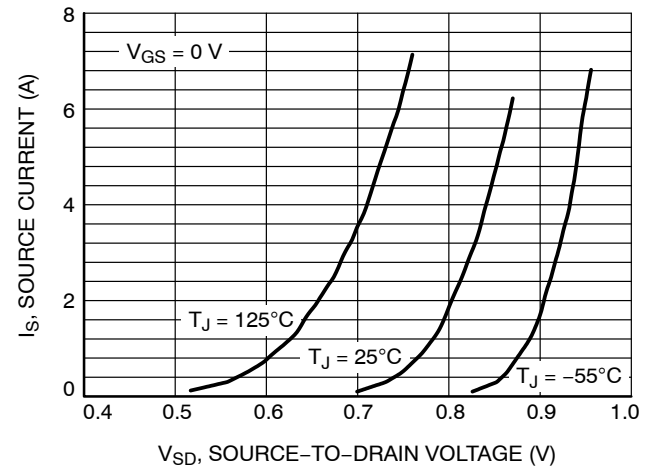


Figure 10. Diode Forward Voltage vs. Current

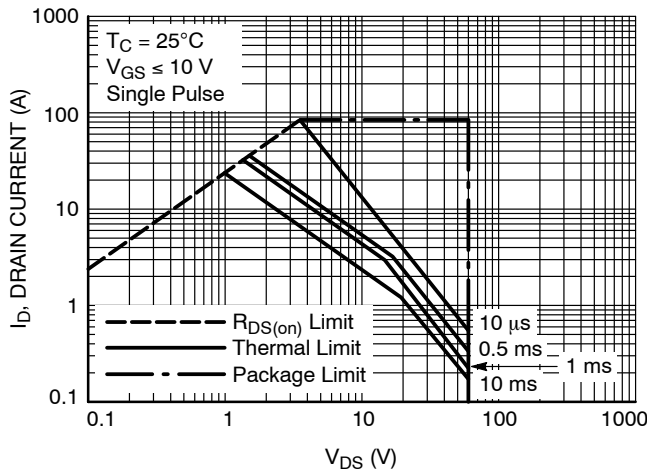


Figure 11. Maximum Rated Forward Biased Safe Operating Area

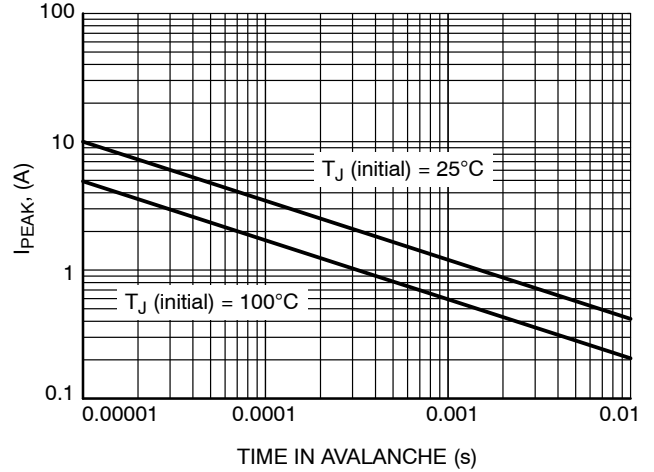


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C680NL

TYPICAL CHARACTERISTICS

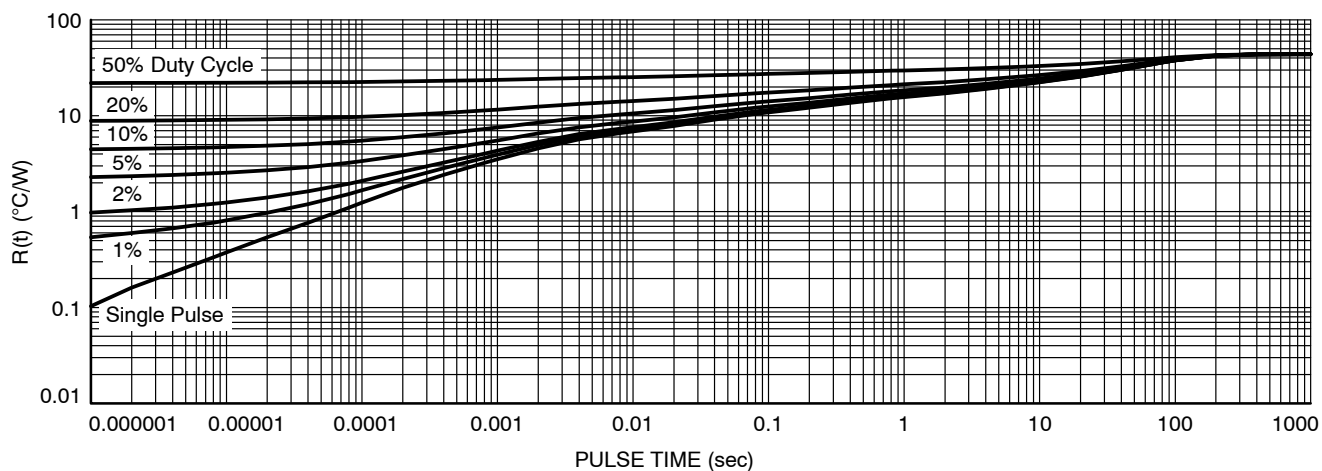


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C680NLT1G	5C680L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C680NLWFT1G	680LWF	DFNW5 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	—	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
theta	0°	—	12°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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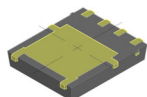
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

ON

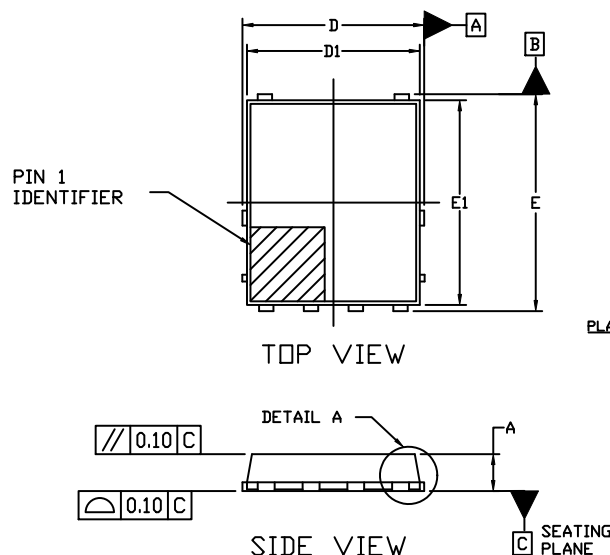


DFNW5 5x6 (FULL-CUT SO8FL WF)

CASE 507BA

ISSUE A

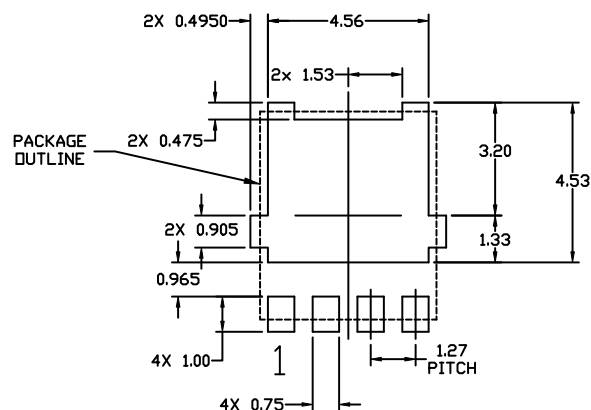
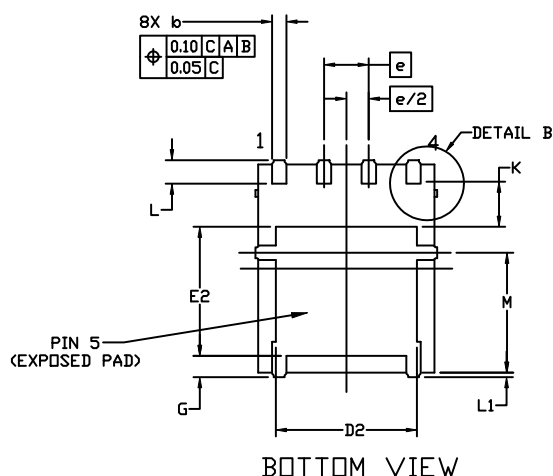
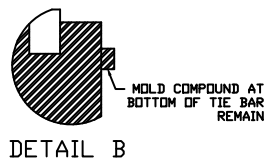
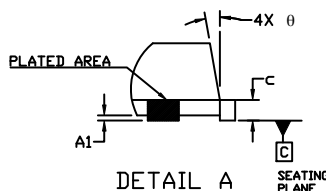
DATE 03 FEB 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

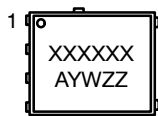
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L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED MOUNTING FOOTPRINT

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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