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ESD7382MUT5G

ESD Protection Diode

Micro-Packaged Diodes for ESD Protection

The ESD7382 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, it is suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Features

- Ultra-Low Capacitance: 0.37 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.60 mm x 0.30 mm
- Low Body Height: 0.3 mm
- Stand-off Voltage: 5.0 V
- Low Leakage
- Insertion Loss: 0.030 dBm
- Response Time is < 1 ns
- Low Dynamic Resistance < 1 Ω
- IEC61000-4-2 Level 4 ESD Protection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|--------------------------|-------------|------|
| IEC 61000-4-2 (ESD) | Contact Air | ±20 ±20 | kV |
| Total Power Dissipation on FR-5 Board (Note 1) @ $T_A = 25^\circ\text{C}$ | P_D | 250 | mW |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 400 | °C/W |
| Junction and Storage Temperature Range | T_J , T_{stg} | -40 to +125 | °C |
| Lead Solder Temperature – Maximum (10 Second Duration) | T_L | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.

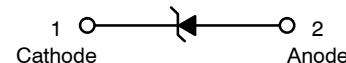
See Application Note AND8308/D for further description of survivability specs.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



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MARKING DIAGRAM

PIN 1



2 = Specific Device Code
(Rotated 270°)
M = Date Code



8:1 XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------------------------|---------------------|-----------------------|
| ESD7382MUT5G | X3DFN2 (Pb-Free) | 10,000 / Tape & Reel |
| ESD7382N2T5G (In Development) | X2DFN2 (Pb-Free) | 10,000 / Tape & Reel |

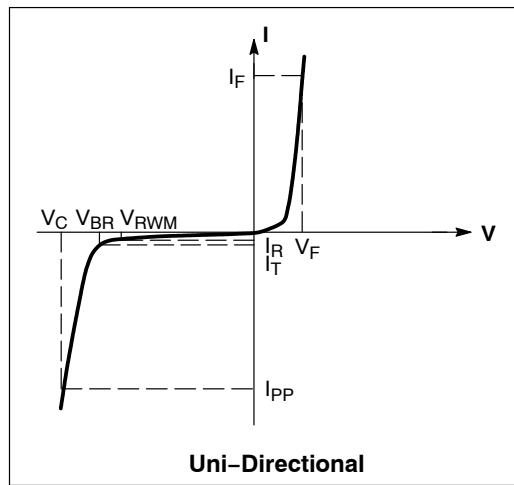
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------|---|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|-----------|--|---------------------|----------------|--------------|---------------|
| Reverse Working Voltage | V_{RWM} | | | | 5.0 | V |
| Breakdown Voltage (Note 2) | V_{BR} | $I_T = 1 \text{ mA}$ | 5.2 | | | V |
| Reverse Leakage Current | I_R | $V_{RWM} = 5.0 \text{ V}$ | | | 1.0 | μA |
| Clamping Voltage (Note 3) | V_C | $I_{PP} = 1 \text{ A}$ | | | 8.0 | V |
| Clamping Voltage (Note 3) | V_C | $I_{PP} = 3 \text{ A}$ | | | 10 | V |
| ESD Clamping Voltage | V_C | Per IEC61000-4-2 | See Figures 1 and 2 | | | |
| Junction Capacitance | C_J | $V_R = 0 \text{ V}, f = 1 \text{ MHz}$ $V_R = 0 \text{ V}, f < 1 \text{ GHz}$ | | 0.37 0.25 | 0.55 0.55 | pF |
| Dynamic Resistance | R_{DYN} | TLP Pulse | | 0.32 | | Ω |
| Insertion Loss | | $f = 1 \text{ MHz}$ $f = 8.5 \text{ GHz}$ | | 0.030 0.573 | | dB |

2. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
3. Non-repetitive current pulse at $T_A = 25^\circ\text{C}$, per IEC61000-4-5 waveform.

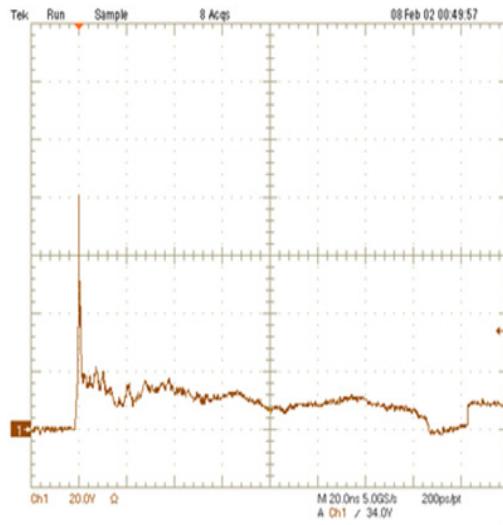


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000-4-2

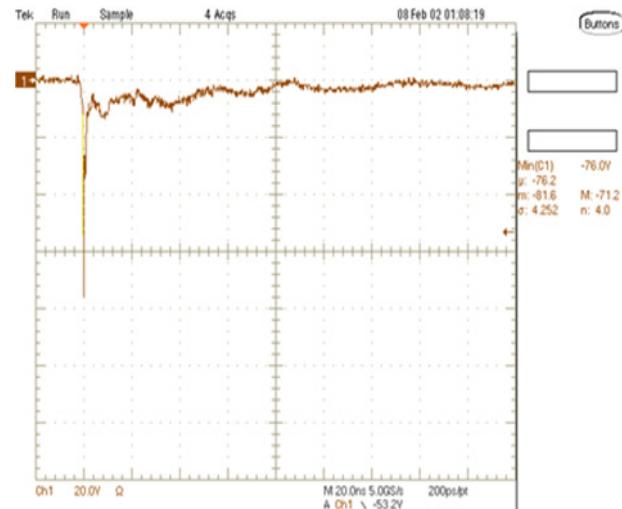
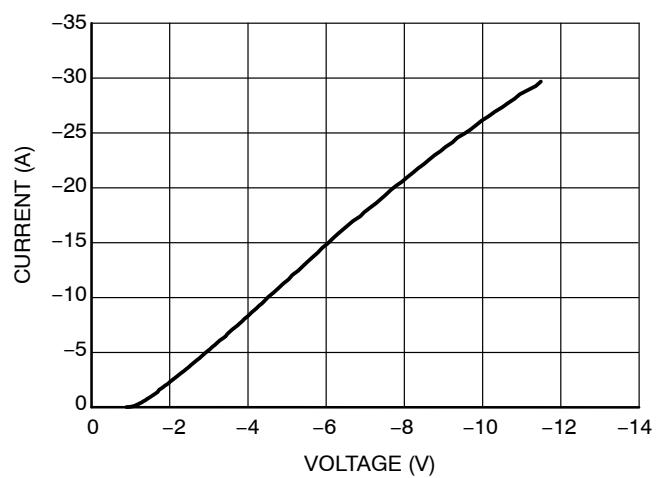
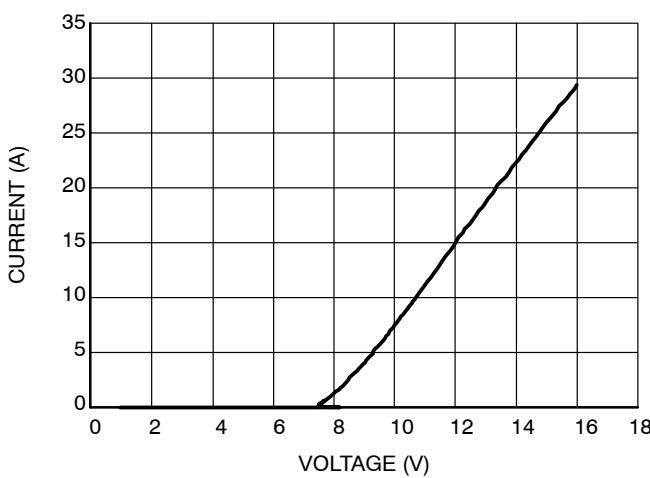
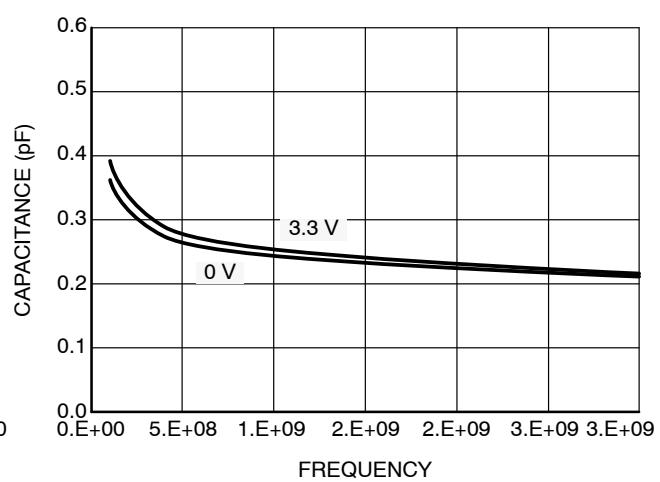
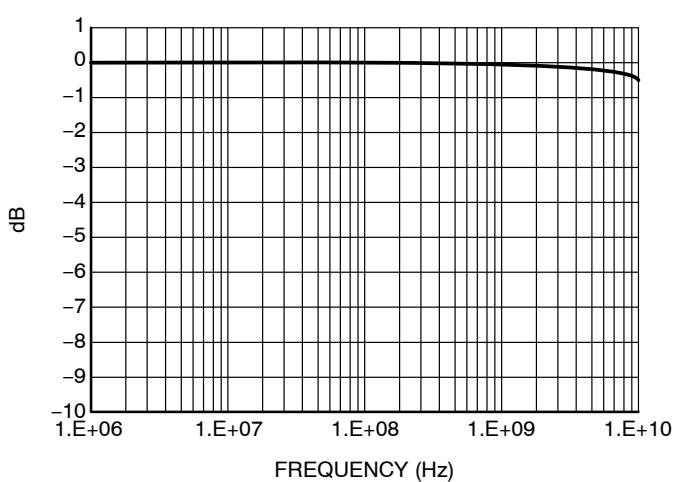
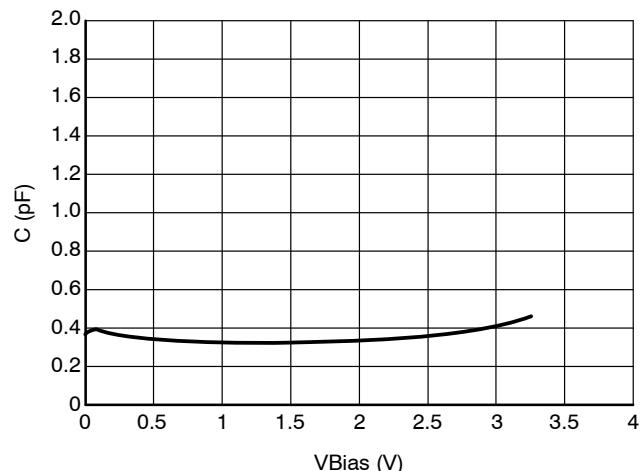
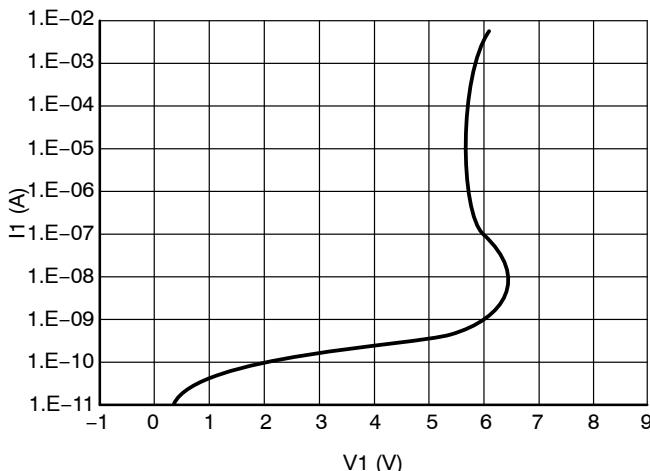


Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000-4-2

ESD7382MUT5G



ESD7382MUT5G

IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

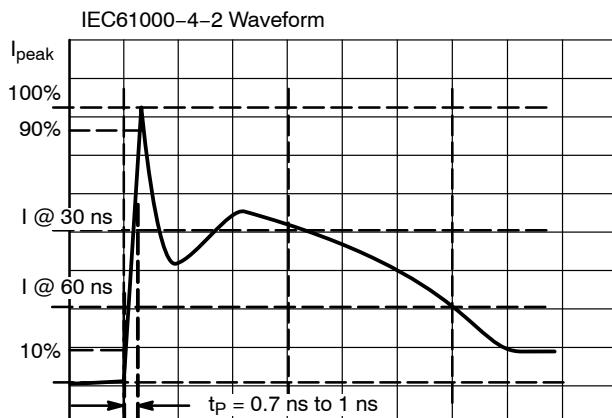


Figure 9. IEC61000-4-2 Spec

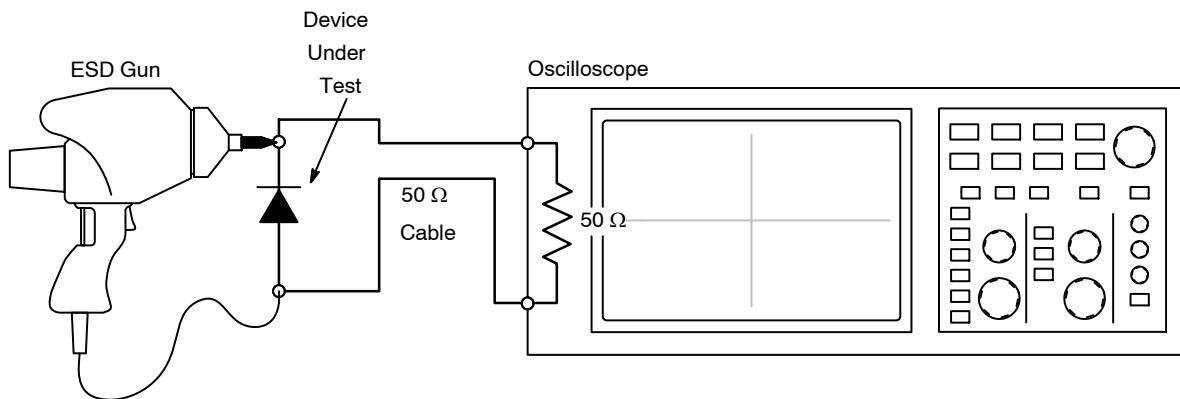


Figure 10. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage

at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

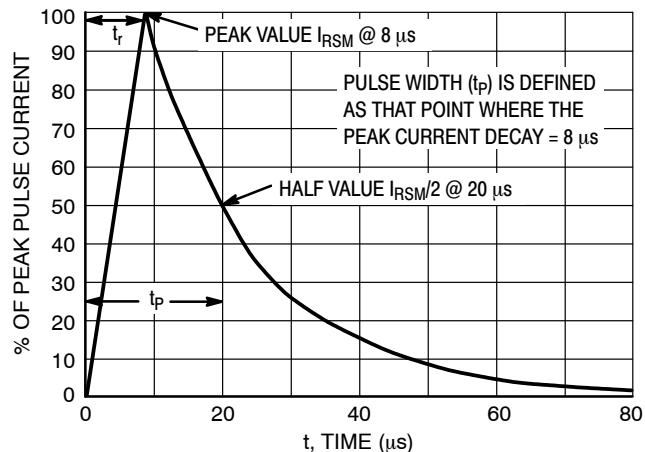
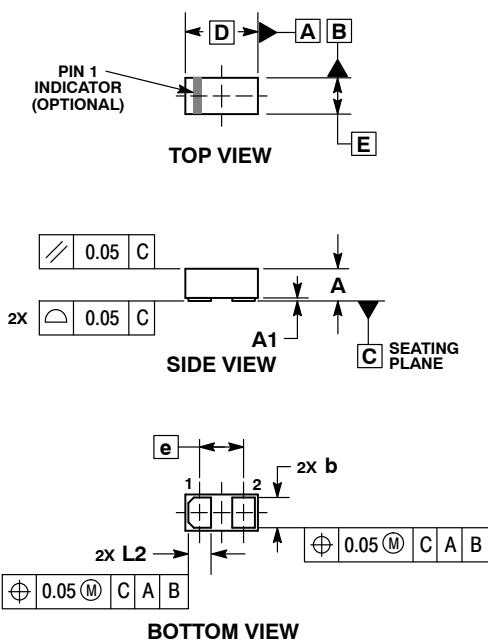


Figure 11. 8 X 20 μ s Pulse Waveform

PACKAGE DIMENSIONS

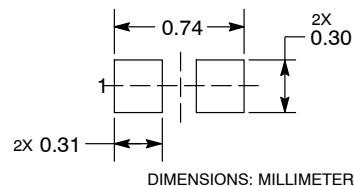
X3DFN2, 0.62 x 0.32, 0.355P, (0201)
 CASE 152AF
 ISSUE A



NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

| MILLIMETERS | | |
|-------------|-----------|------|
| DIM | MIN | MAX |
| A | 0.25 | 0.33 |
| A1 | --- | 0.05 |
| b | 0.22 | 0.28 |
| D | 0.58 | 0.66 |
| E | 0.28 | 0.36 |
| e | 0.355 BSC | |
| L2 | 0.17 | 0.23 |

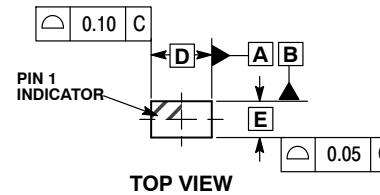
**RECOMMENDED
 MOUNTING FOOTPRINT***



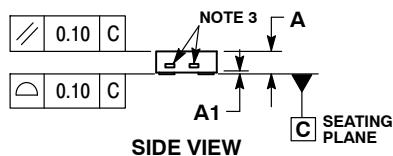
See Application Note AND8398/D for more mounting details

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

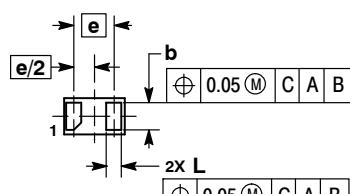
PACKAGE DIMENSIONS

X2DFN2 1.0 x 0.6, 0.65P
CASE 714AB
ISSUE A

TOP VIEW



SIDE VIEW

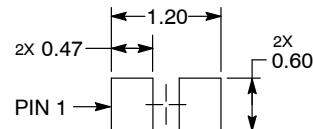


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.34 | 0.40 |
| A1 | --- | 0.05 |
| b | 0.45 | 0.55 |
| D | 1.00 BSC | |
| E | 0.60 BSC | |
| e | 0.65 BSC | |
| L | 0.20 | 0.30 |

RECOMMENDED
SOLDER FOOTPRINT*

DIMENSIONS: MILLIMETERS

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "C" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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