LDO Regulator, Low Noise (8 µV$_{RMS}$), ADJ/FIX

38 V, 150 mA

NCP731

The NCP731 device is based on unique combination of features – very low noise, low quiescent current, fast transient response and high input and output voltage ranges. The NCP731 is CMOS LDO regulator designed for up to 38 V input voltage and 150 mA output current. Very low noise (8 µV$_{RMS}$) makes this device an ideal solution for application where clean voltage rails are critical for system performance (power operational amplifiers, analog–to–digital / digital–to–analog converters and other precision analog circuitry).

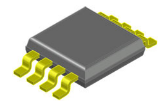
Internal short circuit and over temperature protections saves the device against overload conditions.

Features

- Operating Input Voltage Range: 2.7 V to 38 V
- Output Voltage Adjustable Range: 1.2 V to 35 V
- Fixed Output Voltage Versions: 3.3 V and 5.0 V (other voltage versions on request)
- Very Low Noise: 8 µV$_{RMS}$ (10 Hz to 100 kHz)
- Low Quiescent Current: 48 µA typ.
- Low Shutdown Current: 100 nA typ.
- Low Dropout: 290 mV typ. at 150 mA
- Output Voltage Accuracy ±0.6% (25°C)
- Programmable Soft Start Circuit
- Stable with Small 1 µF Ceramic Capacitors
- Over–Current and Thermal Shutdown Protections
- Available in Micro–8 EP Package
- Device is Pb–Free and RoHS Compliant

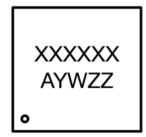
Typical Applications

- Supply Rails for OpAmps, ADCs, DACs and other Precision Analog Circuitry and Audio
- Post DC–DC Converter Regulation and Ripple Filtering
- Test and Measurement
- Industrial Instrumentation
- Metering
- Battery Powered Devices



MSOP8 EP 3x3
CASE 846AT

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

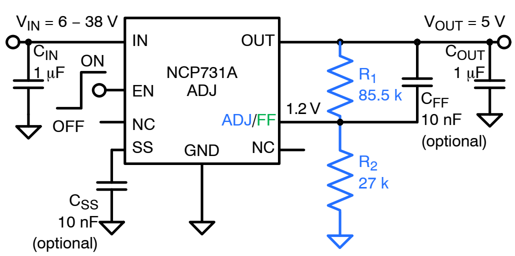


Figure 1. Adjustable Output Voltage Application

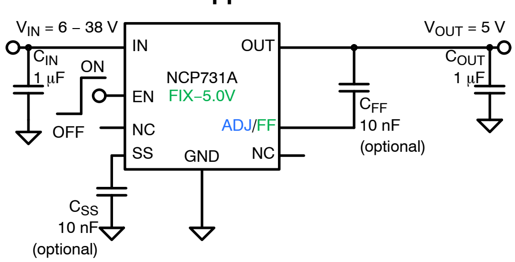


Figure 2. Fixed Output Voltage Application

Notes:
Blue objects are valid for ADJ version only
Green objects are valid for FIX version only
Black objects are common for all version

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

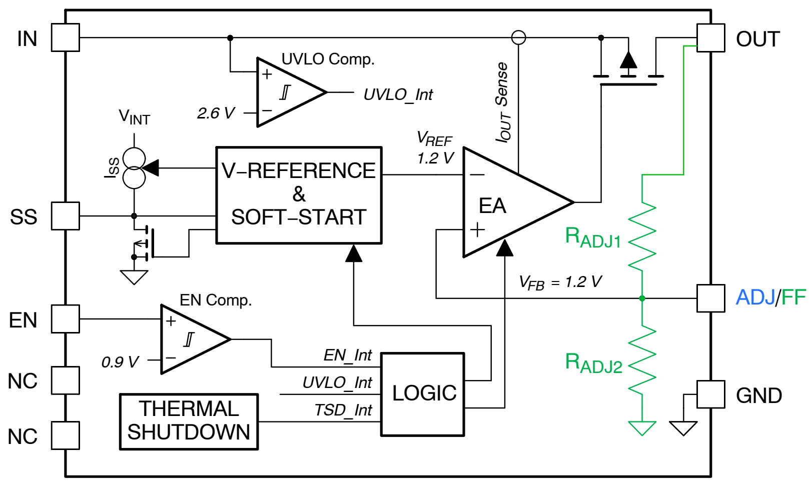


Figure 3. Internal Block Diagram

Notes:
Blue objects are valid for ADJ version only
Green objects are valid for FIX version only
The rest valid for both versions

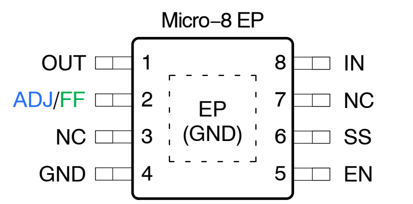


Figure 4. Pin Assignments

PIN DESCRIPTION

Pin Number	Pin Name	Description
8	IN	Power supply input pin.
4	GND	Ground pin.
1	OUT	LDO output pin.
5	EN	Enable input pin (high = enable, low = disable). If this pin is not needed it should be conned to IN pin. No internal pull–up or pull–down circuit is present.
2	ADJ/FF	ADJ version – pin is ADJ • Adjust input pin. Could be connected directly or by the resistor divider to the output pin. FIX versions – pin is FF • Feed forward capacitor pin. Could be connected by C_{FF} capacitor to OUT pin for better dynamic performance & lower noise or left unconnected.
3, 7	NC	Not internally connected. Could be left unconnected or connected to GND.
6	SS	Soft–start input pin. Connect a C_{SS} capacitor to set soft–start time. Could be left floating if not used.
EP	EPAD	Exposed pad, must be connected to GND.

Table 1. MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IN Voltage (Note 1)		V_{IN}	−0.3 to 40	V
OUT Voltage	ADJ Version and FIX Versions with $V_{OUT-NOM} > 6.0$ V	V_{OUT}	−0.3 to [(V_{IN} + 0.3) or 40; whichever is lower]	V
	FIX Versions with $V_{OUT-NOM} \leq 6.0$ V		−0.3 to [(V_{IN} + 0.3) or 7; whichever is lower]	
EN Voltage		V_{EN}	−0.3 to (V_{IN} + 0.3)	V
ADJ/FF Voltage		V_{ADJ}	−0.3 to 5.5	V
SS Voltage		V_{SS}	−0.3 to 5.5	V
Output Current		I_{OUT}	Internally limited	mA
Maximum Junction Temperature		$T_{J(MAX)}$	150	°C
Storage Temperature		T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001, EIA/JESD22−A114
   ESD Charged Device Model tested per ANSI/ESDA/JEDEC JS−002, EIA/JESD22−C101

Table 2. THERMAL CHARACTERISTICS (Note 3)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	44	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JCt}$	99	°C/W
Thermal Resistance, Junction−to−Case (bottom)	$R_{\theta JCb}$	19	°C/W
Thermal Characterization Parameter, Junction−to−Case (top)	Ψ_{JCt}	12	°C/W
Thermal Characterization Parameter, Junction−to−Board [FEM]	Ψ_{JB}	16	°C/W

3. Measured according to JEDEC board specification (board 2S2P, Cu layer thickness 1 oz, Cu area 645mm^2, no airflow). Detailed description of the board can be found in JESD51−7.

Table 3. ELECTRICAL CHARACTERISTICS $V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (Note 4), C_{SS} = 0 nF, C_{FF} = 0 nF, T_J = −40°C to 125°C, ADJ tied to OUT, unless otherwise specified.

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Recommended Input Voltage			V_{IN}	2.7	–	38	V
Output Voltage Accuracy (Note 5)	T_J = +25°C		V_{OUT}	−0.6	–	0.6	%
	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V I_{OUT} = 0.1 mA to 150 mA T_J = −40°C to +85°C			−1.0	–	1.0	
	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V I_{OUT} = 0.1 mA to 150 mA T_J = −40°C to +125°C			−1.5	–	1.5	
Output Voltage Range (Note 6)			$V_{OUT-ADJ}$	V_{ADJ}	–	35	V
ADJ Reference Voltage (Note 6)			V_{ADJ}	–	1.2	–	V
ADJ Input Current (Note 6)	V_{ADJ} = 1.2 V		I_{ADJ}	−0.05	0.01	0.05	μA
Quiescent Current	$V_{IN} = V_{OUT-NOM}$ + 1 V to 38 V, I_{OUT} = 0 mA		I_Q	–	48	100	μA
Ground Current	I_{OUT} = 150 mA		I_{GND}	–	400	–	μA
Shutdown Current	V_{EN} = 0 V, V_{IN} = 38 V		I_{SHDN}	–	0.07	1.0	μA
Output Current Limit	$V_{OUT} = V_{OUT-NOM}$ − 100 mV		I_{OLIM}	210	295	450	mA
Short Circuit Current	V_{OUT} = 0 V		I_{OSC}	210	365	450	mA
Dropout Voltage (Note 7)	I_{OUT} = 150 mA		V_{DO}	–	230	480	mV
Power Supply Ripple Rejection	$V_{IN} = V_{OUT-NOM}$ + 2 V I_{OUT} = 10 mA	10 Hz	PSRR	–	80	–	dB
		10 kHz		–	70	–	
		100 kHz		–	42	–	
		1 MHz		–	48	–	
Output Noise Voltage	f = 10 Hz to 100 kHz, ADJ version, $V_{OUT} = V_{ADJ}$		V_N	–	8.1	–	μVRMS
	f = 10 Hz to 100 kHz, ADJ version, V_{OUT} = 3.3 V, C_{FF} = 10 nF, R_1 = 47.3 kΩ, R_2 = 27 kΩ		V_N	–	15	–	
	f = 10 Hz to 100 kHz, ADJ version, V_{OUT} = 5 V, C_{FF} = 10 nF, R_1 = 85.5 kΩ, R_2 = 27 kΩ		V_N	–	20	–	
EN Threshold	V_{EN} rising		V_{EN-TH}	0.7	0.9	1.1	V
EN Hysteresis	V_{EN} falling		V_{EN-HY}	0.02	0.1	0.2	V
EN Input Current	V_{EN} = 30 V, V_{IN} = 30 V		I_{EN}	−1	0.15	1	μA
Internal UVLO Threshold	V_{IN} voltage rising		$V_{UVLO-TH}$	2.43	2.55	2.69	V
Internal UVLO Hysteresis	V_{IN} voltage falling		$V_{UVLO-HY}$	0.01	0.04	0.07	V
SS Charging Current	V_{SS} = 0 V		I_{SS}	–	910	–	nA
SS High Voltage	SS pin floating		V_{SS-HI}	–	2.4	–	V
SS Time (Note 8)	C_{SS} = 10 nF		$t_{SS-10nF}$	–	14	–	ms
	C_{SS} not connected		t_{SS-0nF}	–	0.5	–	
Thermal Shutdown Temperature	Temperature rising from T_J = +25°C		T_{TSD}	–	170	–	°C
Thermal Shutdown Hysteresis	Temperature falling from TSD		T_{TSDH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Effective capacitance, including the effect of DC bias, tolerance and temperature. See the Application Information section for more information.
5. Output voltage accuracy of ADJ version is guaranteed when ADJ pin is connected to OUT pin. The $V_{OUT-NOM}$ is then equal to V_{ADJ}.
6. Applicable only to ADJ version.
7. Dropout voltage is measured when the output voltage falls 100 mV below the nominal output voltage. ADJ version is measured with ADJ pin connected to resistor divider which sets V_{OUT} to 5.0 V. Limits are valid for all voltage versions.
8. Startup time is the time from EN assertion to point when output voltage is equal to 95% of $V_{OUT-NOM}$.

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq 2.7$ V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

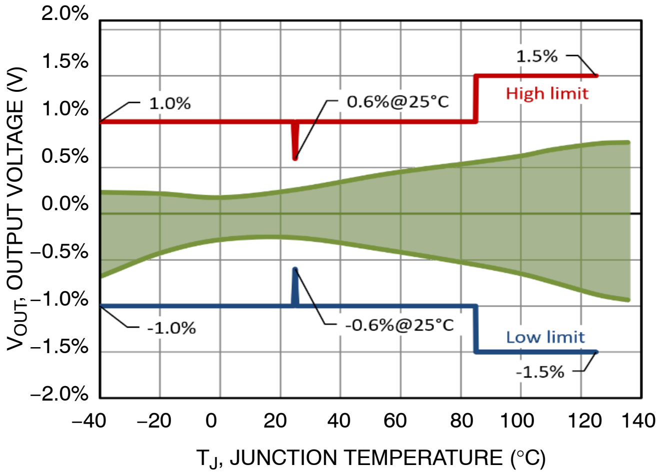


Figure 5. Output Voltage vs. Temperature

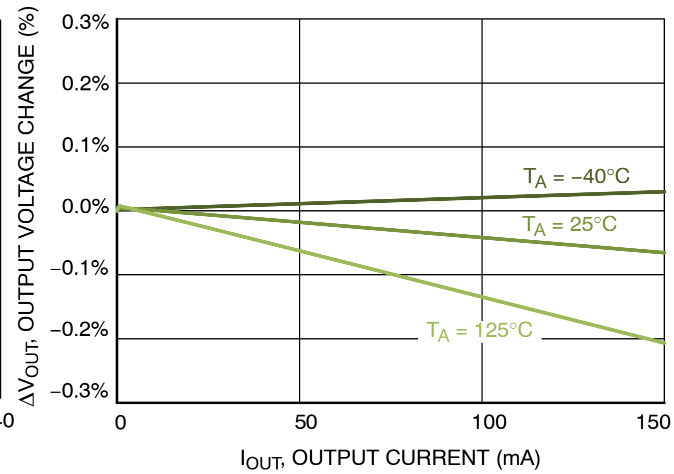


Figure 6. Load Regulations

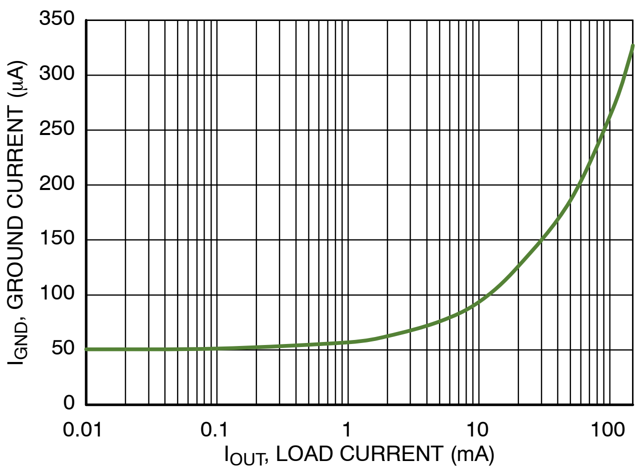


Figure 7. Ground Current vs. Load

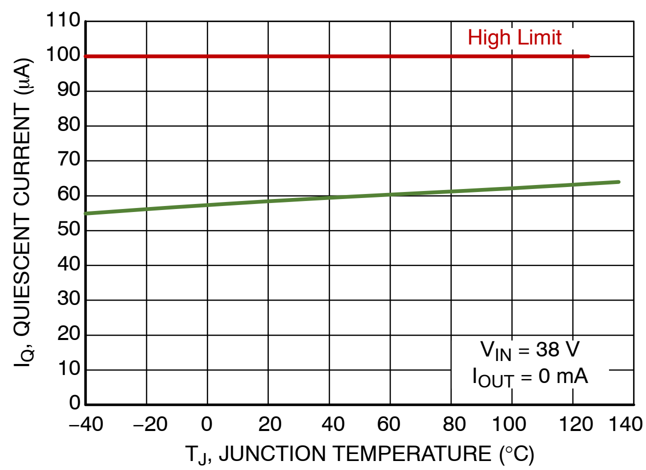


Figure 8. Quiescent Current vs. Temperature

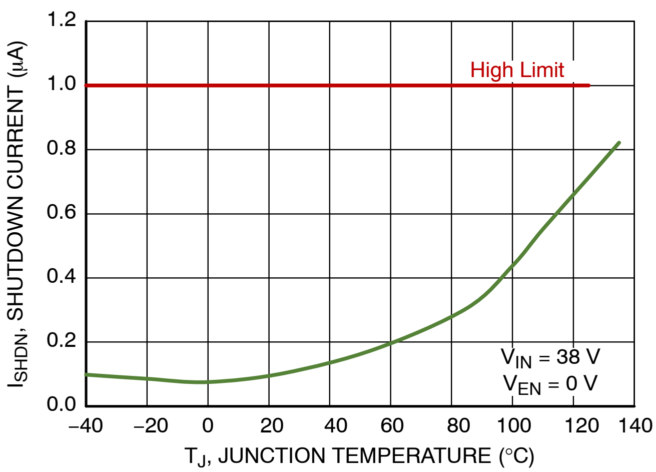


Figure 9. Shutdown Current vs. Temperature

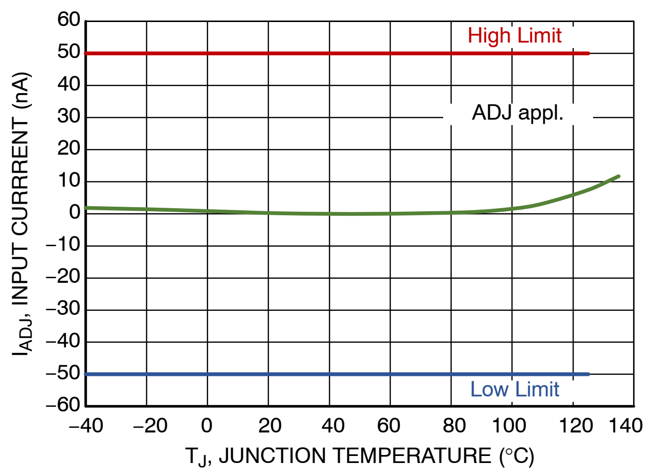


Figure 10. ADJ Input Current vs. Temperature

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40$°C to 125°C, all output voltage versions, unless otherwise specified.

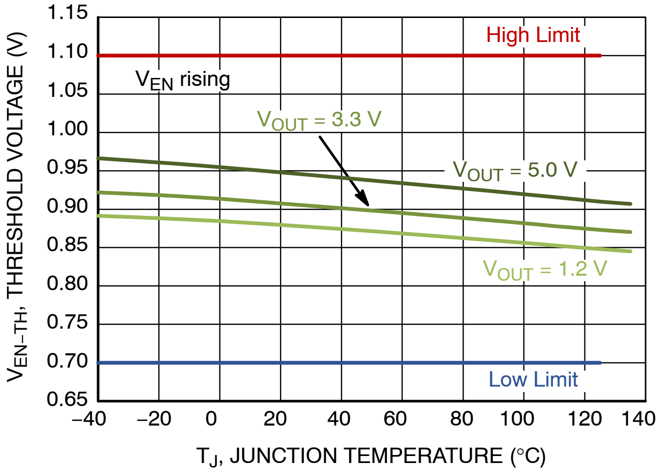


Figure 11. Enable Threshold Voltage vs. Temperature

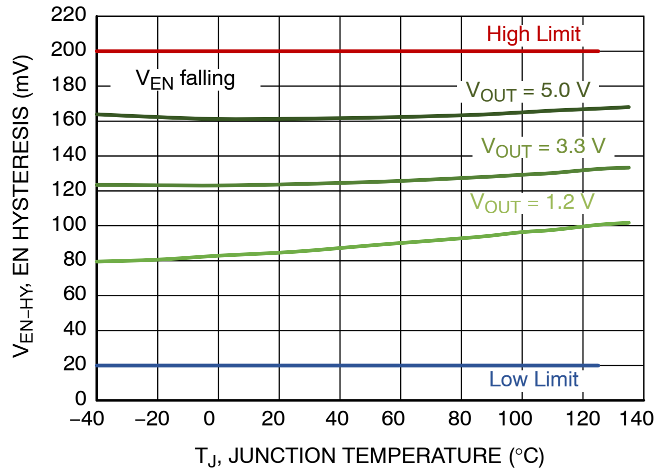


Figure 12. Enable Hysteresis vs. Temperature

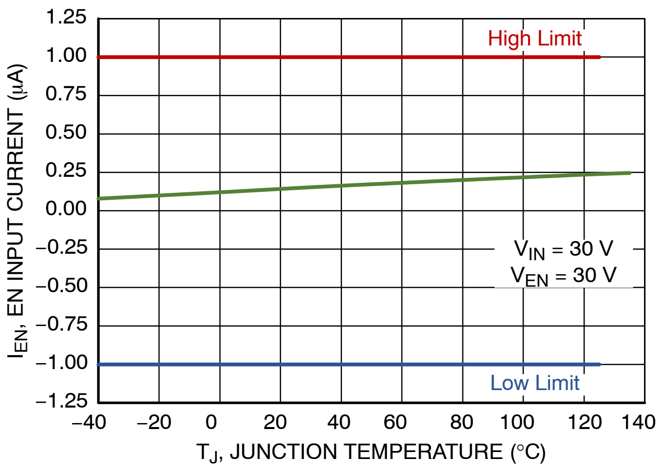


Figure 13. Enable Input Current vs. Temperature

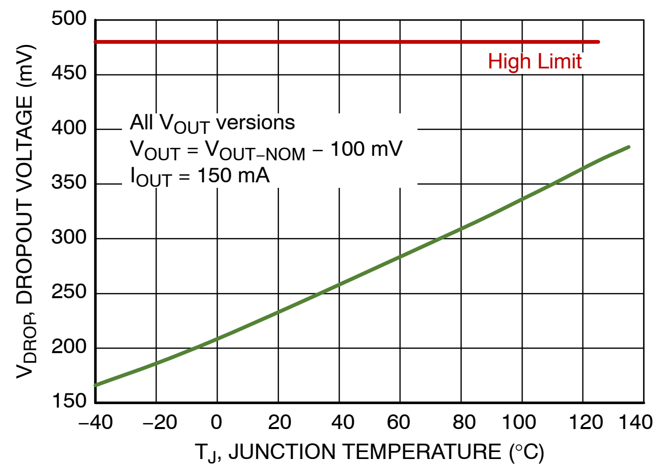


Figure 14. Dropout Voltage vs. Temperature

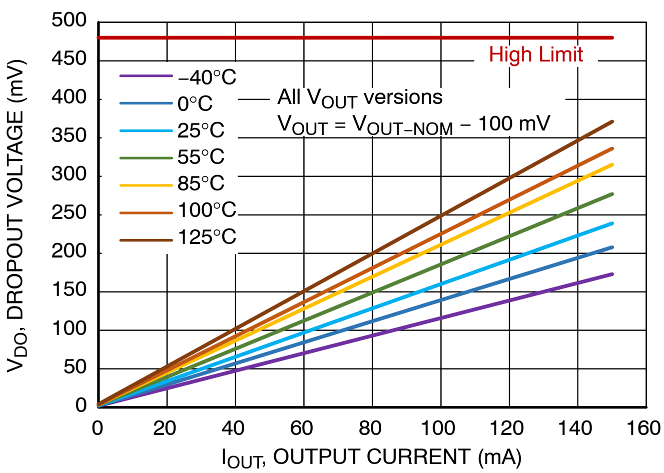


Figure 15. Dropout Voltage vs. I_{OUT}

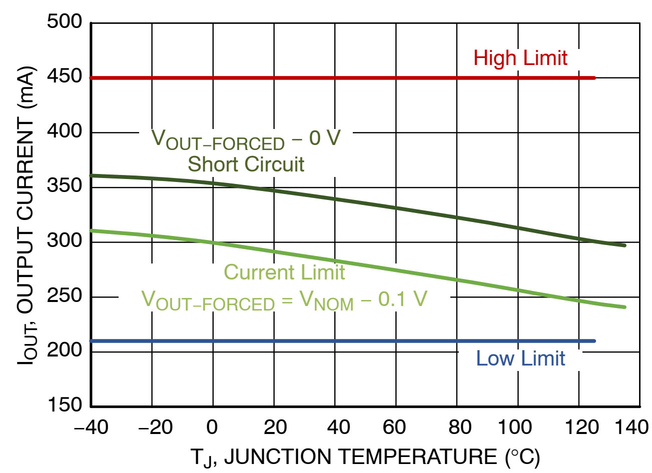


Figure 16. Maximum Output Current vs. Temperature

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM}$ + 1 V and $V_{IN} \geq$ 2.7 V, V_{EN} = 1.2 V, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 µF (effective), C_{SS} = 10 nF, C_{FF} = 10 nF, R_{ADJ1} = 85.5 kΩ, R_{ADJ2} = 27 kΩ (R_{ADJx} applicable to ADJ application only), T_J = −40°C to 125°C, all output voltage versions, unless otherwise specified.

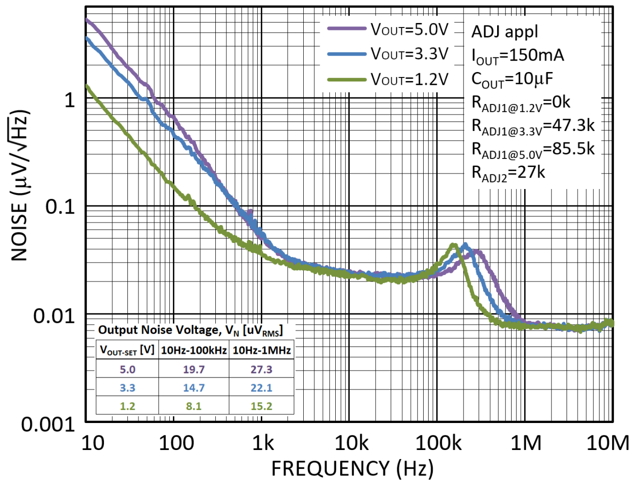


Figure 17. V_{OUT} Noise Density vs. V_{OUT}

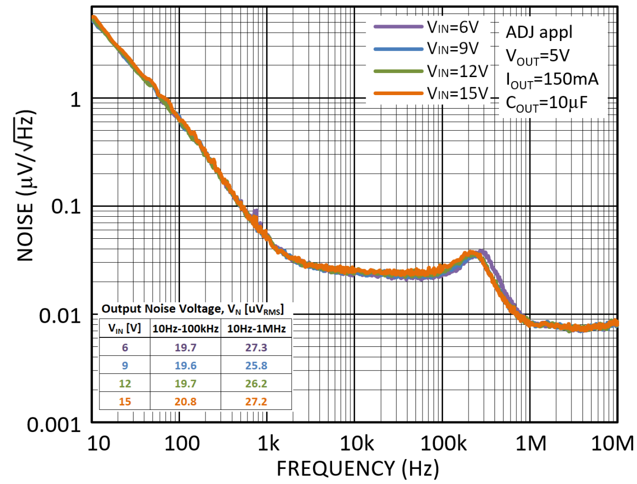


Figure 18. V_{OUT} Noise Density vs. V_{IN}

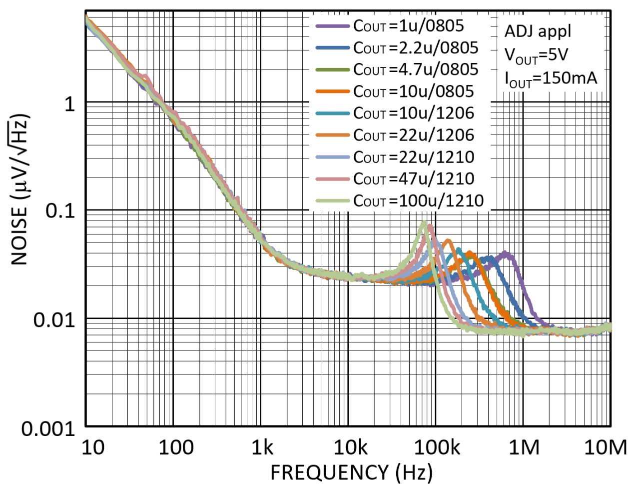


Figure 19. V_{OUT} Noise Density vs. C_{OUT}

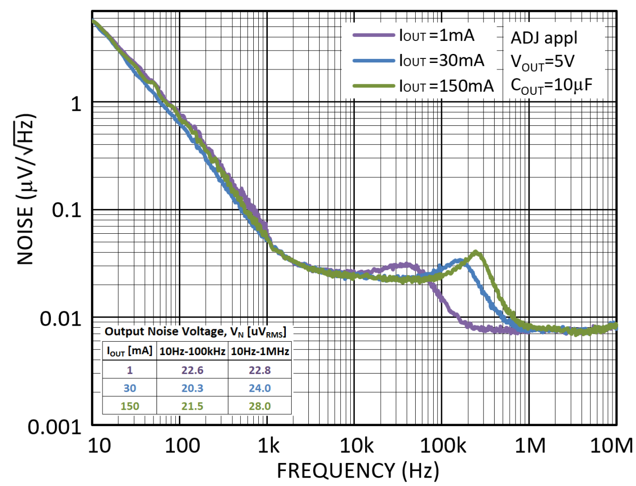


Figure 20. V_{OUT} Noise Density vs. I_{OUT}

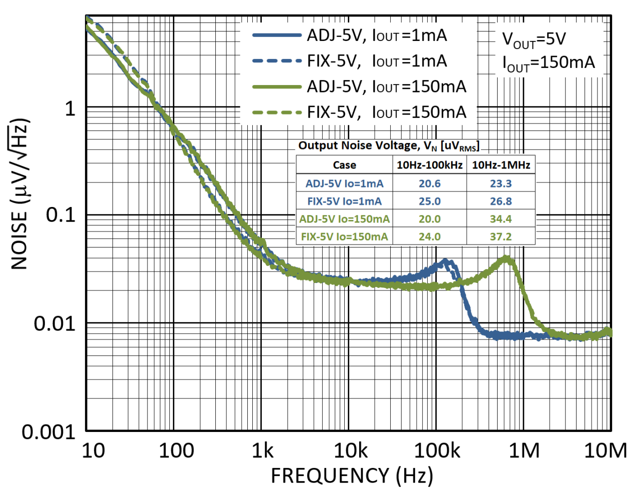


Figure 21. V_{OUT} Noise Density vs. Part−type and I_{OUT}

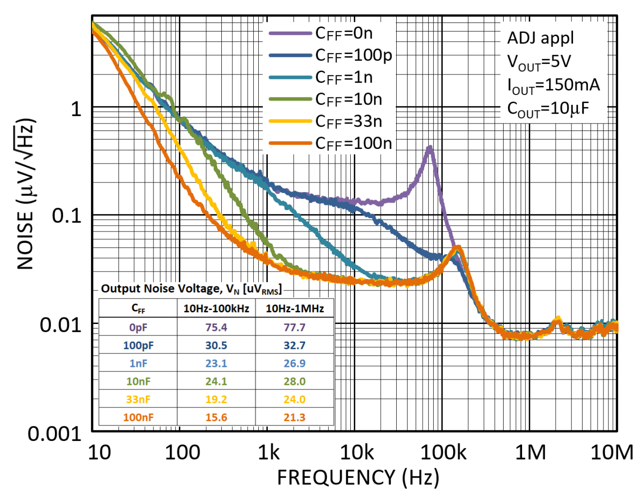


Figure 22. V_{OUT} Noise Density vs. C_{FF}

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40$°C to 125°C, all output voltage versions, unless otherwise specified.

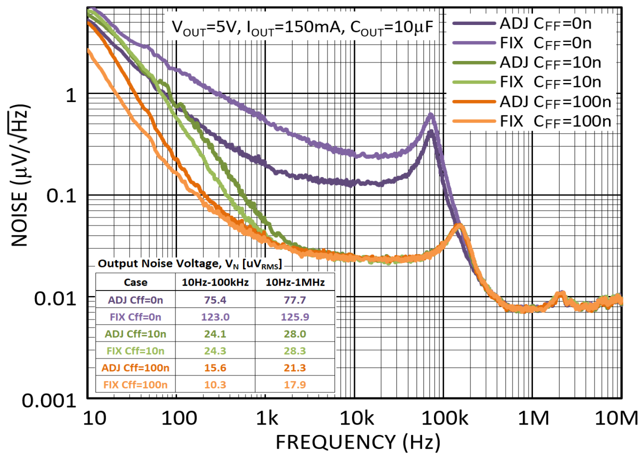


Figure 23. V_{OUT} Noise Density vs. Part−type and C_{FF}

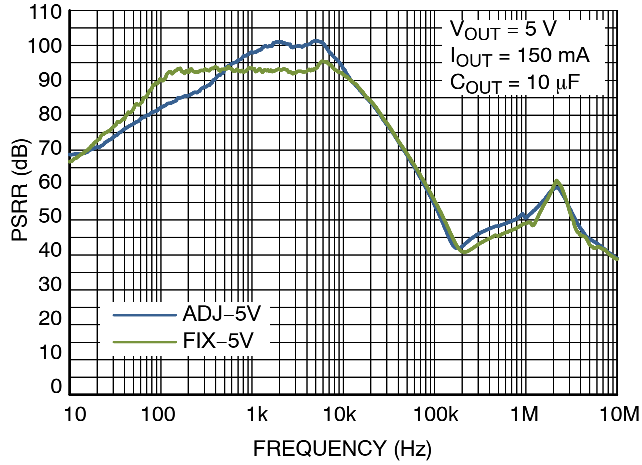


Figure 24. PSRR vs. Part−type

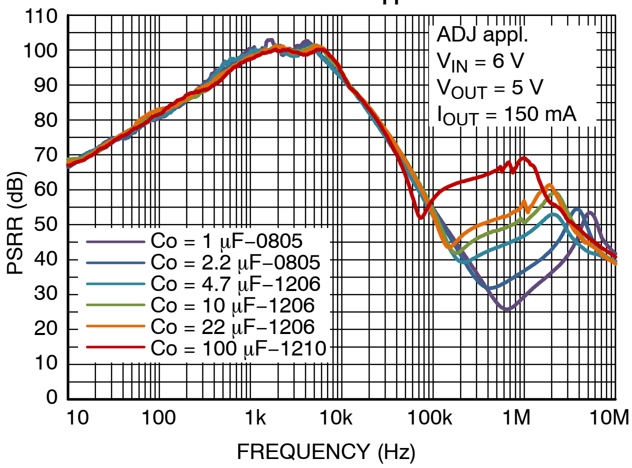


Figure 25. PSRR vs. C_{OUT} (6.0 V, 150 mA)

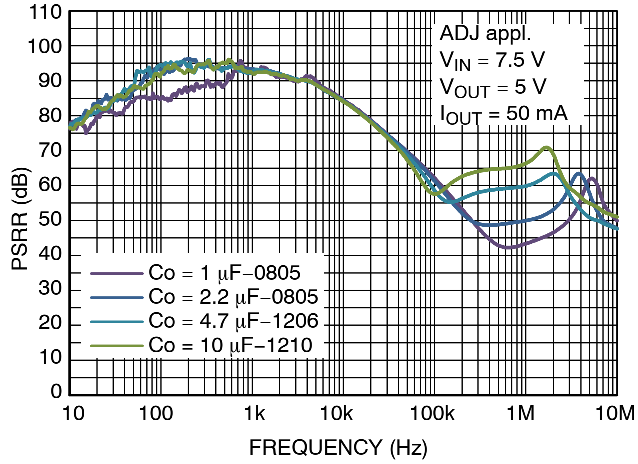


Figure 26. PSRR vs. C_{OUT} (7.5 V, 50 mA)

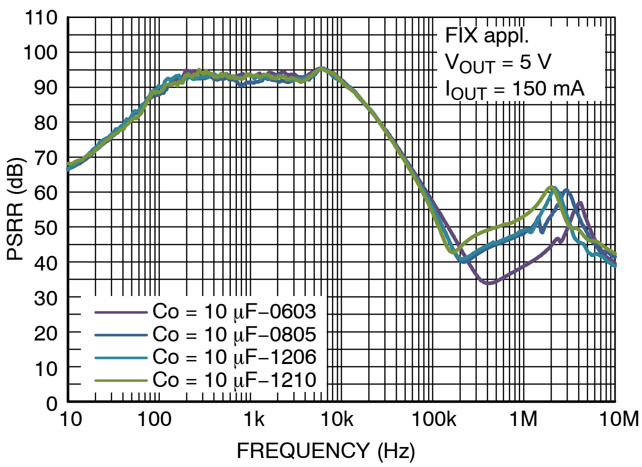


Figure 27. PSRR vs. C_{OUT} Package Size

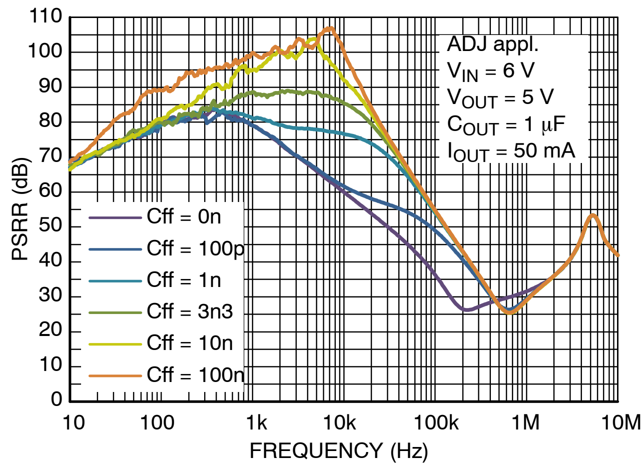


Figure 28. PSRR vs. C_{FF}

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40$°C to 125°C, all output voltage versions, unless otherwise specified.

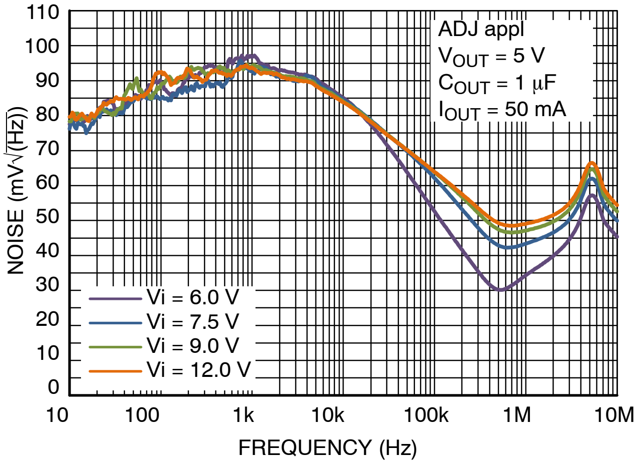


Figure 29. PSRR vs. V_{IN} (50 mA, 1 µF)

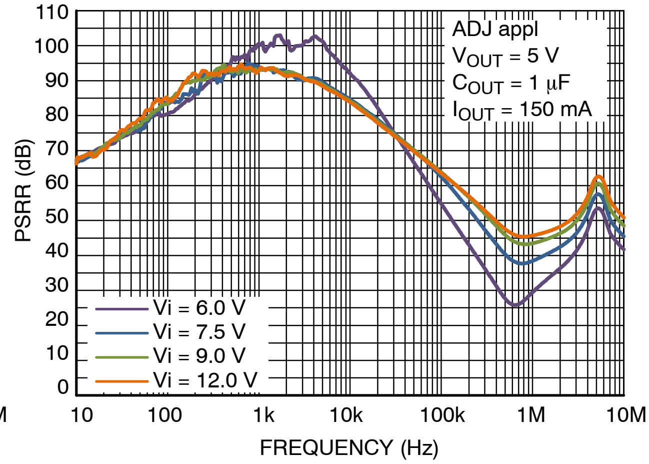


Figure 30. PSRR vs. V_{IN} (150 mA, 1 µF)

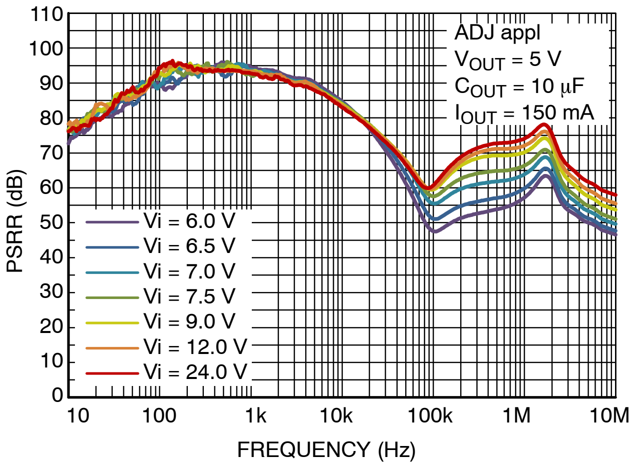


Figure 31. PSRR vs. V_{IN} (50 mA, 10 µF)

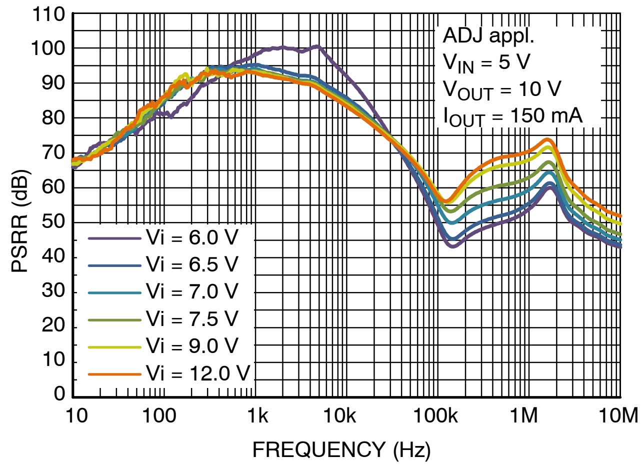


Figure 32. PSRR vs. V_{IN} (150 mA, 10 µF)

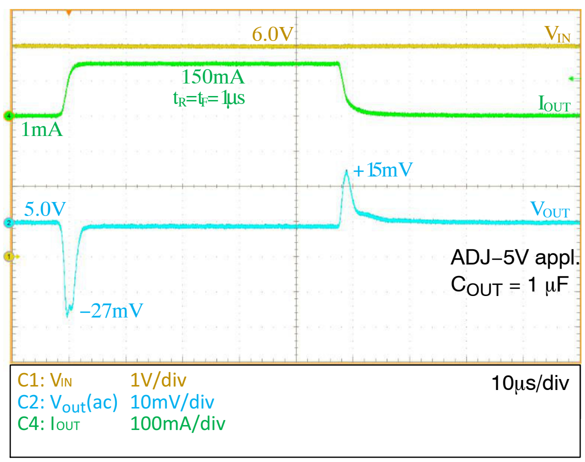


Figure 33. Load Transient Response ($ADJ-5V$, $V_{IN} = 6.0$ V, $C_{OUT} = 1$ µF)

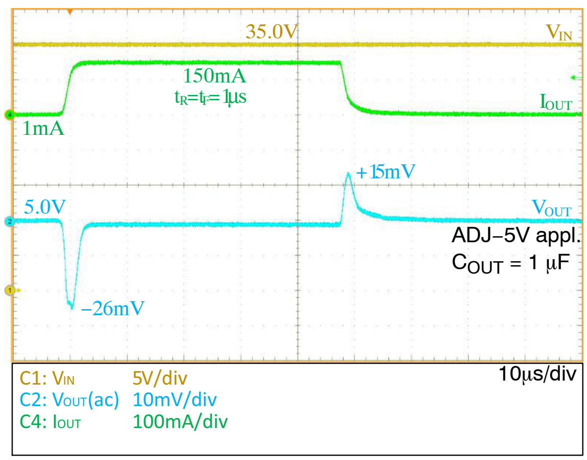


Figure 34. Load Transient Response ($ADJ-5V$, $V_{IN} = 35.0$ V, $C_{OUT} = 1$ µF)

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40$°C to 125°C, all output voltage versions, unless otherwise specified.

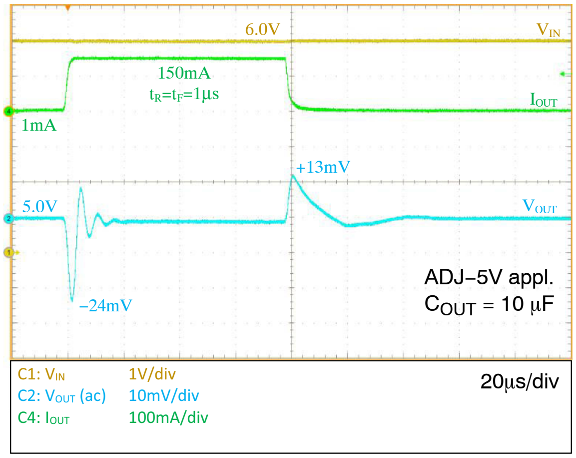


Figure 35. Load Transient Response (ADJ−5V, V_{IN} = 6.0 V, C_{OUT} = 10 µF)

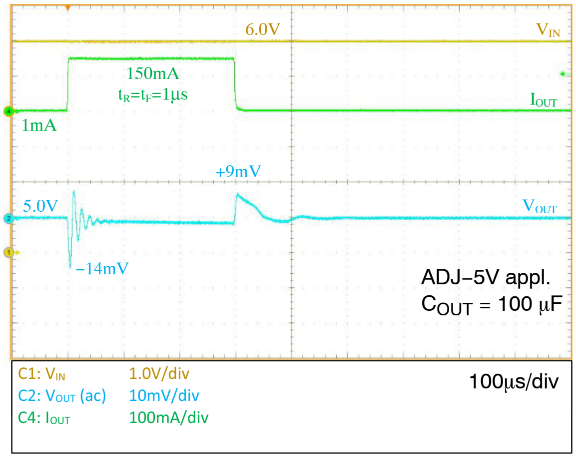


Figure 36. Load Transient Response (ADJ−5V, V_{IN} = 6.0 V, C_{OUT} = 100 µF)

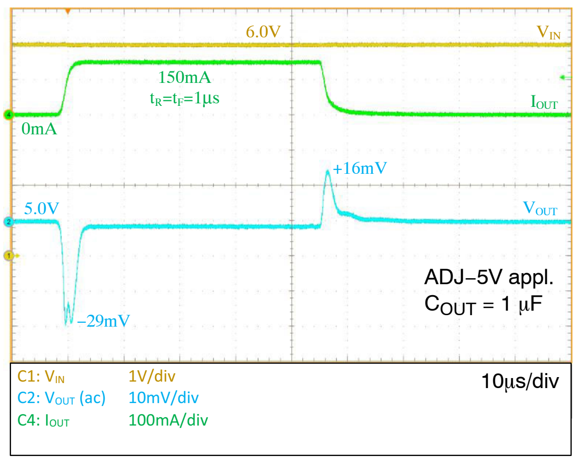


Figure 37. Load Transient Response (V_{IN} = 6.0 V, I_{OUT} = 0 − 150 mA)

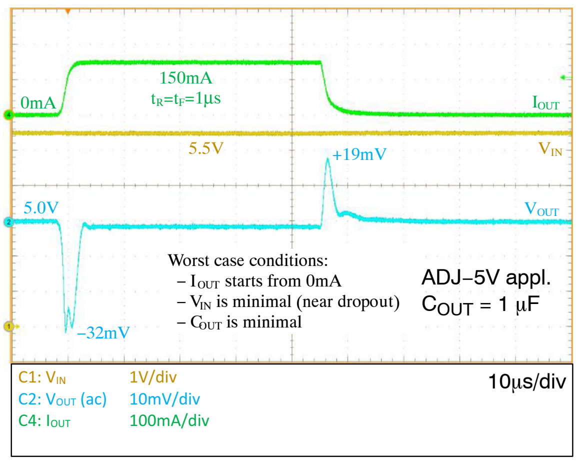


Figure 38. Load Trans. Response (V_{IN} = 5.5 V, I_{OUT} = 0 − 150 mA ~ Worst Conditions)

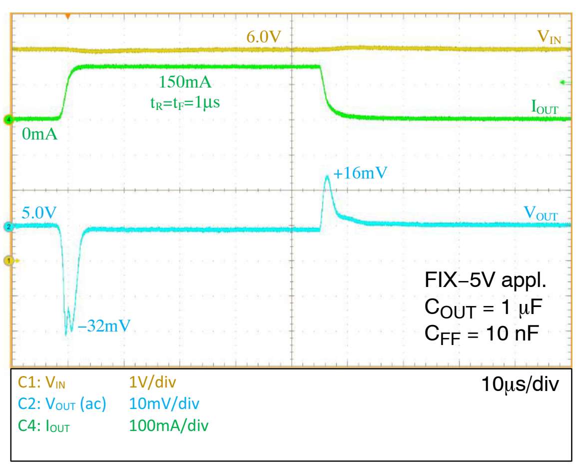


Figure 39. Load Transient Response (FIX−5V, V_{IN} = 6.0 V, C_{OUT} = 1 µF)

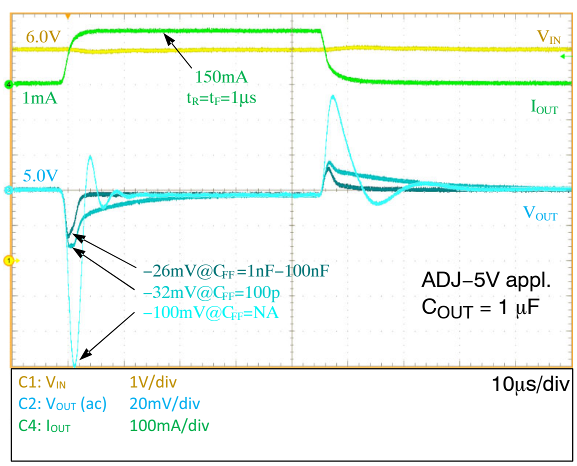


Figure 40. Load Transient Response (ADJ−5V, C_{FF} = variable)

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ μF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40°C$ to 125°C, all output voltage versions, unless otherwise specified.

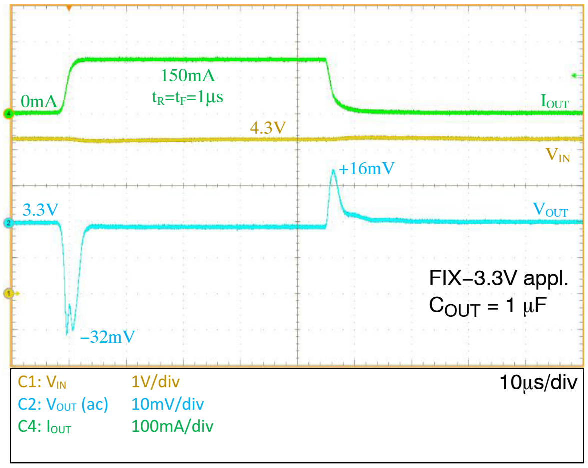


Figure 41. Load Transient Response ($FIX-3.3V$, $V_{IN} = 4.3$ V, $C_{OUT} = 1$ μF)

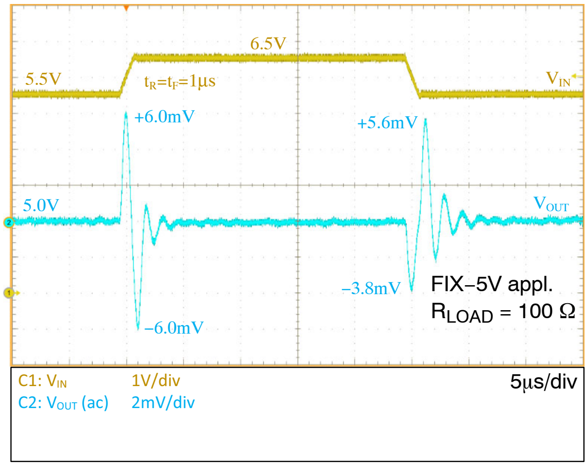


Figure 42. Line Transient Response ($V_{OUT} = 5.0$ V, $V_{IN} = 5.5 – 6.5$ V)

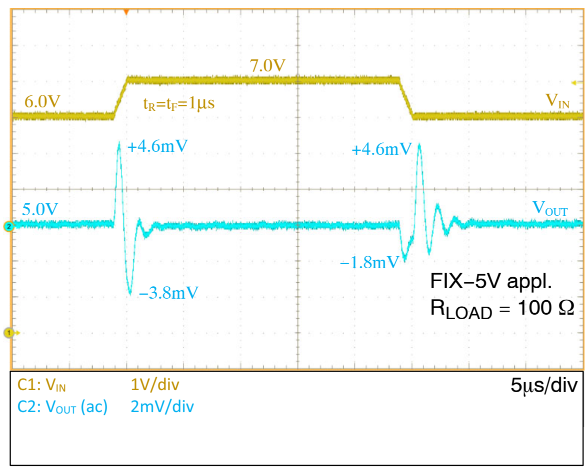


Figure 43. Line Transient Response ($V_{OUT} = 5.0$ V, $V_{IN} = 6.0 – 7.0$ V)

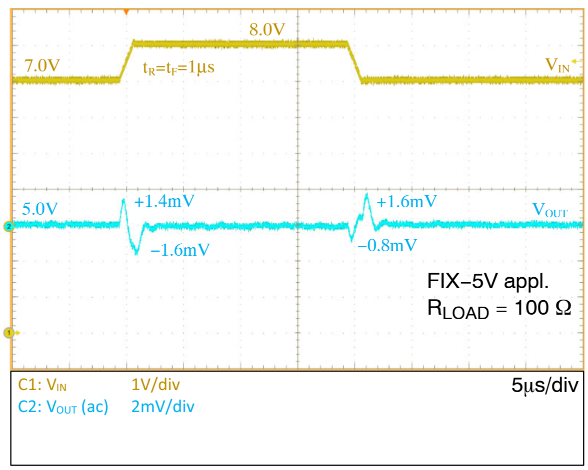


Figure 44. Line Transient Response ($V_{OUT} = 5.0$ V, $V_{IN} = 7.0 – 8.0$ V)

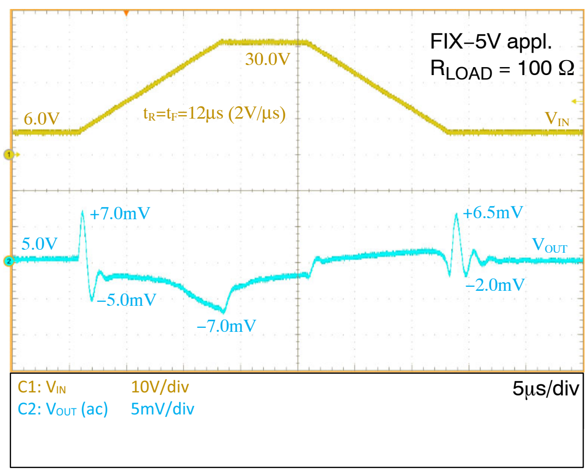


Figure 45. Line Transient Response ($V_{OUT} = 5.0$ V, $V_{IN} = 6.0 – 30.0$ V)

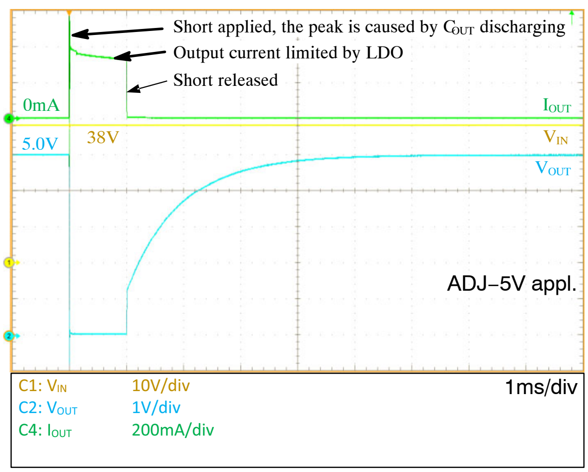


Figure 46. Short Circuit (1 ms)

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40$°C to 125°C, all output voltage versions, unless otherwise specified.

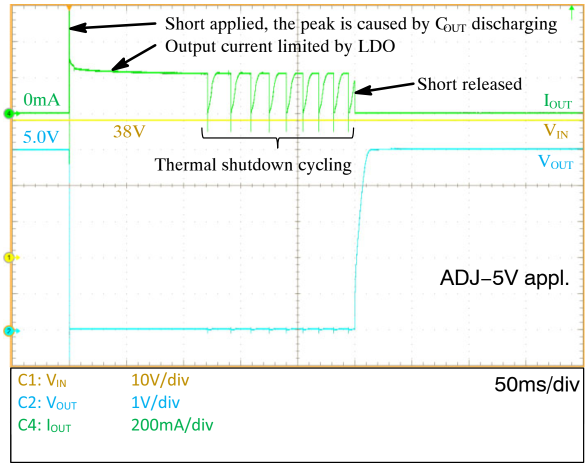


Figure 47. Short Circuit (250 ms)

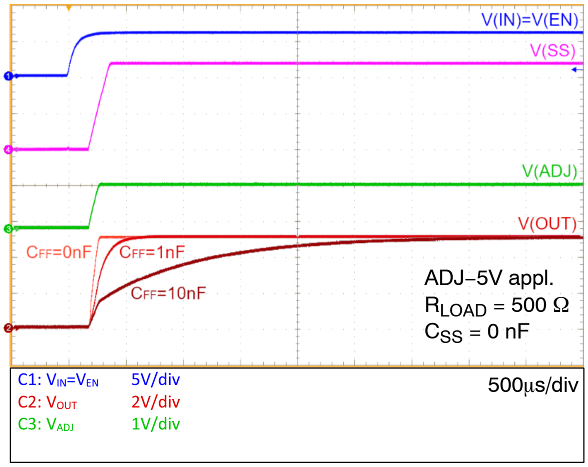


Figure 48. Startup by V_{IN} (ADJ−5V, C_{SS} = 0 nF)

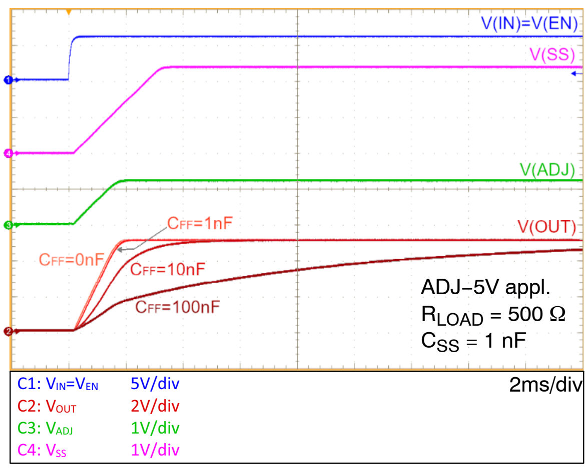


Figure 49. Startup by V_{IN} (ADJ−5V, C_{SS} = 1 nF)

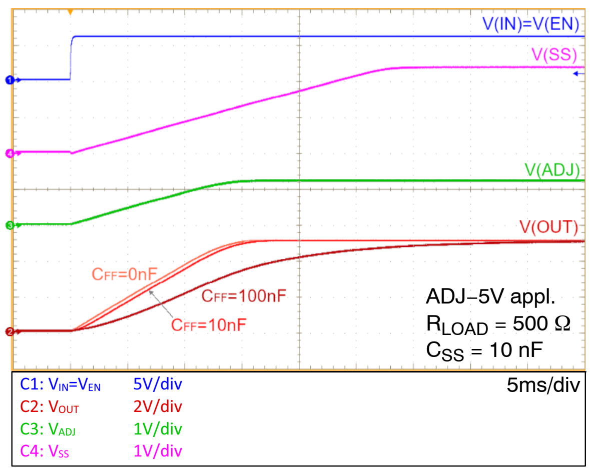


Figure 50. Startup by V_{IN} (ADJ−5V, C_{SS} = 10 nF)

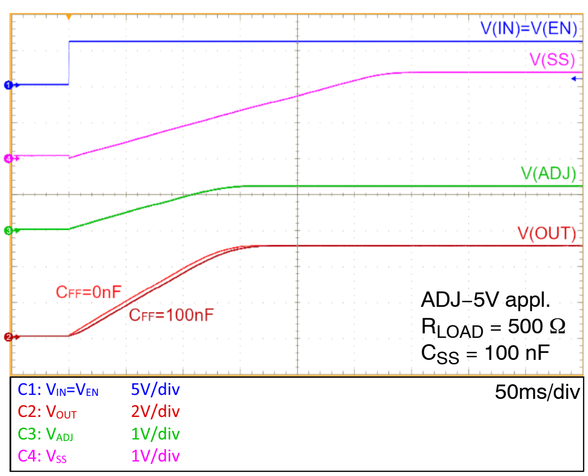


Figure 51. Startup by V_{IN} (ADJ−5V, C_{SS} = 100 nF)

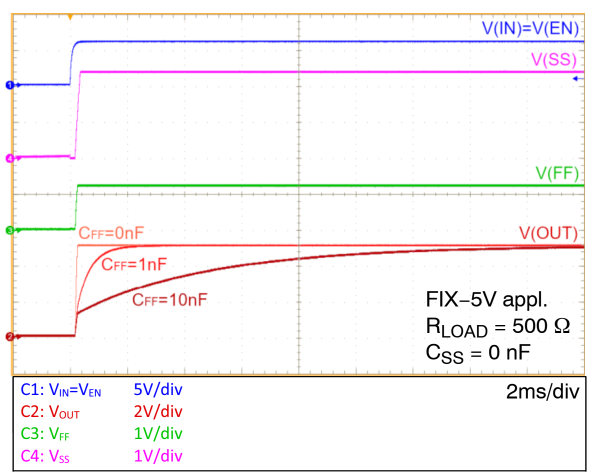


Figure 52. Startup by V_{IN} (FIX−5 V, C_{SS} = 0 nF)

TYPICAL CHARACTERISTICS

$V_{IN} = V_{OUT-NOM} + 1$ V and $V_{IN} \geq 2.7$ V, $V_{EN} = 1.2$ V, $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1.0$ µF (effective), $C_{SS} = 10$ nF, $C_{FF} = 10$ nF, $R_{ADJ1} = 85.5$ kΩ, $R_{ADJ2} = 27$ kΩ (R_{ADJx} applicable to ADJ application only), $T_J = -40$°C to 125°C, all output voltage versions, unless otherwise specified.

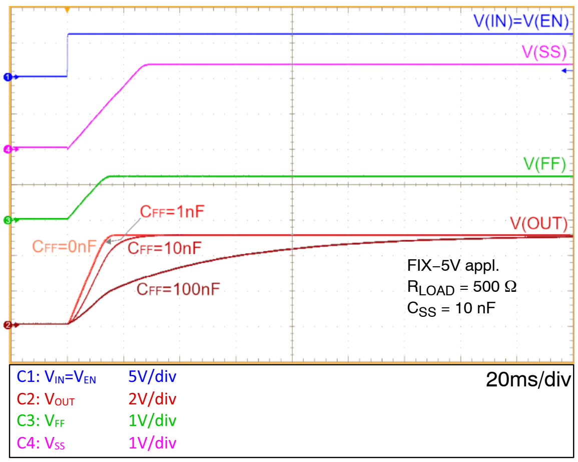


Figure 53. Startup by V_{IN} (FIX–5V, C_{SS} = 10 nF)

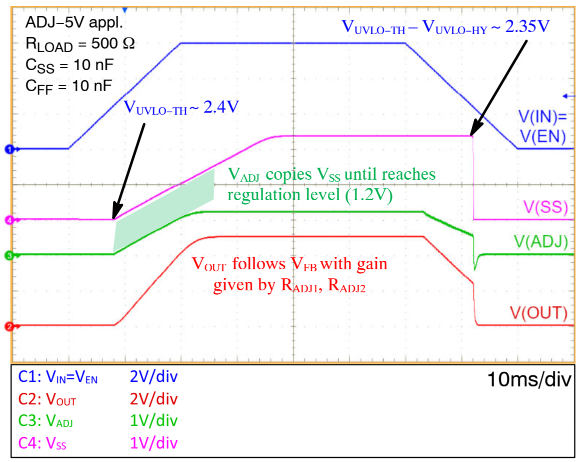


Figure 54. Startup/Shutdown by V_{IN} (Slow Rising Edge)

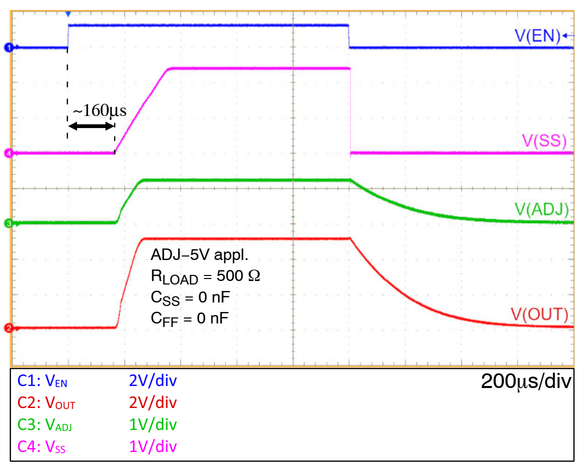


Figure 55. Startup/Shutdown by V_{EN} (Fast Rising Edge)

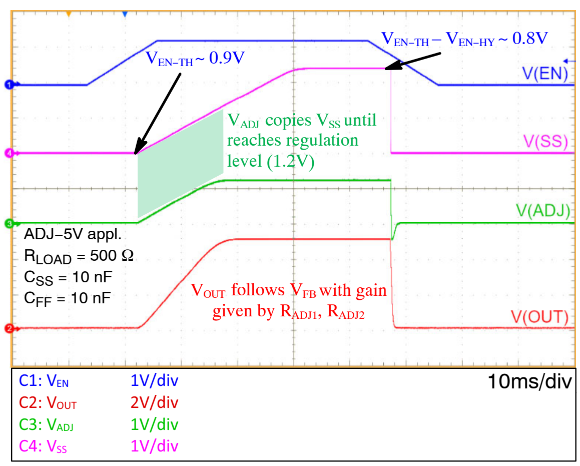
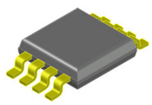


Figure 56. Startup/Shutdown by V_{EN} (Slow Rising Edge)

ORDERING INFORMATION

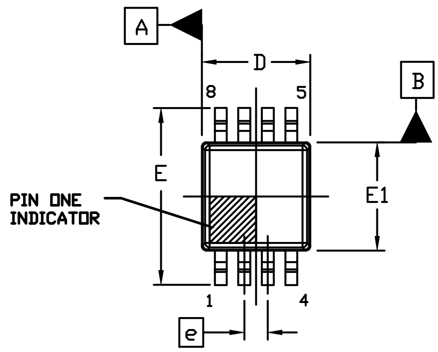
Part Number	Marking	Voltage Option ($V_{OUT-NOM}$)	Package	Shipping†
NCP731ADN330R2G	731A33	FIX, 3.3 V	MSOP8 EP (Pb−Free)	3000 / Tape & Reel
NCP731ADN500R2G	731A50	FIX, 5.0 V		
NCP731ADNADJR2G	731AAD	ADJ, 1.2 V		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



MSOP8 EP 3x3
CASE 846AT
ISSUE O

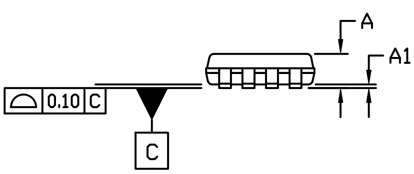
DATE 01 OCT 2020



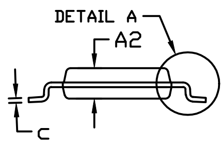
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS b AND c APPLY TO THE PLATED LEADS.
5. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

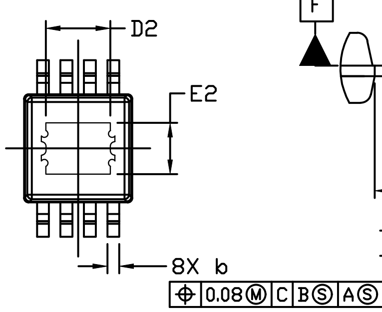
DIM	MILLIMETERS MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.10	0.15
A2	0.813	0.863	0.914
b	0.28	---	0.38
c	0.139	---	0.23
D	2.90	3.00	3.10
D2	1.50	1.70	1.80
E	4.775	4.876	4.978
E1	2.90	3.00	3.10
E2	1.14	1.40	1.50
e	0.65 BSC		
L	0.40	---	---
L1	0.94 REF		
L2	0.25 REF		
M	0°	---	8°



SIDE VIEW

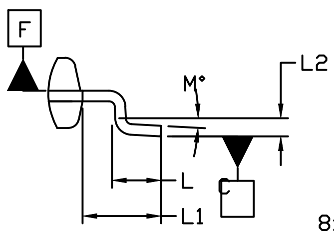


END VIEW

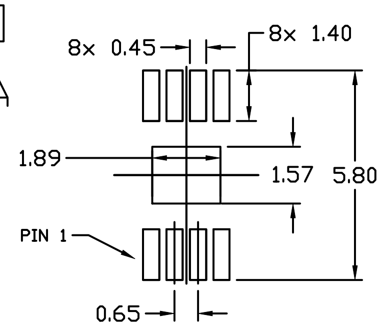


BOTTOM VIEW

NOTE 3



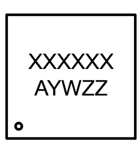
DETAIL A



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	MSOP8 EP 3x3	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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Email Requests to: orderlit@onsemi.com

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative